Fabrication of a 3D nano-imprint template with a conformal dry vapor deposited electron beam resist

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ABSTRACT

Nano-Imprint lithography has garnered much interest in the microlithography and nano-fabrication communities, and appears on the ITRS as a possible future lithography solution. The promise of this approach includes realization of ultimately finer features than might be possible through optical lithography and simplification of mask pattern complexity through the elimination of optical enhancements such as phase shifting and optical proximity correction. Imprinting approaches have demonstrated that sub-50nm lithography of 2D structures is possible using this approach. A potentially enabling method to enhancing imprint lithography is to add additional structures to a 2D template to form 3D profiles, thereby realizing additional benefits that can be achieved through imprinting 3D structures. In this paper we discuss fabrication of such a template, which has the potential to eliminate masking layers by allowing for two or more layers to be imprinted with a single template. A 2D template is formed on a fused silica substrate using Quantiscript's QSR-5 sterol-based vapor deposited electron beam resist, low energy e-beam lithography and reactive ion etching of the underlying substrate. Vapor deposition is especially conducive for patterning ultra thin (<50nm) layers of resist on imprint templates where high resolution structures on the order of 50-100nm are desired. After complete fabrication of the 2D template, a second resist vapor deposition, lithography and etch sequence is performed to add the 3D structures. Since the QSR-5 vapor deposited resist exhibits substrate conformal properties, uniformly thin coatings can be achieved on both 2D surfaces, allowing for high resolution trench-bottom or ridge/mesa-top lithography and processing while simultaneous protection of the initial 2D structures is realized.

Keywords: Imprint, Nanoimprint, Templated, 3D template

1. CONTEXT

Nano-imprint lithography is currently a candidate technology on the International Technology Roadmap for Semiconductors at the 32 nm node[1]. In order to overcome barriers to acceptance by the IC fabrication community, one must identify cost saving advantages that could be obtained by the introduction of this technology into the chip fabrication processes. One major cost savings that might be realized could arise from the adoption of multiple layer lithography in a single-step, made possible by the fabrication of 3-dimensional nano-imprint templates[2]. This type of template has been the object of various research activities over the past few years and its feasibility has been demonstrated for the specific applications of T-gate formation for high speed transistor [3, 4, 5], as well as for more complex structures such as air bridges for monolithic microwave integrated circuits [4]. Another tantalizing application is the potential fabrication of a metal interconnect and the via level in a single lithography step. If an appropriate 3D template can be fabricated to address this issue, an extremely significant reduction in the number of overall processing steps in the fabrication of a leading edge integrated circuit could be accomplished.

In previously published work by other groups[3,4], the 3D templates were constructed using a single plasma etching step with three dimensional etch mask on the surface of the substrate, usually prepared with multilayer coatings through electron beam lithography. These coatings must provide the possibility of selectivity in a dry etching step. While this technique demonstrates the feasibility of the 3D imprint technique, each new pattern requires a custom and complex etch mask, generally limited to a 2-layer structure. A simpler yet more versatile approach has been developed and is presented here. It makes use of a conformal resist process which can be deposited on top of any pattern which has previously been etched into the template substrate. This removes many of the disadvantages tied to the preparation of the 3 dimensional etch mask and allows for the pattern transfer of a certain class of 3D patterns which simply could not be prepared using only a single step resist etch mask. This class of patterns includes those required for preparing templates to be used for the single step lithography of interconnects with vias.

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In order to highlight the differences brought about by the new approach, the fabrication method used by other groups to prepare 3D templates will first be illustrated in figure 1. The basic principle is the etch mask with two metal layers which can be wet etched in a selective fashion. The metal layers can be deposited onto the template surface using electron beam lithography with a two layer resist system to fabricate the basic shape, and lift-off after metal evaporation of the two layers.

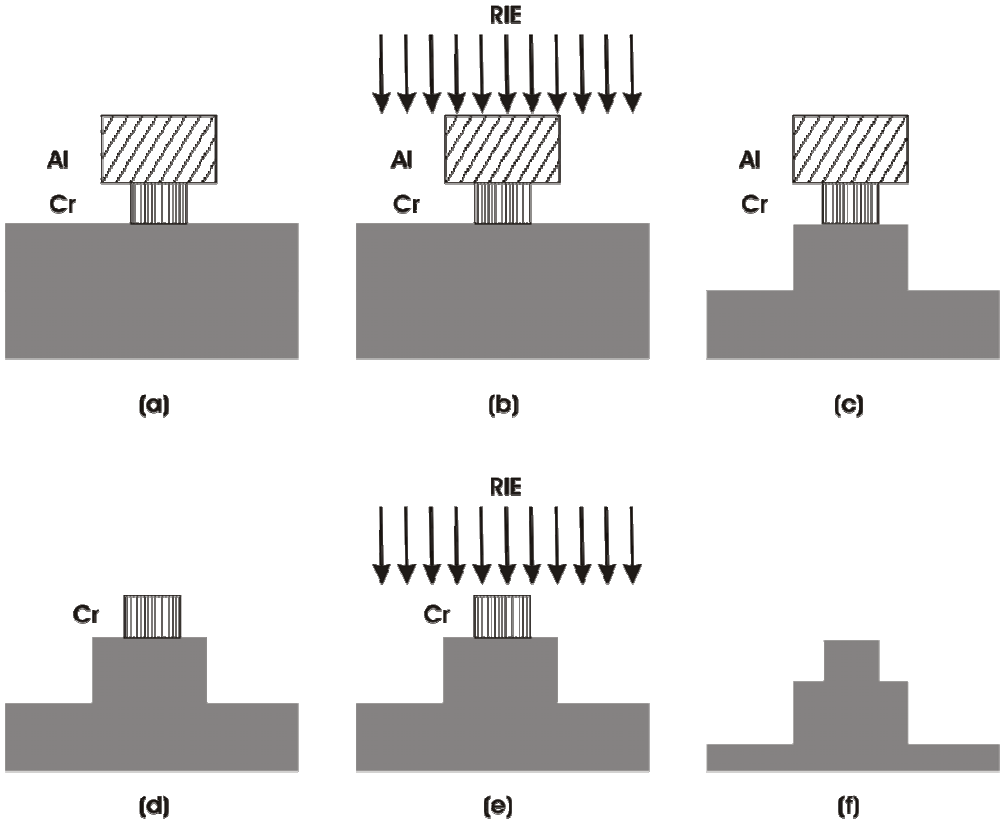


Figure 1. Example of fabrication process used by other authors for the preparation of a 3D nanoimprint template, using two etch selective layers; a) Al and Cr etch mask patterned by ebeam lithography in a two step evaporation; b) reactive ion etching of template substrate; c) resulting structure; d) selective wet etch of Al layer; e) second reactive ion etching step; f) final pattern etched into template after Cr pattern removal.

This process works very well for structures such as T-gates. However, in the case of an interconnect pattern with vias, the situation becomes much more complex. Indeed, figure 2a illustrates the type of etch mask using a two layer metal system that would be required for dry etching the T-gate imprint template in a perspective view. This is a fairly straightforward structure to obtain using lift-off. In order to fabricate the etch mask structure needed for an interconnect/via imprint template, the pattern that would be required is illustrated in figure 2b, and cannot be prepared in a one-step lift-off process.

The actual pattern that must be obtained in the template after dry etching is represented in figure 3. This particular structure is very versatile, with via pillars both on top and on the bottom of the interconnect ridges. The use of a conformal electron beam resist makes it quite straightforward to fabricate this template, as will be demonstrated in the following section.

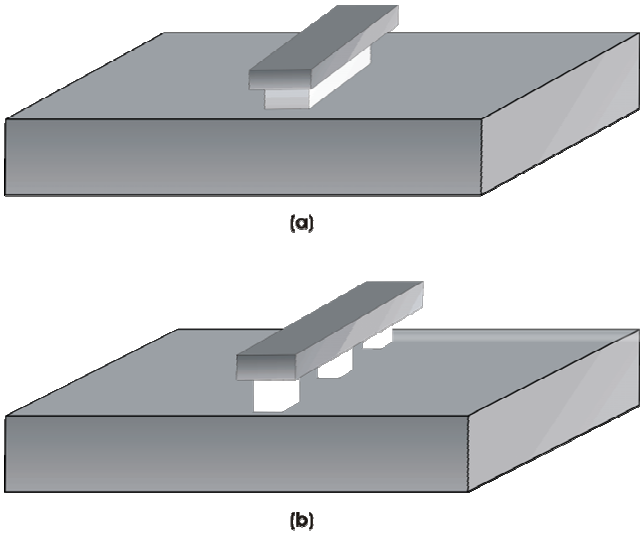


Figure 2. Illustration of the 2 layer metal etch mask approach; a) etch mask for fabricating a T-gate imprint template; b) etch mask required for fabricating an interconnect/via imprint template.

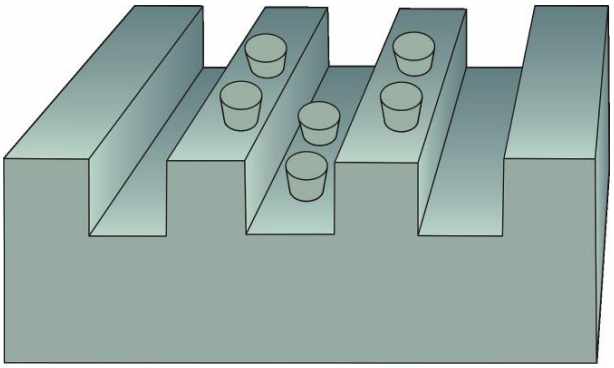


Figure 3 Illustration of a 3D imprint template capable of being used for the fabrication of interconnects and vias in a single lithography step. Posts at the bottom and top of ridges make it possible to address multi-level vias in the single step.

2. FABRICATION PROCESS USING CONFORMAL ELECTRON BEAM RESIST

A conformal negative electron beam resist (QSR-5) which is vacuum evaporated has been developed by Quantiscript and has been used for several different types of applications [6, 7, 8], including the fabrication of various types of advanced lithography masks such as X-ray and LEEPL masks and nanoimprint masks and templates. The conformal properties of the resist are clearly illustrated in figure 4 where the resist has been deposited on a patterned silicon wafer. This wafer has been previously wet etched following a photolithography step in order to produce v-grooves. Figure 4(b) shows a micrograph of an 85 nm thick resist layer at the bottom of the v-groove, clearly showing that the thickness is not affected by the high relief of the substrate surface. Figure 4(c) shows patterning by electron beam lithography of the resist at the top juncture of the v-groove. This micrograph shows that, provided good depth of focus is obtained with the

electron beam system, it is possible to perform lithography throughout a non-flat surface without significantly affecting the critical dimensions of the pattern. This resist is thus ideally suited to be used to fabricate the 3D template required for the interconnect/via lithography. A process flow for this type of fabrication is illustrated in figure 5, showing the main steps required for pattern transfer into the template, independently of whether the substrate is silicon or fused silica. Figure 5a shows the template substrate which has already been patterned via a lithography step to obtain the interconnect pattern etched into the surface. The second step is the thermal evaporation of the conformal resist, QSR-5, followed by electron beam exposure of the resist (figure 5.c). The next step is development of the resist followed by reactive ion etching to transfer the pattern into the substrate. After removal of the resist, the obtained template has a complete 2-level pattern of the interconnects and the vias for transfer into a resist layer by either hot embossing or UV exposure imprint lithography.

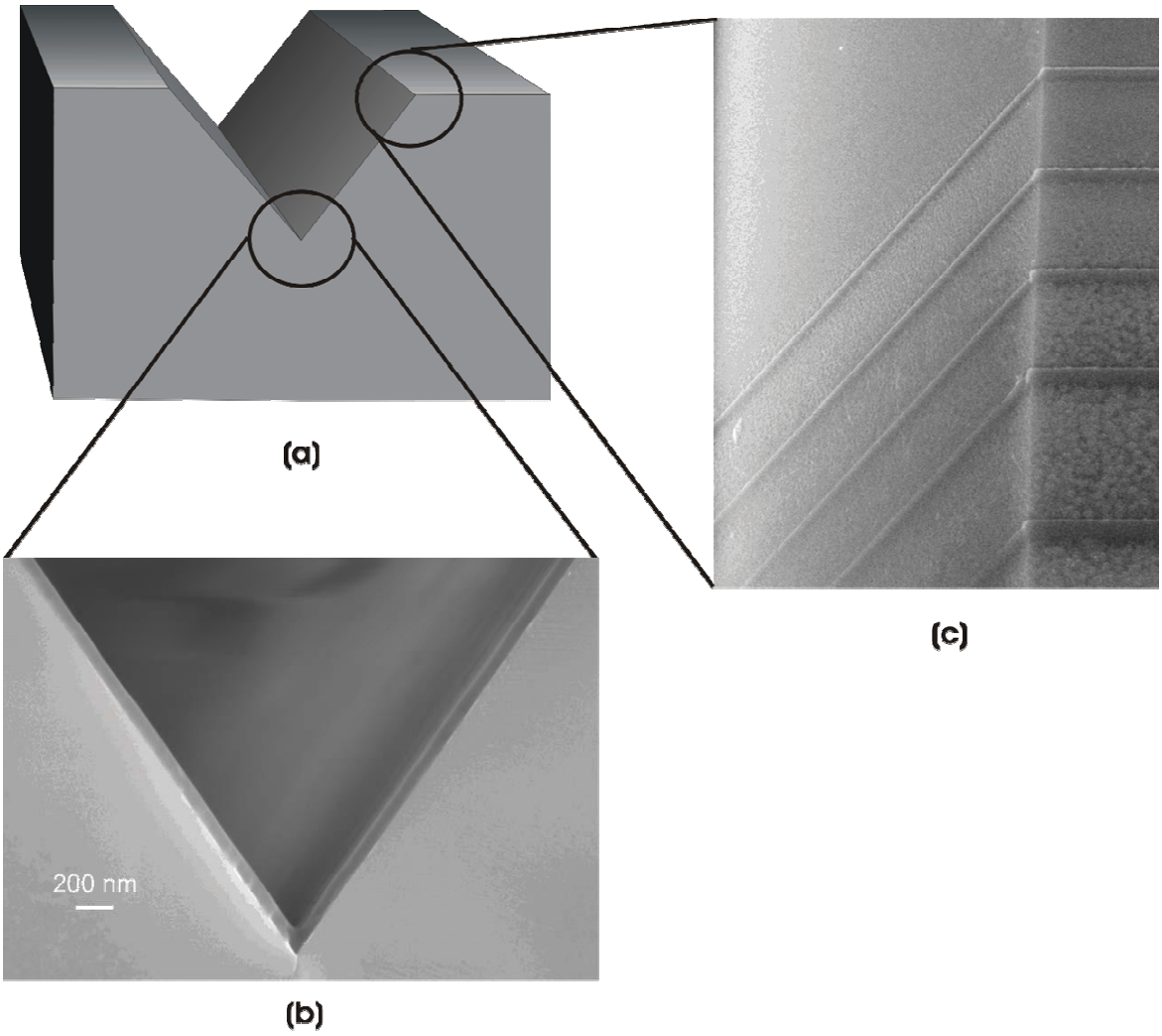


Figure 4 Micrographs and schematic illustration of conformal properties of QSR-5 resist; a) schematic illustration of v-groove etched into silicon wafer; b) micrograph of 85 nm thick QSR-5 resist at bottom of v-groove; c) micrograph of QSR-5 resist after lithography and development, shown at top of v-groove structure.

3. RESULTS FROM THE FABRICATION OF THE 3-DIMENSIONAL TEMPLATE

In order to demonstrate the feasibility of this process, a 300 nm half pitch was first etched into a 6025 fused silica substrate and a micrograph of part of the grating is shown in figure 6. The etch depth into the fused silica is approximately 80 nm. Following the steps illustrated in figure 5, an array of 100 nm posts was exposed in the QSR-5 resist layer and a reactive ion etch step using fluorinated plasma was used to transfer the array onto this grating. The only variation undertaken with respect to the flow illustrated in figure 5 is that a 10 nm metal transfer layer was used between resist and the fused silica surface. Thus the resist pattern was transferred into the Cr layer by etching, and the resulting Cr pattern was used as the etch mask for the fused silica RIE step. A micrograph of the resulting template is shown in figure 7. The same etch recipe was used as for the transfer of the initial grating into the template, so that an etch depth of approximately 80 nm was also obtained for the posts, with a total depth of 160 nm for the deepest trough of the pattern. The final result is a template which includes three height levels on the surface.

There is some residue from the passivation layer still apparent on the sidewalls of the final template. This passivation layer was formed during the initial dry etch step to transfer the array of lines into the template. No residue removal processing was used, therefore this passivation layer acted partly as an etch mask for the second etch process which transferred the via posts into the template. The resulting template was coated with a thin AuPd layer in order to allow for electron beam micrography since the substrate used is electrically insulating. Thus the cracks that are visible on the surface of the pattern in these micrographs are not intrinsic to the pattern but are due to the AuPd layer. Also to be noted that no alignment was used for the electron beam lithography step, thus local alignment of the posts with the underlying grating was achieved simply by using a slightly larger pitch for the array of dots than the pitch for the array of lines first

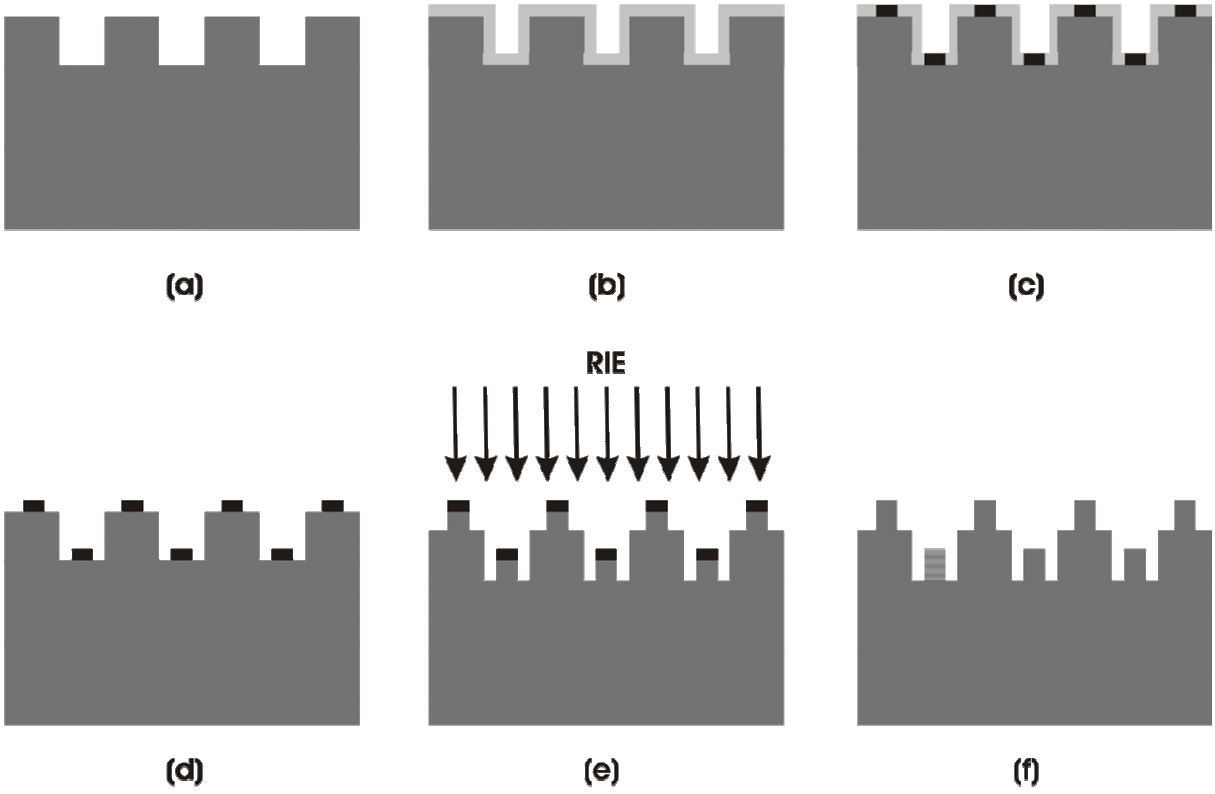


Figure 5 Schematic illustration of the process flow for obtaining a 3D template using QSR-5 conformal resist; a) initial pattern in template; b) deposition by thermal evaporation of QSR-5 resist; c) exposure of resist by electron beam; d) development of pattern; e) reactive ion etching of substrate for pattern transfer; f) finale template after removal of resist.

transferred into the fused silica substrate.

The template was then patterned into a resist layer using the EVG 520 hot embossing system using a temperature of 180ºC and a force of 3000N applied to one quarter of a 3" wafer of silicon. The resist used for the embossing process was 100K molecular weight polystyrene while the template was coated with a silane surfactant as a release layer. The resist thickness was chosen to be much larger than the total template depth in order to avoid any potential damage to the template. The total embossing time was 10 minutes. The results are illustrated in figure 9. It can clearly be seen that both the posts on top of the ridges and at the bottom of the troughs of the array are well imprinted into the polystyrene resist.

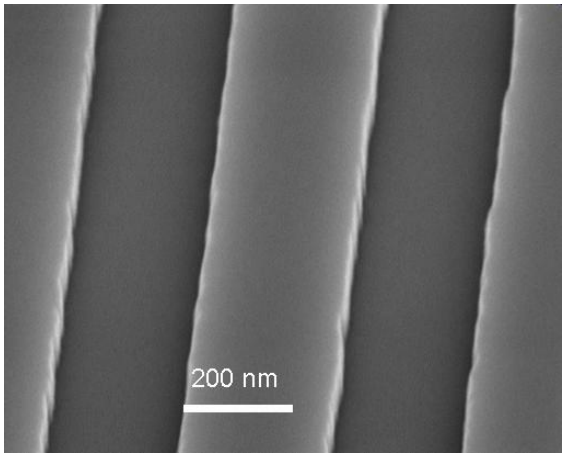


Figure 6 Electron micrograph of 300 nm half pitch array etched 80 nm deep into a 6025 fused silica substrate.

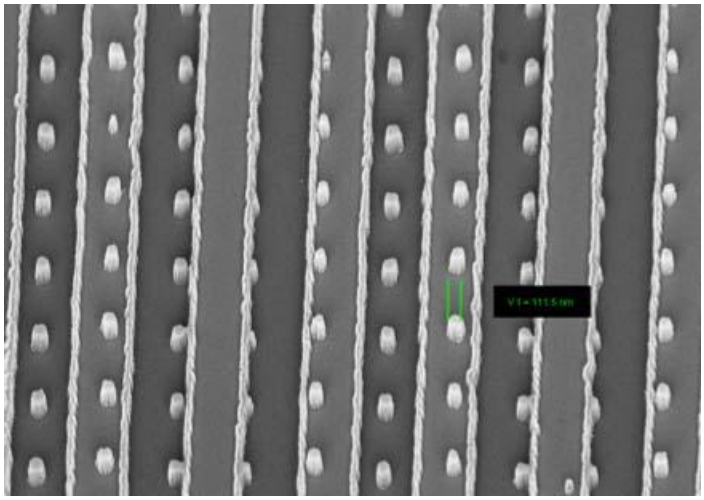


Figure 7 Micrograph of the resulting template with 100 nm via posts formed on top of a 300 nm half pitch grating.

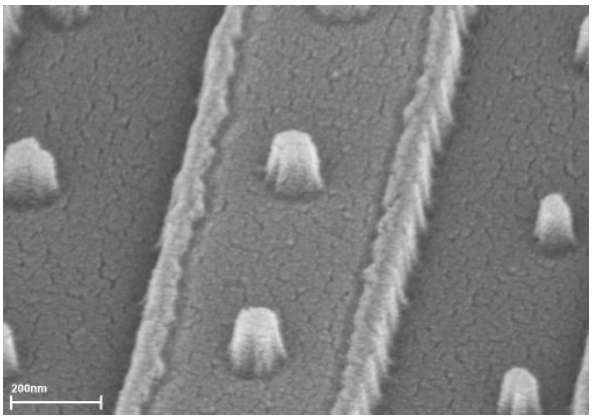
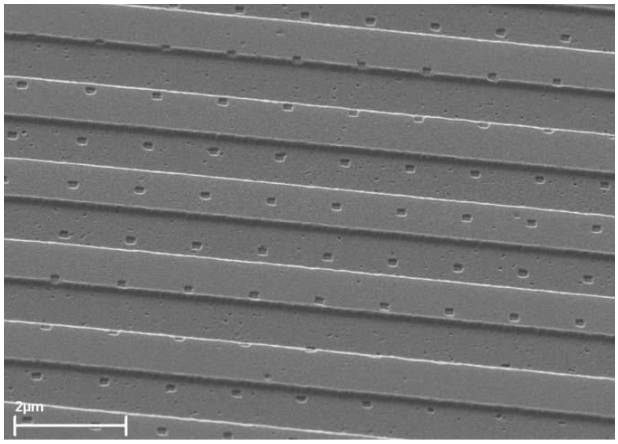
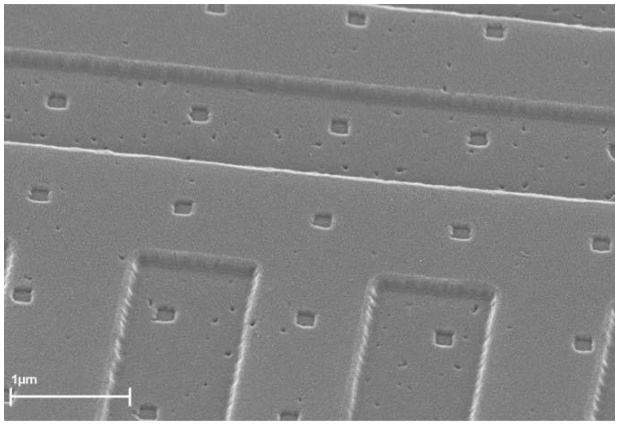


Figure 8 High magnification micrograph of the resulting 2 layer template.



(a)



(b)

Figure 9 Electron micrographs of the resulting of embossing the 3D template into polystyrene resist with a lower (a) and higher (b) magnification view.

Correct pattern transfer has thus been achieved into the resist. While hot embossing was used in this process, a fused

silica substrate was chosen specifically to demonstrate that the method is equally applicable to prepare templates for the UV flash imprint process.

4. CONCLUSIONS

The use of a conformal coating resist, QSR-5, has been demonstrated in the fabrication of a 3-dimensional template consisting in the demonstration case of 3 different height levels on a template. The process described here simplifies the fabrication of such templates by making it possible to pattern directly by electron beam lithography on a non-planar surface. It also opens the way for several different classes of 3-dimensional templates which could not be fabricated with the traditional process that combines two metal layers with wet etch selectivity to be used as an etch mask for the template. It has also been shown that sub-100 nm features can be fabricated with this technique and the method has been fully demonstrated including the hot embossing step using a polystyrene resist. The prototype template is of the same type as could be used for the fabrication a template that could be used for the pattern transfer of an interconnect/via multilayer combination in a single lithography step, which could have tremendous value in significantly reducing the number of steps in the fabrication of state of the art integrated circuits.

5. REFERENCES

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