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Filling of nano-via holes by laser-assisted direct imprint

Bo Cui *, Wei Wu [1], Chris Keimel [2], Stephen Y. Chou *

NanoStructure Laboratory, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544, USA

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Abstract

A new technique for filling narrow and high-aspect ratio nanoscale via holes by laser-assisted direct imprint has been proposed and developed. In the process, the filling material (e.g., metals or Si) is first deposited onto the nano-via holes by a deposition method that has a poor step coverage and hence fills the holes partially with voids. Then a mirror-flat transparent plate (mold) is pressed against the substrate, while an excimer laser pulse (XeCl, 308 nm wavelength, 20 ns pulse duration) shines through the mold. The laser pulse melts the filling material, and the flat mold presses the molten materials into the holes, filling them completely without voids. As examples, we successfully filled a hole array having 100 nm diameter, 500 nm depth (aspect ratio 5) and 200 nm inter-hole spacing (pitch) with e-beam evaporated silicon and copper. Besides superior step coverage and negligible thermal budget, this technique is fast and simple and doesn't need a seed layer. Furthermore, it can planarize the wafer surface in addition to filling the holes. Clearly, this technique could be extended to other materials important for ICs metal interconnect, and may become an alternative to the dual damascene and CVD tungsten plug process used in the current ULSI fabrication.
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Keywords: LADI; Nanoimprint; Pulsed excimer laser; Via filling; Step coverage; Nanofabrication

1. Introduction

Filling via holes or trenches with a deposited material is an important step in IC manufacturing. At present, the metal interconnect for ICs is typically fabricated by the dual damascene and, for the first wiring level, tungsten CVD plug process [1,2], where the via holes and trenches are etched in a dielectric material and subsequently filled up with a metal. Clearly, any voids left in the vias or trenches caused by poor step coverage will create a serious problem for the interconnects.

Though superior to PVD, the step coverage of tungsten CVD is still limited by the low volatility of the precursor gas WF_6 that leads to a low vapor pressure. The result is a mass transport limited deposition rate, and the hole opening receives faster deposition and would be closed before the holes are completely filled. Another disadvantage of CVD is its relatively high thermal budget.

Atomic layer deposition (ALD) can achieve excellent step coverage in certain conditions [3]. It is a modified form of CVD with gas precursors introduced one at a time with pump/purge in between. So the film is deposited one atomic layer per cycle, with a typical deposition rate of order 0.5 nm/min. Not only the slow deposition rate is a manufacturing issue, but also in ALD, voids will be formed if the via holes or trenches have a sidewall with negative angle.

Another candidate for filling future high-aspect ratio vias is chemical fluid deposition (CFD) developed recently [4]. CFD uses supercritical fluids like CO_2 as a carrier for organometallics. As the supercritical fluid CO_2 retains its gas nature and can flow into deep holes, the material deposition rate is limited by chemical reaction rate, giving conformal step coverage. The drawbacks of CFD include high process pressure of order 100 bar and limited choice

* Corresponding authors. Present address: Industrial Materials Institute, National Research Council of Canada, Boucherville, Que., Canada.Tel.: +1 450 641 5231; fax: +1 450 641 5105.
E-mail addresses: bo.cui@nrc.ca (B. Cui), chou@princeton.edu (S.Y. Chou).
[1] Currently with HP Quantum Science Research, Palo Alto, CA, USA.
[2] Currently with GE Global Research, Niskayuna, New York, USA.

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of precursors having high solubility in the supercritical fluid. Moreover, like ALD, voids will be formed when vias or trenches have a negative sidewall angle.

Therefore, there is still a great need for a new method capable of completely filling nano-via holes with high-aspect ratio, regardless of the sidewall angle, and with a high throughput. In this work, we will demonstrate that high-aspect ratio holes can be filled by pressing while melting momentarily the filling material using a pulsed laser, a process similar to laser-assisted direct imprint (LADI) [5] and laser-assisted nanoimprint lithography (LAN) [6].

2. Experiments and results

To demonstrate our method of filling nanoscale via holes by LADI, we fabricated in Si a hole array having 100 nm diameter, 500 nm depth (aspect ratio 5) and 200 nm inter-hole spacing (pitch). The hole array was patterned by nanoimprint lithography and etched by Cl_2/Ar RIE. As silicon is a good heat sink, a 15 nm thermal oxide layer was grown to reduce heat loss to the surrounding bulk Si, and to shrink the hole size at the same time. Finally, 200 nm Si or Cu was deposited on top of the hole array by e-beam evaporation. As expected and shown in Fig. 1, evaporation has very poor step coverage, so the holes were only partially filled, with the sidewall of the holes receiving little deposition before the hole opening was closed.

During the hole filling by LADI, we pressed a UV grade quartz plate with a mirror-flat surface against the substrate coated with the filling material, and vacuumed the sample assembly below 200 mTorr. Then a single excimer laser pulse (XeCl, 308 nm wavelength, 20 ns pulse duration, 2.5×2.5 mm^2 beam size) of fluence 1.1 J/cm^2 melted the filling material momentarily. When in molten state, Si and Cu have very low viscosity (see the following section), so they could flow into the hole and reach the hole bottom within some 100 ns. Fig. 2 shows via filling by Si, indicating a complete filling without voids. For via filling by Cu

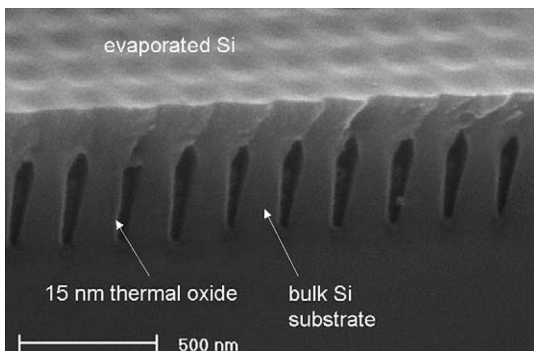

Fig. 1. Holy array with 200 nm period, 100 nm diameter and aspect ratio 5:1 for via filling by LADI, after evaporation of filling material, here 200 nm Si. (15 nm thermal oxide has been grown to reduce heat loss to bulk Si).

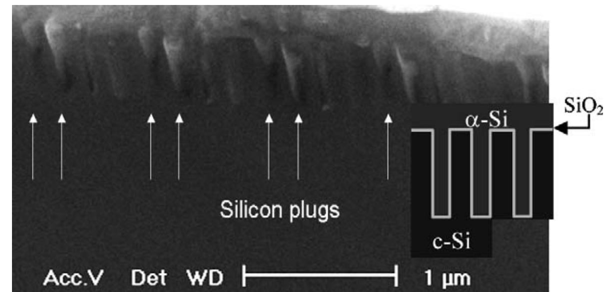

Fig. 2. Laser-assisted via-hole filling by α-Si, showing all holes were completely filled without void. The insert shows the schematic structure. Laser fluence 1.1 J/cm^2.

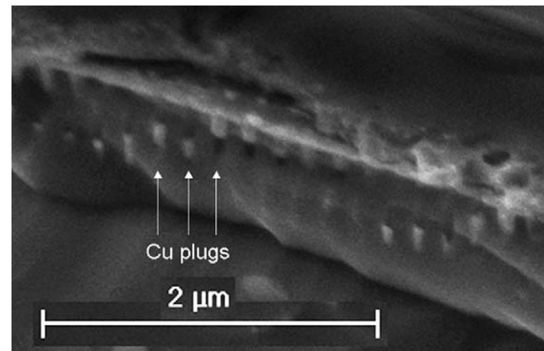

Fig. 3. Laser-assisted via-hole filling by Cu. The Cu plugs were found broken after wafer cut. Laser fluence 1.1 J/cm^2.

(Fig. 3), the Cu plugs were found broken after wafer cut, and it is possible that the built-in stress caused by fast cooling of the liquid Cu has contributed to the Cu plug fracture. Nonetheless, we believe that most holes were completely filled to the bottom, as indicated by the Cu plug sections found on the bottom of the holes.

For both Si and Cu filling, based on the laser fluence and thermal properties of the related materials, the 15 nm SiO_2 and a very thin layer of the surrounding Si at the upper part of the hole should have been melted. However, due to the 8–9 orders higher viscosity of SiO_2 compared to that of the filling material, the flow of the molten SiO_2/Si is negligible, leading to no apparent distortion of the holes, as evidenced by the regular and distinct shape of the Si and Cu plugs with diameter corresponding to the original hole diameter. On the other hand, the 15 nm thermal SiO_2 is much thinner than the characteristic heat diffusion length (see the following section) of 260 nm for SiO_2, leading to significant heat loss to the bulk Si. The via filling would be greatly facilitated in reality when the vias are surrounded by a thick thermal insulator.

During the via filling by LADI, the wafer surface could also get planarized due to the low viscosity of the molten material and the flat surface of the mold. The wafer planarization method, termed as wafer planarization by laser-assisted direct imprint (PLADI), will be discussed elsewhere [7].

Table 1
Thermal–physical parameters of liquid Si and Cu, together with those of H_2O for comparison

	Melting temperature, T_m (K)	Liquid density (g/cm^3)	Thermal conductivity (W/cm K)	Specific heat (J/g K)	Thermal diffusivity (cm^2/s)	Surface tension at T_m (N/m)	Viscosity at 2000 K (10^{-3} Pa s)
Si	1685	2.53	0.17	0.97	0.069	0.775	0.423
Cu	1358	8.0	1.7	0.5	0.425	1.33	1.8
H_2O	273	1.0	0.006	4.2	0.0014	0.074	0.911

Note that the surface tension and viscosity for H_2O are for 25 °C (data adapted from Ref. [8,9]).

3. Discussions

In the via filling process, the driving force is apparently the applied pressure. The counter forces include surface tension, the viscous force and the inertial force. For simplicity, we will discuss them separately.

The minimum applied pressure necessary for squeezing the molten material into the holes is determined by the surface tension and has order of σ/ϕ with σ as surface tension and ϕ as hole diameter. As seen in Table 1, liquid Si and Cu have surface tensions one order higher than that of water, necessitating order of 100 bar for filling holes with 100 nm diameter. In practice, this restriction could be relieved by coating the wall of the holes with a thin lining layer that wets the molten filing material.

The effect of viscous force can be estimated by assuming that a steady flow develops momentarily at $t = 0$ (i.e., ignore inertial force). Then the liquid filling material will travel, before it solidifies, to a critical depth having order of [10]:

$$L_{c1} = \phi\sqrt{\frac{P_{eff}\tau}{\mu}},$$

where P_{eff} is the effective pressure (order of 10 bar) taking into account the surface tension, μ is the viscosity, and τ is the melting duration (~100 ns) at the propagating plug front that depends on the thermal diffusivity D ($=\kappa/\rho\ C_p$, with κ as thermal conductivity, C_p as specific heat and ρ as density [9]) and the laser pulse duration t_p. Thanks to the low viscosity of liquid Cu and Si that is comparable to that of water (Table 1), the theoretical filling depth L_{c1} is calculated to be several μm, one order higher than the hole depth in the experiment.

Similarly, the effect of inertial force, which decides how fast the steady flow develops, can be estimated by assuming an inviscid liquid ($\mu = 0$). The corresponding critical filling depth has order of [10]:

$$L_{c2} = \sqrt{\frac{P_{eff}}{\rho}}\tau.$$

L_{c2} is estimated to be several μm, the same range as L_{c1}. Therefore, both the viscous force and the inertial force are important in determining the overall maximum filling depth.

As for substrate heating, an upper limit of the maximum temperature experienced at the supposed dielectric/semiconductor interface can be estimated as following. We know that for a homogeneous material, the maximum temperature reached at depth equal to its characteristic heat diffusion length δ ($=2\sqrt{Dt_p}$) is roughly 1/5 that of the maximum temperature experienced at the top surface at the end of the laser pulse [9]. Now suppose that the dielectric material below depth δ is replaced by a semiconductor (i.e., assume dielectric thickness equal to δ, or 260 nm for SiO_2) that conducts heat better, then the maximum temperature experienced at the dielectric/semiconductor interface should be <1/5 that of the maximum temperature at the top dielectric surface, or 400 °C if assuming a maximum surface temperature of 2000 °C; and the heating lasts for only order of 10 t_p (=200 ns here). As a consequence, unlike tungsten CVD, the via-hole filling by LADI would have a negligible thermal budget.

Besides superior step coverage and negligible thermal budget, the current technique is fast and simple and doesn't need a seed layer. Its disadvantage, as compared to tungsten CVD, lies in the challenge to scale up due to the likely high pressure required to overcome the surface tension, and the availability of high power pulsed laser having wafer-size power uniformity.

4. Summary

We have demonstrated a novel process capable of completely filling deep high-aspect ratio holes by laser-assisted direct imprint. The holes are 500 nm deep and 100 nm wide, with a spacing of 200 nm between neighboring holes. The filling materials are e-beam evaporated Si and Cu, and the filling time is on the order of 100 ns. Besides Si and Cu, this process could be extended to other materials important to ICs and other nano-devices. Together with trench filling and wafer planarization that can be accomplished simultaneously, the current process could fulfill the needs for ICs metal interconnect that is currently realized by the dual damascene and tungsten CVD process.

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