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Microelectronic Engineering 84 (2007) 1544–1547
MICROELECTRONIC ENGINEERING
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Fabrication of metal nanoring array by nanoimprint lithography (NIL) and reactive ion etching

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Available online 3 February 2007

Abstract

We report a new technique for fabricating metal nanoring array. In the process, a Cr nanodisk array was first formed by evaporating Cr onto the bottom of a 200 nm period hole array having large undercut. The hole array was produced by NIL and RIE pattern transfer in a polymer sandwiched between a thin SiO_2 and Si layer, which were stacked on a second polymer layer; and the undercut was formed by excessive polymer RIE. The thin Si surrounding the Cr disk was subsequently etched through by SF_6 RIE, resulting in a ring-shaped hole structure in Si. After removing SiO_2 and the first polymer layer and etching through the second polymer layer, a metal ring array was created by standard evaporation and liftoff. As examples, we fabricated Cr nanoring array with height 15 nm, inner diameter 70–120 nm and ring-width down to 22 nm. We have found that, for a fixed hole diameter, the ring-diameter is strongly dependent on the hole depth. The ring symmetry and the wafer edge effect are discussed. The process can certainly be extended to metals other than Cr. Compared to previous methods, the current one is simpler, less costly and more suitable for narrow ring fabrication, though it suffers from reduced ring symmetry. However, asymmetric (nonconcentric) nanoring could be desirable for magnetic data storage and plasmonic devices.
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PACS: 81.16.−c

Keywords: Nanoring; Nanocrescent; Nanoimprint lithography; Reactive ion etching; Nanofabrication

1. Introduction

Nanorings have unique magnetic and optical properties and thus have many potential applications. For example, when the ring-width is smaller than the domain wall thickness (order 50 nm in Co), a magnetic nanoring will have a stable flux-closure vortex state with a more reproducible switching than a nanodisk, which is essential for high-density magnetic recording and magnetic random access memory [1,2]. Metallic nanorings also offer tunable optical resonance at longer wavelength than a nanodisk [3] and higher optical transmission efficiency [4].

Various fabrication techniques have been demonstrated for the fabrication of ring-shaped nanostructures. For a single ring as well as a ring array over small area, focused ion beam (FIB) milling or electron beam lithography is preferred due to its high resolution and versatility [5]. The fabrication of nanoring array over large area has been previously demonstrated by nano-sphere (colloidal) lithography [6,7], which is a simple and efficient method but the ring diameter is limited to several hundred nanometers and it lacks long-range ordering that is essential for certain applications (data storage, photonic devices). Another low-cost technique capable of producing sub-100 nm rings over large area is based on templating with porous anodic aluminum oxide (AAO) membranes [8]; yet it lacks long-range ordering and the AAO membrane that supports the ring is fragile. Ring pattern can also be created from a circular structure by the so-called lateral pattern definition or edge-defined technique [9–12], where the ring was defined on the sidewall of a circular pillar or hole pattern. Closely resembling the traditional edge defined technique, nanoring was fabricated recently by capillary force lithography [13,14], templated electrochemical deposition [15], and nanoskiving [16].

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0167-9317/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2007.01.158

Here we report an alternative approach for the fabrication of ordered array of nanorings over large area. It also resembles the traditional edge-defined technique, but rather than depositing a material on the sidewall of the supporting structure, the ring structure is formed around a metal nanodisk by lateral etching during Si RIE with the 'zero-order' etching blocked by the metal disk. The approach includes only NIL, physical vapor deposition (PVD), and dry and wet etch, all of which are low-cost processes. It is suitable for narrow (~20 nm) ring fabrication, as well as for asymmetric ring or nano-crescent structures.

2. Experimental

The process can be divided into two parts: the creation of Cr nanodisk on the bottom of a hole array; and the formation of nanoring surrounding the nanodisk. The NIL mould consists of a 200 nm period and 60 nm diameter pillar array fabricated by two orthogonal NIL steps using a large area grating mould. The substrate for NIL consists of five layers: (1) a 160 nm crossed-linked polymer ARC (anti-reflection coating, Brewer Science XHRiC-16) on Si; (2) 6 nm evaporated Si; (3) a second ARC layer with thickness 50–320 nm; (4) 15 nm evaporated SiO_2; and (5) 200 nm PMMA as NIL resist.

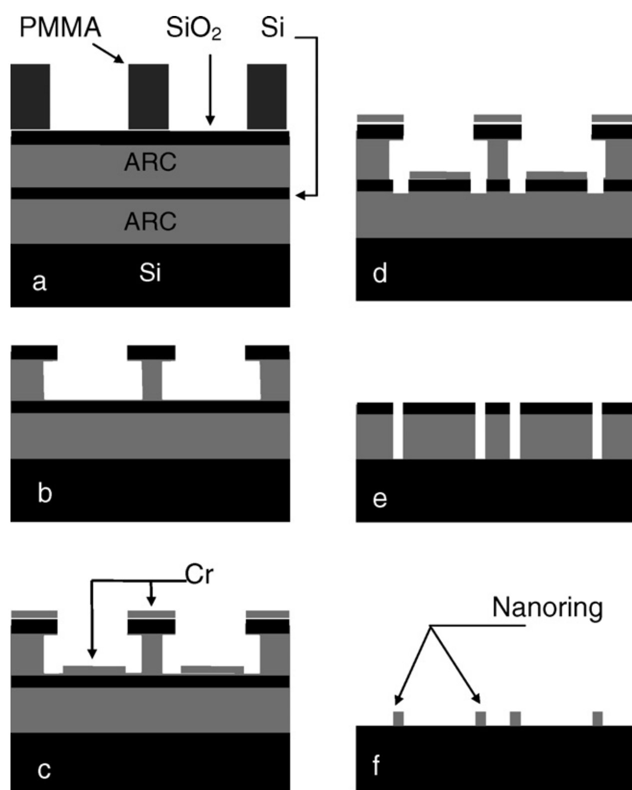

Fig. 1. Schematic representation of the process for metal nanoring fabrication: (a) NIL into PMMA using a pillar array mold; (b) RIE pattern transfer into SiO_2 and then into ARC with over-etch; (c) evaporation of Cr; (d) RIE of the thin Si layer; (e) removal of Cr, SiO_2, ARC, and RIE of ARC; (f) metal evaporation and liftoff.

As shown in Fig. 1, a 60 nm diameter hole array in ARC was first patterned by NIL and RIE pattern transfer. A large undercut was then created by etching ARC with 100 W and 100 mTorr O_2 for 5 min at 150 nm/min, which removed ARC on the bottom Si over area having a diameter about 140 nm. Next, 10 nm Cr was evaporated at normal incidence angle, forming a nanodisk array on the bottom of the hole array. In a subsequent step, Si RIE was carried out using an Oxford Instruments PlasmaLab 80Plus etcher with graphite plate, 20 sccm SF_6 gas, 20 mTorr (default) pressure and 100 W power, which resulted in an etching rate of 200 nm/min and 77 nm/min for Si and ARC, respectively. Due to lateral etch, the thin Si surrounding the Cr nanodisk was etched through. The Cr, SiO_2 and the top ARC layer were subsequently removed by commercial Cr etchant Cr–4S, diluted HF that etched negligible Si, and O_2 RIE, respectively. In a following step, the ring-shaped hole pattern in Si was transferred into the underneath ARC by O_2 RIE, again with over-etch to facilitate the following liftoff. Finally, a metal film was deposited and lifted off by ARC, resulting in a nanoring array on the Si substrate.

3. Results and discussion

We found that the 6 nm Si around the Cr disk lying on the bottom of the holes was etched through only after approximately 40 s RIE, which would etch 133 nm flat Si at 200 nm/min. Anisotropic etching of Si using CF_4/O_2 gas has also been tested, but due to sidewall passivation by fluorocarbon polymer, the 6 nm Si was not etched through even after equivalent 300 nm etching of flat Si.

After liftoff 15 nm Cr, the completed nanoring array with three different sizes is shown in Fig. 2. The different ring widths and diameters were achieved by varying the Si etching time and the ARC spacer height, respectively. It was found that the ring inner diameter strongly depended on the hole depth (equal to ARC height). As can be imagined, for thin ARC (<100 nm), the ring inner diameter is close to the hole diameter of 60 nm. But for thick ARC (>200 nm), the ring inner diameter is considerably larger than the hole diameter because the etching profile in Si is a triangle and its dip may lie far away from the edge of the Cr disk. In the experiment, the hole diameter was fixed at 60 nm. Certainly, the ring diameter could also be tailored by varying the hole diameter.

The etching rate and profile also depend on the gas pressure (fixed at 20 mTorr till now). As shown in Table 1, higher SF_6 pressure leads to higher etching rate and lower bias voltage, which suggests more isotropic and lateral etch. To study the effect of gas pressure on the etching profile in Si, we fabricated Cr disks directly lying on bulk Si by the same process as above but on a substrate without the evaporated Si and bottom ARC layer. We then conducted RIE of Si with pressure ranging from 10 to 100 mTorr. A typical etching profile in bulk Si is shown in Fig. 3. It was found that, for a fixed etching depth of flat Si that

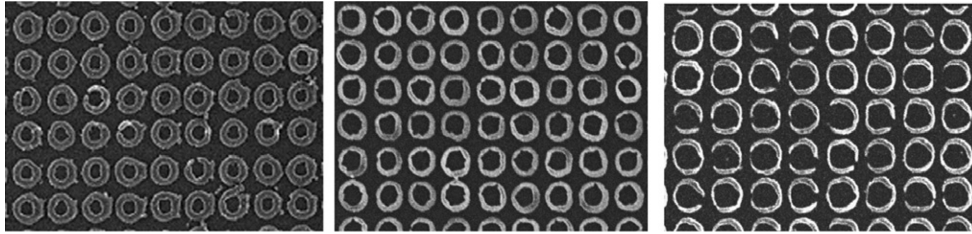

Fig. 2. 200 nm Period Cr nanoring array with inner diameter/width of 70/45 mm (left), 95/30 nm (middle) and 120/22 nm (right), achieved by varying the Si etching time/ARC spacer height at 80 s/100 nm, 80 s/260 nm, and 60 s/320 nm, respectively. (Some sections of the rings are missing for the 22 nm-wide ring due to liftoff.).

Table 1
Si etching rate and bias voltage for different gas pressure

Pressure (mTorr)	10	20	50	100
Rate (nm/min)	150	200	293	467
Bias (V)	330	268	108	28

SF_6 20 sccm, 100 W, graphite plate.

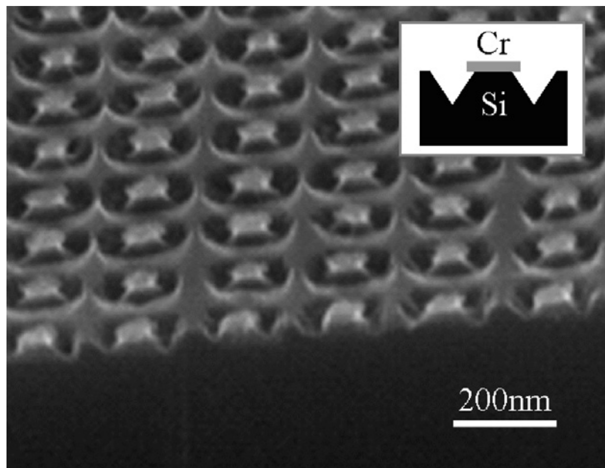

Fig. 3. Etching profile in Si around Cr disks having lied on the bottom of 160 nm deep holes, here RIE with 20 mTorr SF_6 for 80 s at 200 nm/min. The insert shows the schematic profile.

was 267 nm in the experiment, higher pressure led to a wider but shallower triangular profile. Therefore, high pressure would be preferable for wide nanoring fabrication or if the Si film is very thin (say, <5 nm), and vice versa.

Asymmetric nanorings with one side wider than the other (Fig. 4a), or even nano-crescents with one side missing (Fig. 4b) can be fabricated by putting the wafer away from the RIE chamber center. The asymmetry may result from the non-vertical gas flow direction that depends on RIE tool design, gas flow rate and pressure. One simple and efficient way to improve the symmetry is to divide the etching into two steps of equal time with wafer rotation 180° in between. On the other hand, asymmetric nanoring could be desirable for magnetic data storage since it has more controllable magnetic switching than a symmetric one [7], and for plasmonic device since it offers an additional degree to tune the plasmon resonance [17]. As reported earlier [18], metallic nano-crescent could find application in the field of biosensor based on surface enhanced Raman scattering (SERS).

The other major source of asymmetry of the nanorings is the Si wafer edge. In the plasma environment, the wafer is negatively charged and the electric field at the edge is not vertical, leading to slanting incidence of reactive species. This results in very asymmetric nanorings or nano-crescents with its wider side pointing away from the edge. The characteristic length scale within which the edge effect is drastically decreased for a 0.5 mm-thick wafer was ~1 mm. When symmetric rings are desired, the edge effect can be practically eliminated by placing a dummy wafer next to the real wafer.

Asymmetric nanorings or nano-crescents could also be achieved by carrying out the Cr deposition step (Fig. 1c) at an angle other than normal so that the Cr disk lies off the center of the hole bottom.

4. Summary

In this work we developed an approach for the fabrication of a regular metal nanoring array with inner diameter 70–120 nm and ring-width down to 22 nm. Compared to

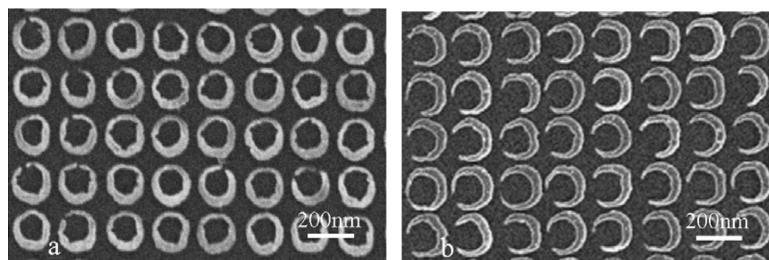

Fig. 4. 200 nm Period array of asymmetric nanoring (a) and nano-crescent (b) in 15 nm Cr.

previous methods, the current one is simpler and less costly as it includes only NIL, PVD, RIE and wet etch.

The method could potentially fabricate nanorings of virtually any material that can be deposited by a method suitable for liftoff, such as evaporation, pulsed laser deposition, or sputtering if the film is thin enough for liftoff.

The area uniformity of the array is limited by the reduced ring symmetry and one approach was proposed to improve the ring symmetry. On the other hand, for many applications asymmetric nanorings or nano-crescents are preferable, which can be readily achieved by the current method.

Like other edge-defined technique, the current one can be extended to other types of structure such as a grating, which would result in a grating with doubled spatial frequency [19,20].

References

[1] S.P. Li, D. Peyrade, M. Natali, A. Lebib, Y. Chen, U. Ebels, L.D. Buda, K. Ounadjela, Phys. Rev. Lett. 86 (2001) 1102.
[2] J.G. Zhu, Y. Zheng, G.A. Prinz, J. Appl. Phys. 87 (2000) 6668.
[3] J. Aizpurua, P. Hanarp, D.S. Sutherland, M. Kall, G.W. Bryant, F.J. Garcia de Abaho, Phys. Rev. Lett. 90 (2003) 057401.
[4] F.I. Baida, D.V. Labeke, B. Guizal, Appl. Opt. 42 (2003) 6811.
[5] A. Perentes, I. Utke, B. Dwir, M. Leutenegger, T. Lasser, P. Hoffman, F. Baida, M.P. Bernal, M. Russey, J. Slavi, D. Van Labeke, Nanotechnology 16 (2005) S273–S277.
[6] D. Jia, A. Goonewardene, Appl. Phys. Lett. 88 (2006) 053105.
[7] F.Q. Zhu, G.W. Chern, O. Tchernyshyov, X.C. Zhu, J.G. Zhu, C.L. Chien, Phys. Rev. Lett. 96 (2006) 027205.
[8] S. Wang, G.J. Yu, J.L. Gong, Q.T. Li, H.J. Xu, D.Z. Zhu, Z.Y. Zhu, Nanotechnology 17 (2006) 1594–1598.
[9] D.C. Flanders, N.N. Efremow, J. Vac. Sci. Technol. B 1 (1983) 1105.
[10] P.B. Grabiec, M. Zaborowski, K. Domanski, T. Gotszalk, I.W. Rangelow, Microelectron. Eng. 73–74 (2004) 599–603.
[11] S.F. Bai, S.Y. Chou, in: The 50th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication (Eipbn'06), Baltimore, MD, 2006.
[12] R. Ji, M. Knez, T. Xie, A. Frommfeld, P. Werner, U. Gosele, K. Nielsch, Micro- and Nano-Engineering, Barcelona, Spain, 2006.
[13] S. Kim, J.R. Jeong, S.H. Kim, S.C. Shin, S.M. Yang, J. Appl. Phys. 99 (2006) 08G310.
[14] S. Kim, J.M. Jung, D.G. Choi, H.T. Jung, S.M. Yang, Langmuir 22 (2006) 7109–7112.
[15] R. Ji, W. Li, R. Scholz, U. Gosele, K. Nielsch, Adv. Mater. 18 (2006) 2593–2596.
[16] Q. Xu, R. Perez-Castillejos, Z. Li, G.M. Whitesides, Nanoletter 6 (9) (2006) 2163–2165.
[17] Y. Wu, P. Nordlander, J. Chem. Phys. 125 (2006) 124708.
[18] G.L. Liu, Y. Lu, J. Kim, J.C. Doll, L.P. Lee, Adv. Mater. 17 (2005) 2683–2688.
[19] Z. Yu, W. Wu, L. Chen, S.Y. Chou, J. Vac. Sci. Technol. B 19 (2001) 2816.
[20] B. Cui, Z. Yu, G. Ge, S.Y. Chou, Appl. Phys. Lett. 90 (2007) 043118.