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Charging effect reduction in electron beam lithography with nA beam current

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ABSTRACT

Charging effect becomes a more serious issue when performing electron beam lithography using high beam current. Here we studied the charging effect using PMMA, PMGI and ZEP-520A resist to pattern 200 nm period hole array. It is found that charging effect can be reduced by simply re-arranging the exposure sequence such that subsequent writing elements are farther apart. It can also be decreased by using a more conductive substrate. Among the three resists, the charging effect is the least for the insensitive PMGI resist, though at the cost of longer writing time when using the same beam current. The opposite is true for the more sensitive ZEP-520A resist.

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1. Introduction

Electron beam lithography (EBL) [1], focused ion beam (FIB) [2] lithography and nanoimprint lithography (NIL) [3] are currently the three most widely employed nanolithography techniques. Among them, EBL is undoubtedly the most popular for R&D. In recent years, there are two main trends in EBL development. One is the effort towards ultra-high resolution and pattern density, with the record pattern density of 9 nm period line arrays using HSQ resist and salty development [4]; the other is towards writing over large area with acceptable throughput needed for, e.g., the fabrication of NIL mold for bit-patterned recording media [5], and with the advancement of EBL tool and resist development, it is now possible to create nano-patterns over an entire wafer. For high resolution features (sub-50 nm), low beam current (sub-100 pA) is usually used when writing time is not a concern. Otherwise, one has to use large beam current typically in the nA range.

Besides decreased depth of focus, other issues for high current EBL include substrate heating and charging effect that happens when the conductivity of the substrate is not ideal. During exposure, electrons are injected into the resist and substrate; and the deposited charge can deflect the incoming electrons, resulting in pattern distortion and positioning error. To overcome this problem, the most widely used anti-charging method is to coat the resist with a metal or conducting polymer layer [6] to dissipate the charge. Similar to variable pressure scanning electron microscopy (SEM), variable pressure EBL [7] has demonstrated capability of conducting EBL on insulating substrate since the negatively-charged electrons can be balanced by the positive ions created by the electron–gas molecule collision; yet the resolution may suffer from the electron scattering by the gas molecules. Critical energy EBL [8], which makes use of the fact that, at certain electron energy, the number of ejected electrons (secondary and backscattered) is equal to the injected primary electrons, can also suppress the charging effect; yet only moderate resolution was demonstrated partly because of the very low critical energy (only 1.3 kV for 65 nm-thick PMMA on glass) that also requires very thin resist. Another method to reduce the charging effect is to carry out the EBL on a thin electron-transparent membrane that traps only a small percentage of the electrons (the back-scattered electrons are also greatly reduced, leading to significantly less proximity effect [9,10]). In this paper, we will show that charging effect can also be reduced by optimizing the exposure sequence and/or using more conductive substrate like a heavily doped Si wafer.

2. Discussion of charging effect

During e-beam exposure, electrons are deposited into the top conducting layer (if coated), the resist and the substrate, and trapped there if the material is insulating. For conducting or semiconducting materials, the charge will dissipate; or the surrounding free carriers will move toward (for p-type semiconductors) or away from (for n-type or metals) the deposited charge, which leads to "screening" of the deposited charge. The charging effect can never be completely eliminated by a top conducting layer, because at equilibrium the screening effect of any point charge is equivalent to the creation of a dipole between the point charge and its mirror charge above the metal layer. Though the dipole field decays faster than the electric field from a point charge ($1/r^3$ vs. $1/r^2$, r being the distance from the point charge or dipole), it can still deflect the incoming electrons and cause pattern distortion. Therefore, charging effect can only be totally eliminated by charge dissipation. Nonetheless, charging effect will still be considerable if

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the characteristic charge screening/dissipation time is comparable to or longer than the exposure time for one element, or the time interval between subsequent elements. In addition, it is expected that the pattern distortion due to deposited charge during the exposure of the same element is less than the deposited charge during the exposure of previous element, because for the former case the electric field (from deposited charge) above the element being exposed is roughly normal to the surface with minimal lateral component that deflects the incoming electrons. For the latter case, apparently the farther away between subsequent exposure elements, the smaller electric field from deposited charge, and thus the less pattern distortion due to charging effect.

Based on the above qualitative analysis, we anticipate that charging effect can be reduced by re-arranging the exposure sequence such that the subsequent writing elements are farther apart, and/or by using more conductive substrates that dissipate/screen the deposited charge faster.

3. Experiment

Two-dimensional periodic structures are the building blocks for photonic crystals, bit-patterned magnetic recording media, etc., so we limit our study to the exposure of 200 nm period dot array. EBL is carried out using Raith 150^{TWO} system with 30 kV acceleration voltage and 60 μm beam aperture that leads to a beam current of 1.2–1.5 nA. The periodic dot arrays were exposed using four different pattern designs, as shown in Fig. 1: (a) a large 100 μm square with the exposure step size set to 200 nm in both *x*- and *y*-direction (we name it (1 0 0) lattice); (b) parallel horizontal lines with offset of $100 \times \sqrt{2}$ nm at the beginning, step size $200 \times \sqrt{2}$ nm, and spacing between two adjacent lines $200/\sqrt{2}$ nm ((1 1 0) lattice); (c) same as (b) but replacing $\sqrt{2}$ with $\sqrt{5}$ ((1 2 0) lattice); (d) periodic dot array, which leads to a very large CAD file (we name it dot array). The areal, line and dot doses are set such that the exposure dose for each dot is the same: 12 fC/dot for poly(-methyl methacrylate) (PMMA). All the four designs will result in the same pattern, except that the array is rotated by 45° for (b), and $\tan^{-1}(1/2) = 26.6°$ for (c). However, the total writing time that includes both dwelling time and setting time (the "pause" before exposing each element, 0 for (a–c), finite for (d)) is much longer for (d) than for (a–c).

For some resist films, 20 nm Cr was coated by e-beam evaporation, which was removed before development by wet etching using an etchant containing a mixture of 120 g ceric ammonium nitrate ($Ce(NH_4)_2(NO_3)_6$), 100 ml acetic acid (CH_3COOH) and 500 ml deionized water for 3 min.

4. Results and discussion

We first demonstrated that charging effect is significant even for a heavily doped Si substrate with low resistivity, and the pattern distortion due to charging effect can be greatly reduced simply by re-arranging the exposure sequence. Fig. 2 shows the SEM images of 200 nm period hole array in 100 nm thick PMMA developed using methyl isobutyl ketone (MIBK): 2-propanol (IPA) = 1:3 for 30 s. The substrate is a heavily Sb doped n-type silicon with a resistivity of 0.01–0.02 Ω cm. Because of charging effect, it was found that the holes were noticeably elongated along the beam scanning (horizontal) direction. The direction of elongation is consistent with the direction of electrostatic force between deposited electrons during the exposure of previous hole and incoming electrons. The elongation is highest (average hole-width 86 nm) for the "(1 0 0) lattice" pattern design, followed by the "(1 1 0) lattice" pattern design (hole-width 68 nm), and the lowest (hole-width 53 nm) for the "(1 2 0) lattice" pattern design. The pattern elongation (hole-width 60 nm) exposed using the "dot array" pattern design is also much lower than that for the "(1 0 0) lattice" pattern design, which is because of the longer charge dissipation time. However, this means longer writing time (28 μs per dot, including dwelling time 8.2 μs and setting time 19.8 μs) when using "dot array" pattern design, as compared to that for the "(1 0 0) lattice" pattern design (8.2 μs per dot for beam current 1.46 nA).

To study the influence of substrate conductivity on charging effect, we performed electron beam lithography on a lightly doped Si and insulating quartz substrate having lower charge dissipation/screening rate. For the "(1 0 0) lattice" pattern design as shown in Fig. 3a that used lightly doped n-type wafer with relatively high resistivity of 1–10 Ω cm, the pattern distortion and positioning error is much more severe than that shown in Fig. 2a that used a low-resistivity wafer. As expected, the hole array is better defined for the "(1 1 0) lattice" pattern design as shown in Fig. 3b. For quartz substrate, even when coated with 20 nm Cr layer on the resist, the hole array is not defined for the "(1 0 0) lattice" and "(1 1 0) lattice" pattern design (not shown), and very poorly defined for the "(1 2 0) lattice" pattern design (Fig. 3c). The "traces" that link the holes along the horizontal direction due to partial development when under-exposed are clearly seen. Here we want to mention that the traces are not because of exposure by the un-blanked beam between exposing two adjacent holes, since the patterning speed of the tool is 20 MHz, indicating only order 0.05 μs transfer time. The hole array is reasonably well-defined for the "dot array" pattern design (Fig. 3d), implying that the characteristic charge screening time through the Cr layer is of the same order as the writing time of each hole (28 μs, including dwelling and setting time). We can also conclude that, for the current experimental parameters, the charge dissipation through the lightly doped substrate is more efficient than charge screening through the Cr layer.

Besides PMMA, we also studied poly(dimethyl glutarimide) (PMGI, MicroChem Corp.) resist that is ~4× less sensitive than PMMA when using the same developer (MIBK:IPA) as PMMA [11], and ZEP-520A that is ~5× more sensitive than PMMA when using n-amyl acetate developer for 1 min. As shown in Fig. 4a for

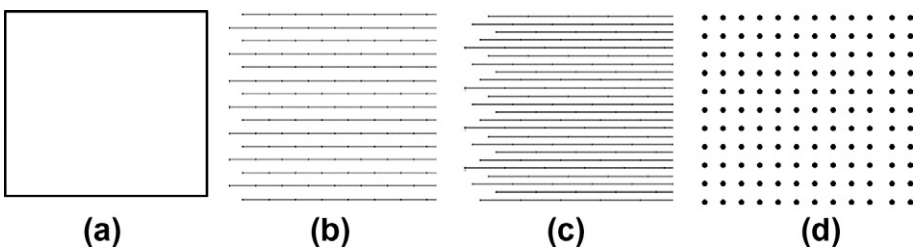

Fig. 1. The four different pattern designs that all give 200 nm period dot array. (a) Large square where array periodicity is defined by the exposure step size along the *x*- and *y*-direction; (b) line array with offset at the beginning, where the "nodes" on each line indicate the position of exposed dots. The resulted 200 nm period dot array is rotated by 45°; (c) similar to (b) but the step size and line-spacing is set such that the resulted 200 nm period dot array is rotated by 26.6° and (d) dot array with 200 nm period along both directions.

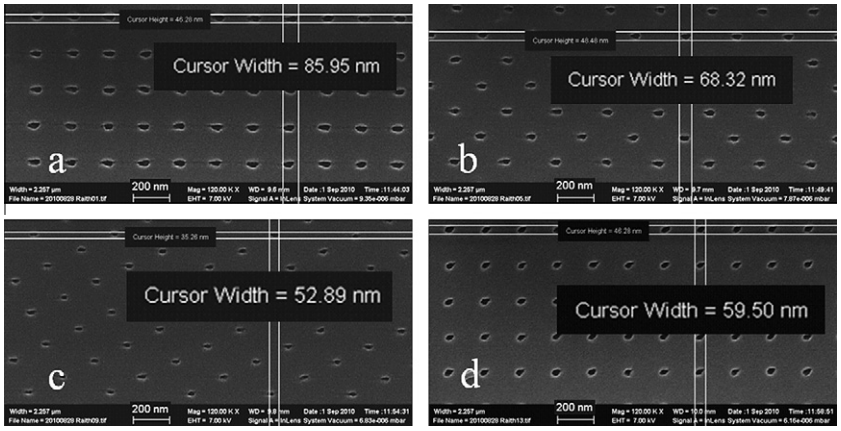

Fig. 2. Hole array with 200 nm period developed in PMMA coated on a heavily doped n-type Si substrate with resistivity 0.01–0.02 Ω cm, (a–d) are exposed using the pattern design as shown in Fig. 1a–d, respectively.

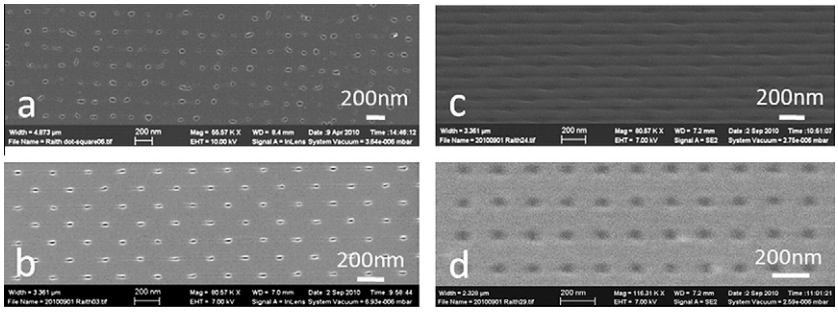

Fig. 3. Hole array with 200 nm period developed in PMMA coated on: (a and b) a lightly doped n-type Si substrate with resistivity 1–10 Ω cm, exposed using the pattern design as shown in Fig. 1a and b, respectively; (c–d) a quartz substrate with 20 nm Cr conductive layer coated on the resist, exposed using the pattern design as shown in Fig. 1c and d, respectively.

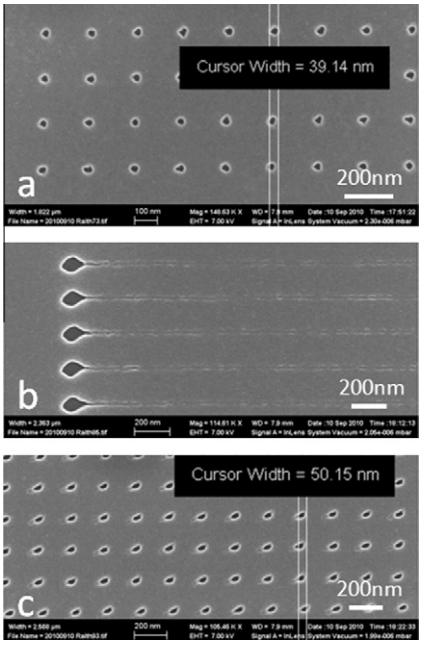

Fig. 4. Hole array with 200 nm period. (a) Developed in PMGI resist using pattern design as shown in Fig. 1a; (b and c) developed in ZEP-520A resist using pattern design as shown in Fig. 1a and d, respectively. The exposure doses are 48 fC/dot for PMGI, and 2.4 fC/dot for ZEP-520A.

PMGI resist, contrary to general intuition, it is found that the charging effect is negligible even for "(1 0 0) lattice" pattern design and high-resistivity wafer. This is because, even though the deposited charge is significantly higher than that for PMMA resist, the charge dissipation/screening time is also higher by the same amount; and as the resist is less sensitive, the exposure due to deflected electrons will not result in noticeable development. However, for the same beam current, the writing time is longer when using less sensitive resists. The exactly opposite situation is true for ZEP-520A resist, where the hole array is not well defined for the "(1 0 0) lattice" pattern design (except for the first hole along each writing line, see Fig. 4b), though the array is clearly defined for the "dot array" pattern design due to the long setting time (Fig. 4c).

5. Conclusion

Because of the insufficient time for charge dissipation and screening, charging effect becomes a more serious issue when performing electron beam lithography using high beam current. Here we studied the charging effect using PMMA, PMGI and ZEP-520A resist to pattern 200 nm period hole array. It is found that charging effect can be reduced by simply re-arranging the exposure sequence such that subsequent writing elements are farther apart. Though greatly reduced, the charging effect is still significant for relatively conductive substrate such as a heavily doped Si wafer. Among the three resists, the charging effect is the least for the insensitive PMGI resist, though at the cost of longer writing time when using the same beam current.

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