Evaluation of STI degradation using temperature dependence of leakage current in parasitic STI MOSFET

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Abstract

Shallow trench isolation (STI) has become the most promising isolation scheme for ULSI applications. However, the trench isolation suffers from dislocations and oxidation induced stacking faults. Such faults are typically located near trench edges. These STI faults increase the junction leakage current and may turn-on the parasitic STI MOSFET resulting in significant leakage current through the trench isolation. In this paper we analyze the mechanism of parasitic STI MOSFET formation and investigate the temperature dependence of its leakage current. Simulation results show that the value of drain current of parasitic STI MOSFET can be used for evaluation of STI degradation. The abnormal temperature dependence of the parasitic drain current with floating body can be used as a faulty STI indicator.

1. Introduction

Shallow trench isolation (STI) has been developed for providing isolation in sub-quarter micron CMOS technologies. The basic advantage of STI is a 2-5X reduction in the minimum device separation compared to the LOCOS-based isolation techniques. There are two major issues, which are typically considered when STI is used. The first issue is the additional process complexity of STI realization and its impact on *pn* junction leakage. The realization of STI inherently causes large mechanical stress in the substrate. These stresses result in the defects. Such defects include dislocations and oxidation induced stalking faults. In recent studies, abnormally large leakage current through the *pn* junction was observed due to the presence of STI dislocations within the depletion region of the junction [1,2]. The second issue deals with the realization of parasitic MOSFET due to the inversion of trench sidewalls. These sidewalls cannot be doped with channel stop implant in a standard field implant process. Therefore, a special angled field implantation is used to dope the trench sidewalls [3]. Despite the higher integration capability, trench isolation presents a serious problem due to leakage currents in pn junctions and parasitic lateral and vertical MOSFETs [4]. This problem becomes more critical with technology scaling, because the trench width is scaled to 0.15 - 0.25 um for 0.1 um CMOS technology [5]. Hence, the risk of turn on the lateral parasitic STI MOSFET is increased with scaling. In this paper, we present the simulation results on the temperature dependence of STI leakage current. This current can be used for evaluation of the STI degradation. The abnormal temperature dependence of the leakage current in parasitic STI MOSFET can be utilized for defects identification in trench isolation.

The paper is organized as follows. In Section 2, we present the typical process flow for STI formation and discuss the critical steps related to the origin of

leakage current in STI. The impact of STI degradation on junction current is considered in Section 3. The test structure for evaluation of STI degradation is analyzed in Section 4. The simulation results of temperature dependence of leakage current in parasitic STI MOSFET are presented and discussed in Section 5. The paper is concluded in Section 6.

2. Typical STI Process Flow and Defects

A simplified STI process includes following basic steps:
(i) Thermal growth of pad oxide and silicon nitride deposition.
(ii) Photo-resist pattering, reactive-ion-etching (RIE) of shallow trenches.
(iii) Deposition of boron diffusion source (p+ poly or BSG) or boron angled channel stop field implant.
(iv) Thermal cycling between 800 °C and 900 °C to drive the boron into the bottom and the sidewalls of trenches and removal of boron diffusion source.
(v) Trench filling with CVD oxide and densification annealing.
(vi) Chemical-mechanical polishing (CMP) for STI planarization.

An application of RIE process for the formation of (ii) often results in RIE-induced damages at the STI sidewalls and bottom. Typically, such damages are located within 10 nm thickness of STI boundary [6]. The surface defect density may reach ~2 x 10^{10} cm^{-2}. These defects generate the oxidation induced stacking faults (OSF) in the subsequent steps of above mentioned STI process flow [6]. Moreover, STI formation also results in dislocations [2]. These dislocations are caused by factors such as crystal defects. Crystal defects are primarily caused by ion implantation, mechanical stresses at STI-Si interface, CMP, and thermal annealing. These two categories of defects are the main reasons for STI degradation. In [7] it was reported that the interface-trapped charge density (D_{it}) in trench sidewalls may reach ~5 - 8 x 10^{11} cm^{-2} in annealed samples carried out for 15 min at 450 °C. It is believe that the high D_{it} is caused by STI dislocations. These interface-trapped charges can significantly increase the perimeter component of STI-junction leakage current due to larger surface generation-recombination rate. There are evidences that the oxidation induced stacking faults may also increase the interface-trapped charge density at the Si-SiO_2 interface of STI [8]. The higher D_{it} concentration in STI increases the *pn* junction leakage current in MOSFETs and as a consequence the lateral parasitic MOSFETs may turn on. This problem is especially important for deep submicron CMOS technologies when STI width is scaled to 0.1 - 0.15 um. In case of improperly passivated trench sidewalls (channel stop doping), the very high D_{it} may create the inversion channel and activate the parasitic lateral MOSFETs. This is an STI degradation mechanism and its temperature dependence is analyzed below.

3. Leakage Current in Parasitic STI MOSFET

The twin well CMOS technology is widely used for advanced memory and logic circuits. Fig. 1 shows the analyzed STI structure. In this case, STI is used as the isolation between two n-MOSFETs (T1 and T2), that are formed in the same well. Such a transistor organization is often used in SRAM and DRAM circuits. The device structure in Fig. 1 may be identified as a lateral parasitic STI MOSFET, which can provide the significant leakage current across STI region when sidewall guard p - doping cannot properly suppress the inversion cannel formation due to impact of STI interface-trapped charges.

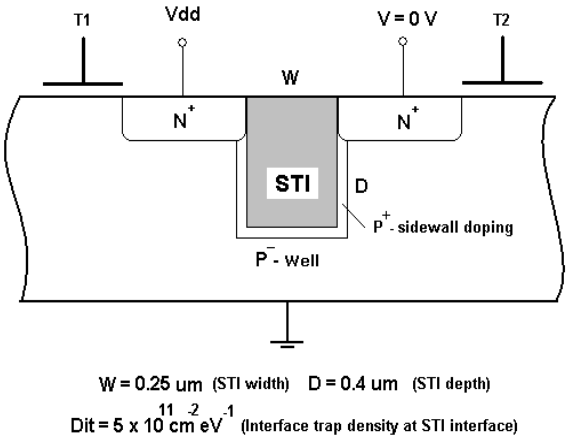

Fig. 1. Cross-section of STI between two n-MOSFETs (T1 and T2).

In order to simulate the behavior of the parasitic STI MOSFET, we used a 2-D device simulator "MicroTec" [9]. The basic technology and geometric parameters of active regions (source (S) and drain (D)) and STI,

which were used for simulations, are given in Table 1. The simulated I_DV_D characteristics of parasitic STI n-MOSFET is shown in Fig. 2. The substrate terminal of STI structure is grounded and temperature is maintained at 300 K. The D_{it} concentration at the STI interface is kept at $5x10^{11}$ cm^{-2}. As it mentioned before, this level of trap charge density may exist in defective STI structures. At V_{DD} = 2.5 V the leakage current of parasitic transistor is approximately 0.32 nA/um. For comparison, the nominal weak inversion leakage current of conventional n-MOSFET, implemented in 0.25 um CMOS technology is around 5.5 pA/um at the same temperature and V_{DD}. Therefore, STI leakage per unit dimension under these conditions may be extremely large (58x) compared to the leakage current. To suppress the action of parasitic STI MOSFET, the sidewall doping should be further increased to ~2 x 10^{18} cm^{-3}.

Table 1.
Technology and geometric parameters of STI structure

Parameter	Value
S/D depth	0.15 um
S/D length	0.5 um
S/D doping	2 x 10^{20} cm^{-3}
Parasitic MOSFET width	5 um
P^+ sidewall doping	8 x 10^{17} cm^{-3}
P^- well doping	5 x 10^{16} cm^{-3}

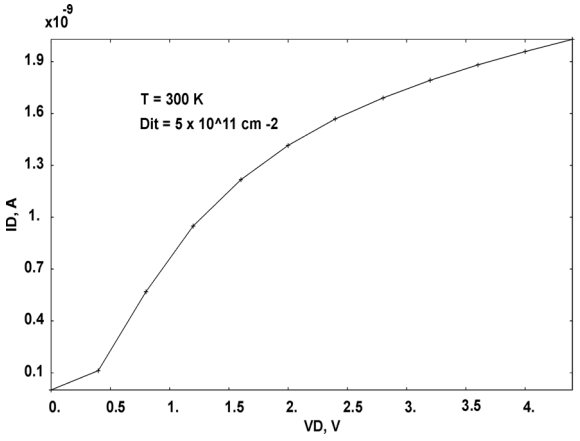

Fig. 2. I_D vs. V_D characteristic of lateral parasitic STI n-MOSFET.

4. Test Structure of Parasitic STI MOSFET for Evaluation of STI Degradation

The quality of LOCOS based dielectric isolation in SRAM cells may be tested using a special cell isolation technique and a signature analysis method proposed in [10]. This technique consists of physical and electrical isolation of analyzed memory cells. The purpose of physical isolation is to separate the analyzed SRAM cell from the array cells. The electrical isolation electrically separates the n-channel and p-channel transistors in the isolated SRAM cell. The physical isolation is performed by cutting the bit/word lines and VDD/Ground lines through focused ion beam (FIB) technique. For electrical isolation, probing is performed with bias voltage applied to the probe pins. Moreover, FIB is also used for metal deposition in order to create probe pads. This procedure allowed researchers to examine each transistor separately for weak inversion leakage and also pair of transistors for LOCOS leakage. The same approach can be applied for STI quality testing.

The test structure and voltage biasing, which were used in our simulations, are shown in Fig. 3. The difference of parasitic STI MOSFET in Fig. 3 in comparison with the parasitic STI MOSFET in Fig. 1 is the floating potential of body terminal. Note, that we assume the dual well CMOS process, when all n-MOSFETs are implemented in P-well and all p-MOSFETs are implemented in N-well.

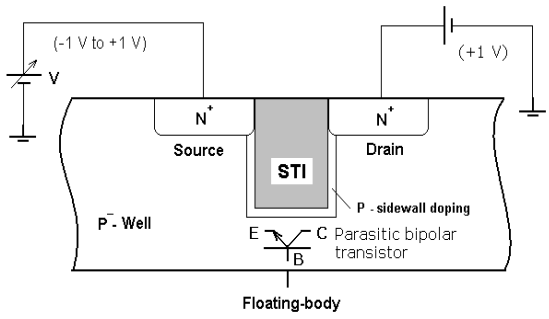

Fig. 3. Equivalent circuit and bias voltages for STI leakage current simulations.

When we apply the negative voltage (from -1 V to 0 V) or forward bias to source, the drain current indicates the collector current of the parasitic transistor with a floating base terminal. The value of STI degradation is defined by the drain current at V_S = 0 V. In the defect free case, the leakage current through the STI is

expected to be approximately in pA/um range. We simulated the parasitic STI MOS transistor with floating body (see Fig. 3) at room temperature and the different interface trap densities at the STI surface. The obtained results are presented in Fig. 4. These curves show the presence of kink effect, which is typical for partially depleted SOI transistors. This can be attributed by the turning on of parasitic bipolar transistor in a floating body configuration. To prove this assumption, we simulated the same parasitic STI transistor at different temperature, because kink effect should be increased with temperature reduction [11]. The obtained results show the increase of curve bending at temperature reduction (see Fig. 5).

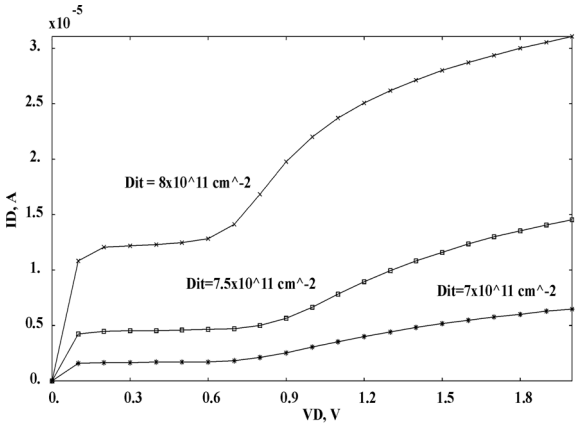

Fig. 4. I_D vs. V_D curve of parasitic STI transistor with floating body at different interface trap densities (T=300 K).

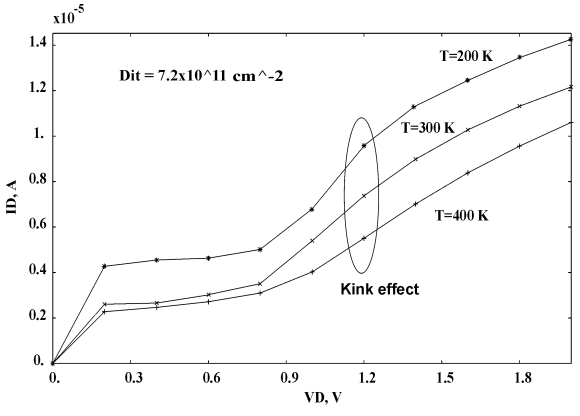

Fig. 5. Temperature dependence of kink effect in parasitic STI transistor with floating body.

The observed thermal behaviour of drain current of parasitic STI transistor with floating body is identical with the thermal behaviour of drain current of partially depleted (PD) SOI transistors [12,13].

5. Temperature dependence of leakage current of parasitic STI MOSFET

Most of leakage current mechanisms in defective and defect free CMOS ICs are diminished with temperature reduction. Hence, the abnormal temperature dependence of leakage current can be used as an indicator of specified degradation mechanism in the chip.

The simulated values of leakage current (I_{off}) of parasitic STI MOSFET versus temperature are plotted in Fig. 6.

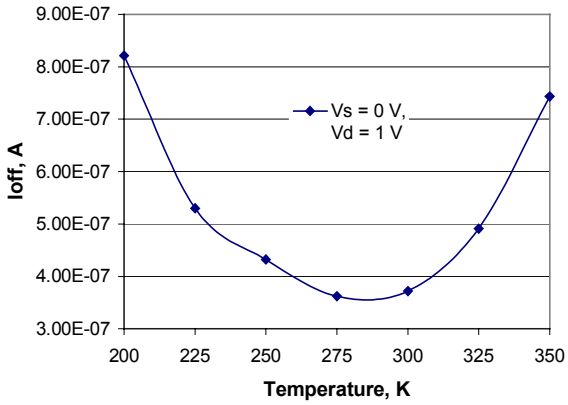

Fig. 6. Leakage current of parasitic STI transistor with floating body and D_{it} = 6.5 x 10^{11} cm^{-2} vs. temperature.

From this graph we can conclude that the I_{off} is reduced with temperature lowering from 350 K to 280 K. In this temperature range, the leakage current is controlled by the channel leakage current of MOS transistor, which is exponentially reduced with temperature. However, starting from 275 K and below the leakage current is increased, since it is controlled by the parasitic BJT device. This can be explained by the fact that the floating body potential ($V_{bulk\text{-}source}$) (Eq. 1) is increased with temperature lowering [12] and it is triggered the parasitic BJT device. Thus, the leakage current of parasitic STI transistor is increased below a certain temperature. The same temperature dependence of

leakage current was observed in PD SOI transistors [13].

$$V_{bulk-source} \approx \frac{m(1+\alpha)}{1+\alpha-m\alpha}\left[\psi_S(T) + \frac{kT}{q}\ln\left(C(M-1)\frac{n^{m-1}(T)n^{3-m}(T_0)}{I_{R0}(T_0)}\right)\right] \quad (1)$$

where m, α, C, M, n are empirical constants, ψ_S is the surface potential, and I_{R0} is the recombination current coefficient [12]. Note, that the high values of leakage current in Fig. 6 are explained by the high charge trap density at STI edge. The abnormal dependence of leakage current in STI structure on the temperature reduction may be used as a reliable indicator of defective STI.

6. Conclusion

In this paper, the temperature dependence of leakage current in parasitic STI MOSFET was investigated. The following conclusions were obtained:

1) The presence of high charge trap density at STI edge results in the inversion channel formation and the activation of parasitic STI MOSFET. The value of drain current of parasitic STI MOSFET can be used for evaluation of STI degradation.

2) It was found that the analyzed STI MOSFET with floating body shows the kink effect, which increases with temperature lowering and charge trap density increase. The observed thermal behaviour of parasitic STI MOSFET with a floating body is similar with the thermal behavior of PD SOI MOSFET.

3) The temperature lowering from 350 K to 280 K results in the leakage current decrease in STI MOSFET with floating body. In this temperature range, the leakage current is controlled by the channel leakage current of parasitic MOS transistor. In the temperature range from 275 K and below, the leakage current is increased. This leakage current in STI MOSFET is controlled by the parasitic lateral BJT device.

4) The abnormal behavior of leakage current in STI structure with the temperature reduction may be used as a reliable indicator of defective STI.

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