E&CE 327 Final

2010t1 (Winter)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the **formulas** you use and **all of your work**.
- The proctors and instructors will **not answer questions**, except in cases where an error on the exam is suspected. If you are confused about a question, write down your **assumptions or interpretation**.
- Justifications of answers will be marked according to **correctness, clarity, and concision**.

			Total Marks	**Approx. Time**	**Page**
Q0	!!Almost Free!!		1	0	3
Q1	Pipelining		17	15	4
Q2	Functional Verification		17	20	5
Q3	Latch Analysis		16	15	8
Q4	Elmore Delay		16	25	9
Q5	Clock Gating		17	25	11
Q6	Testing		17	25	12
Totals			100	125	

Name:_____

UWUserid:_____

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A} \times \mathsf{C} \times \mathsf{V}^2 \times \mathsf{F}) + (\tau \times \mathsf{A} \times \mathsf{V} \times \mathsf{ISh} \times \mathsf{F}) + (\mathsf{V} \times \mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins} \times \mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V} - \mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V} \times \mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q \times \mathsf{Vt}}{k \times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n} \mathsf{PI}_i \times \mathsf{C}_i)}$$

$$\mathsf{A}' = (1 - \mathsf{E}(1 - \mathsf{Pv}))\mathsf{A}$$

$$q = 1.60218 \times 10^{-19}\mathrm{C}$$

$$k = 1.38066 \times 10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

Q0 (1 Mark) !!Almost Free!!

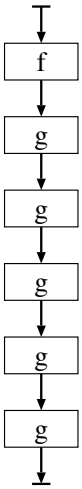
(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (17 Marks) Pipelining

(*estimated time: 15 minutes*)

Design a dataflow-diagram for the data-dependency graph shown below. The circuit will be implemented on an ASIC. Your goal is to maximize optimality, as defined by $\frac{1000}{ClkPeriod \times Area}$, where the clock period is measured in nanoseconds and area is measured in square microns (μm^2).



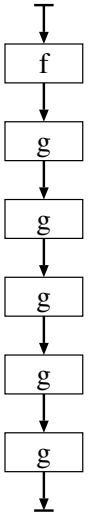
NOTES:

1. The circuit will be implemented on an ASIC, *not* on an FPGA. The area and delay for each component is given in the table below.
2. All of the datapaths are 10 bits wide: each f and g component has one 10-bit input and one 10-bit output.
3. Clock skew, clock jitter, and clock latency are all negligible.
4. The mininum throughput is 1/3.
5. The maximum latency is 8.
6. You must register the inputs, you do *not* need to register the outputs.

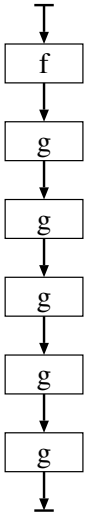
	Area (μm^2)	**Delay (ns)**
f	12	1.7
g	10	1.0
10-bit reg	10	setup: 0.05 hold: 0.07 tco: 0.04

Q1a (10 Marks) Design

Annotate a data-dependendency graph below to create a dataflow diagram with the maximum optimality. Multiple copies of the datadependency graph are provided to allow for scratch work. Put a $\surd$ in the box below the diagram that you wish to be marked.



Final version to be marked ☐



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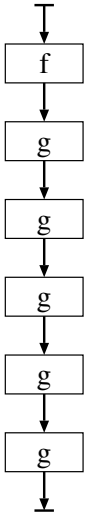


Final version to be marked ☐

Q1b (7 Marks) Analysis

Fill in the table below with the data for your design.

Area	
Minimum Clock Period	
Optimality	
Maximum Throughput	
Latency	

Q2 (17 Marks) Functional Verification

(*estimated time: 20 minutes*)

Q2a (3 Marks) Functional Simulation

For a typical digital circuit, what percentage of its behaviour can be verified with functional simulation during the design process?

In the table below, x represents the percentage of a typical circuit's behaviour that can be verified with functional simulation during the design process. Answer the question by writing a $\surd$ in the box of the row that best characterizes the range in which x would lie.

$0.00\% \leq x < 0.01\%$	☐
$0.01\% \leq x < 1.00\%$	☐
$1\% \leq x < 25\%$	☐
$25\% \leq x < 75\%$	☐
$75\% \leq x \leq 100\%$	☐

Q2b (5 Marks) Coverage Monitors

Give an example of a coverage monitor that could be used in a Kirsch edge detector. (You may use whatever notation is most appropriate: equation, schematic, VHDL code, diagram, or text.)

Either describe the purpose of your coverage monitor, or describe how would you use your coverage monitor.

Q2c (9 Marks) Simulation Options

One day at the lunch table in the cafeteria, your manager says that she recently learned that Y^0-Sim, the VHDL simulator that you use, has split their simulator into two products: one for functional simulation and one for timing simulation. She is considering buying either just the functional simulator or just the timing simulator, and using the money that she saves to buy more computers to speed up simulation.

Your current functional verification methodology uses a mixture of functional simulation, timing simulation, and running on the FPGA board, just as you were taught in ECE-327.

Your manager describes three options: "FTB", "FCB", and "TCB"; where "F" means functional simulation, "T" means "timing simulation", "C" means new computers, and "B" means FPGA board. All three options cost the same.

FTB Buy both the functional simulator and timing simulator, and continue with the current methodology.

FCB Don't buy the timing simulator; use functional simulation and FPGA boards for functional verification. Use the money saved by not buying the timing simulator to buy more computers, which will allow you to *run functional simulation 10-times faster than you do now.*

TCB Don't buy the functional simulator; use timing simulation and FPGA boards for functional verification. Use the money saved by not buying the functional simulator to buy more computers, which will allow you to *run timing simulation at the same speed as you currently run functional simulation.*

For each option, answer whether you think it should be chosen as the best option, considered as a possibility, or rejected. If you recommend that an option be chosen, then you must reject the other two options.

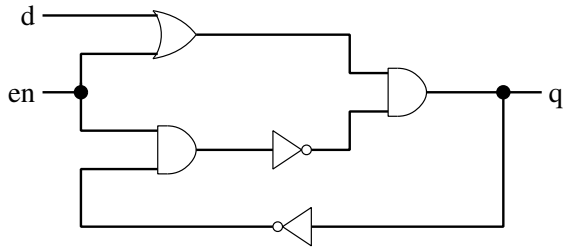
For each option, briefly justify your recommendation in terms of its advantages and/or disadvantages.

	Choose	Consider	Reject
FTB	☐	☐	☐
FCB	☐	☐	☐
TCB	☐	☐	☐

Q3 (16 Marks) Latch Analysis

(*estimated time: 15 minutes*)

Does the circuit below behave correctly as a latch? If not, explain why not. If yes, then calculate the clock-to-Q, setup, and hold times; and answer whether it is active-high or active-low.



NOTES:

1. The delay through each gate is 1 time unit

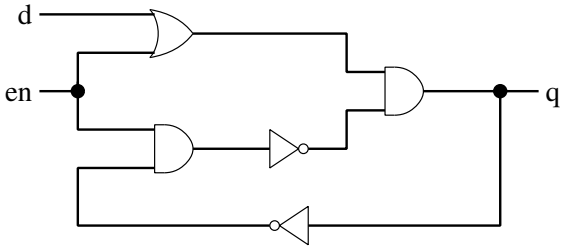
	Yes	**No**
The circuit behaves correctly as a latch	☐	☐

If the circuit behaves correctly as a latch:

	Active-Hi	**Active-Lo**	
Polarity	☐	☐	
Clock-to-Q			ns
Setup			ns
Hold			ns

If the circuit does *not* behave correctly as a latch, explain why it is incorrect.

Extra copy for scratch work



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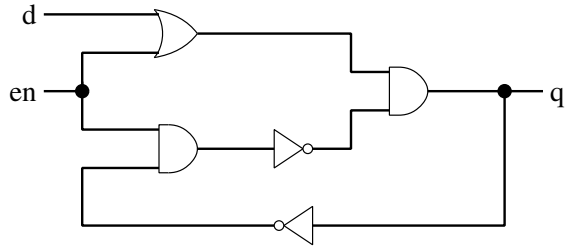

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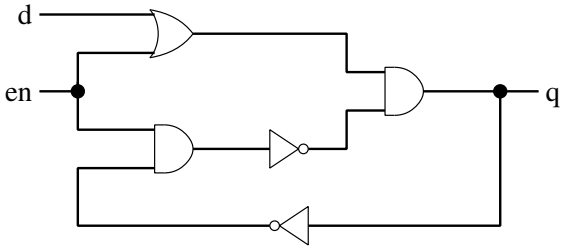

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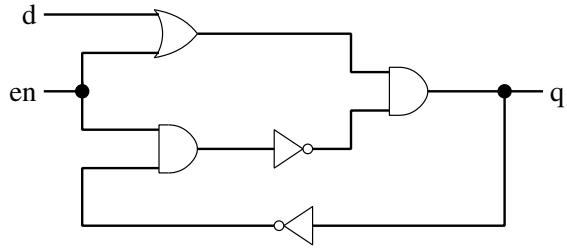


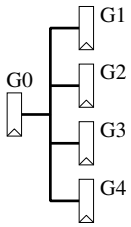
Q4 (16 Marks) Elmore Delay

(*estimated time: 25 minutes*)

In this question you will use the Elmore delay model to analyze the maximum clock speeds of three different layouts of the gate-level schematic shown below.

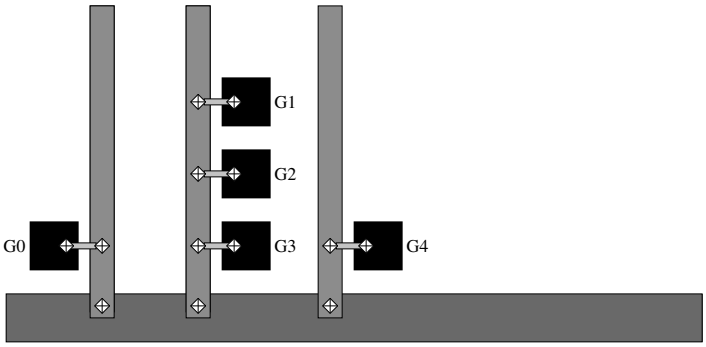
NOTES:

1. G0 is the source. G1, G2, G3, and G4 are the destinations.
2. Do *not* make any assumptions about the values of R, C_X, C_Y, C_Z, and C_g.
3. The capacitance of a wire is independent of distance and location on the wire.
4. Setup, hold, clock-to-Q, Clock skew, clock latency, and clock jitter are all negligible.
5. When comparing the speed of two layouts, compare the *maximum clock speed* of the layouts.

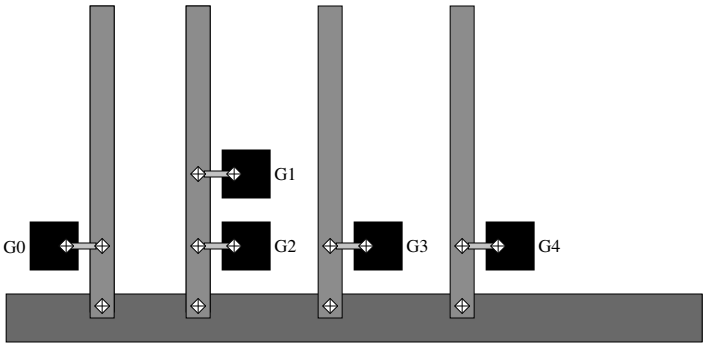


Gate-level schematic

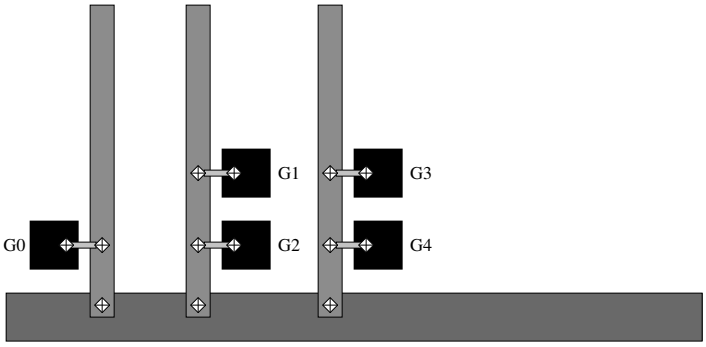
Symbol	Description	Capacitance	Resistance
	Gate	Cg	0
	Interconnect level 1	C_X	0
	Interconnect level 2	C_Y	0
	Interconnect level 3	C_Z	0
	Antifuse	0	R



Layout 1



Layout 2



Layout 3

Q4a (6 Marks) Layout 1 vs 2

Can you determine whether layout-1 is faster than, equal to the speed of, or slower than layout-2? **For full marks, you must justify your answer.**

Justification: _____

Layout-1 is ☐ **faster than** ☐ **equal to** ☐ **slower than** ☐ **cannot determine** layout-2.

Q4b (6 Marks) Layout 2 vs 3

Can you determine whether layout-2 is faster than, equal to the speed of, or slower than layout-3? **For full marks, you must justify your answer.**

Justification: _____

Layout-2 is ☐ **faster than** ☐ **equal to** ☐ **slower than** ☐ **cannot determine** layout-3.

Q4c (4 Marks) Nodes to Measure

To determine the maximum clock speed at which layout-1 would work correctly, at which node(s) would you measure the delay?

NOTES:

1. If any other nodes will have the same delay as the node that you would measure, list these nodes as well.

Nodes at which to measure delay for layout-1: _____

Q5 (17 Marks) Clock Gating

(*estimated time: 25 minutes*)

Your task is to analyze a proposed clock-gating scheme.

NOTES:

1. The latency through the main circuit is 15 clock cycles.
2. The average length of a continuous sequence of valid parcels is 45.
3. The area of the clock-gating circuit is 1/8 that of the main circuit.
4. Short-circuiting and leakage power are negligible.

What is the minimum number of bubbles between valid parcels, if the circuit with clock gating is to have a maximum of 90% of the power of the original circuit? If you are unable to reduce the power to be 90% of the power of the original circuit, then calculate the minimum power that you can achieve with clock gating.

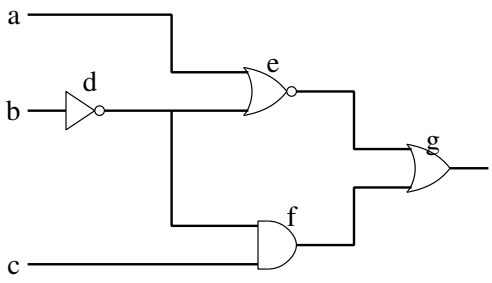
Minimum number of bubbles between valid parcels:
Or, minimum power with clock gating:

Q6 (17 Marks) Testing

(*estimated time: 25 minutes*)

The travel department at your company accidently sent your ticket to the "Manufacturing and Faults Conference (MFC)" to the VP of Marketing, and sent his ticket to the "Marketing Frolics Cabanal ($\mathcal{MFC}$)" to you. When the VP of Marketing returned from the faults conference, he was all excited about the hot topic of the conference, which was the "Single-stuck-at-1" (SS1) fault model. Unfortunately, despite his enthusiasm, he knows almost nothing about faults or testing, and so he has asked you to prepare a report for him to present to senior management.

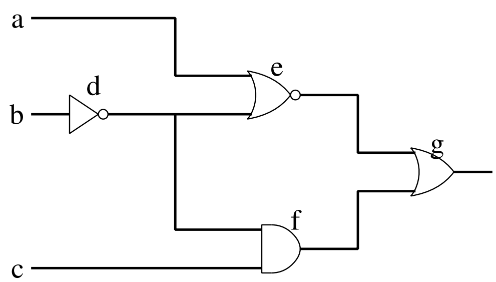
Find the minimum set of test vectors to catch all SS1 faults in the circuit below, and list the test vectors in the order to run them, from first to last.



NOTES:

1. If you do not know how to answer the question using the SS1 fault-model, then you for part-marks, you may answer the question using the fault model that we use in ECE-327. If you do so, write a $\surd$ in the box: ☐
2. The probability of a fault occuring on a wire driving a 1-input gate (e.g. inverter) is half that of the probability of a fault occuring on other wires. Your test vectors must still detect such a fault.
3. Write an "X" in the box for any test vector that is *not* needed.
4. There are copies of the circuit and Karnaugh-map templates on the pages following this question.

Test vec 1	Test vec 2	Test vec 3	Test vec 4	Test vec 5	Test vec 6	Test vec 7	Test vec 8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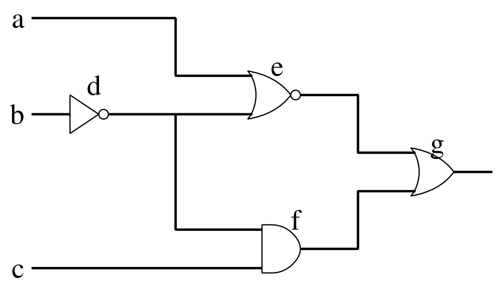
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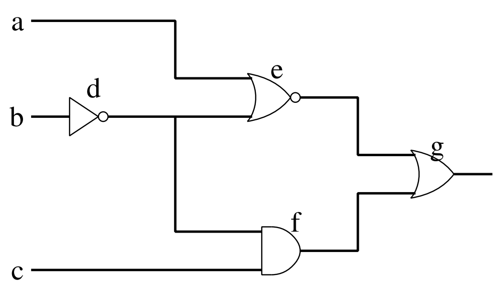
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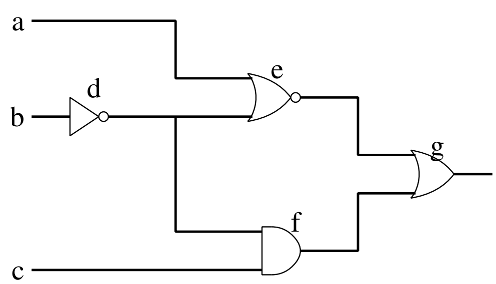
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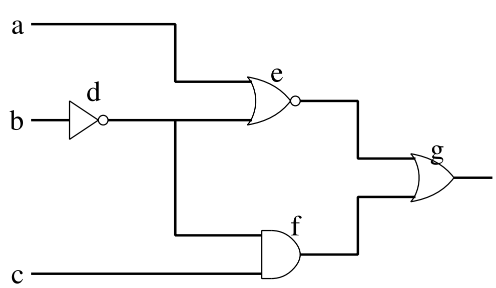
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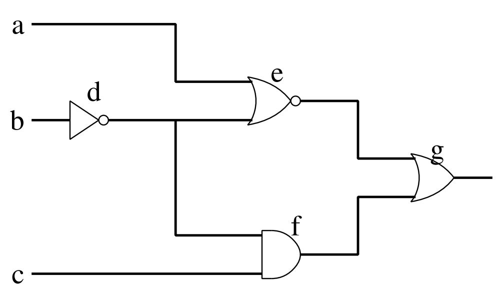
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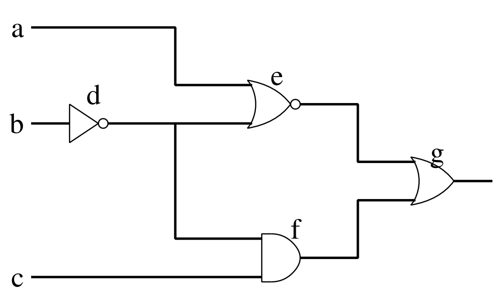
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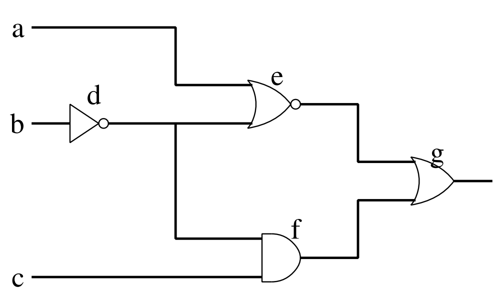
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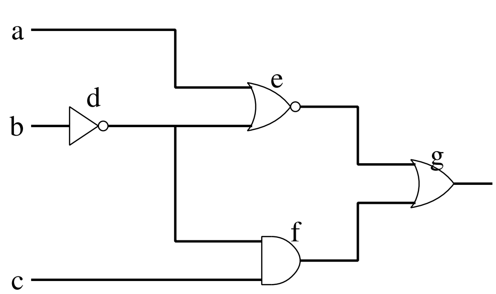
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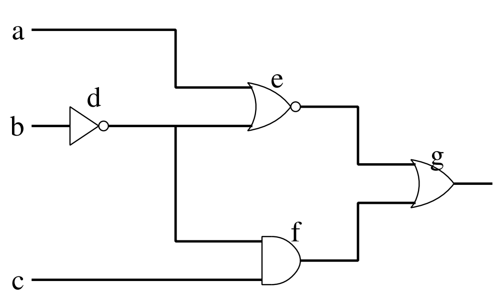
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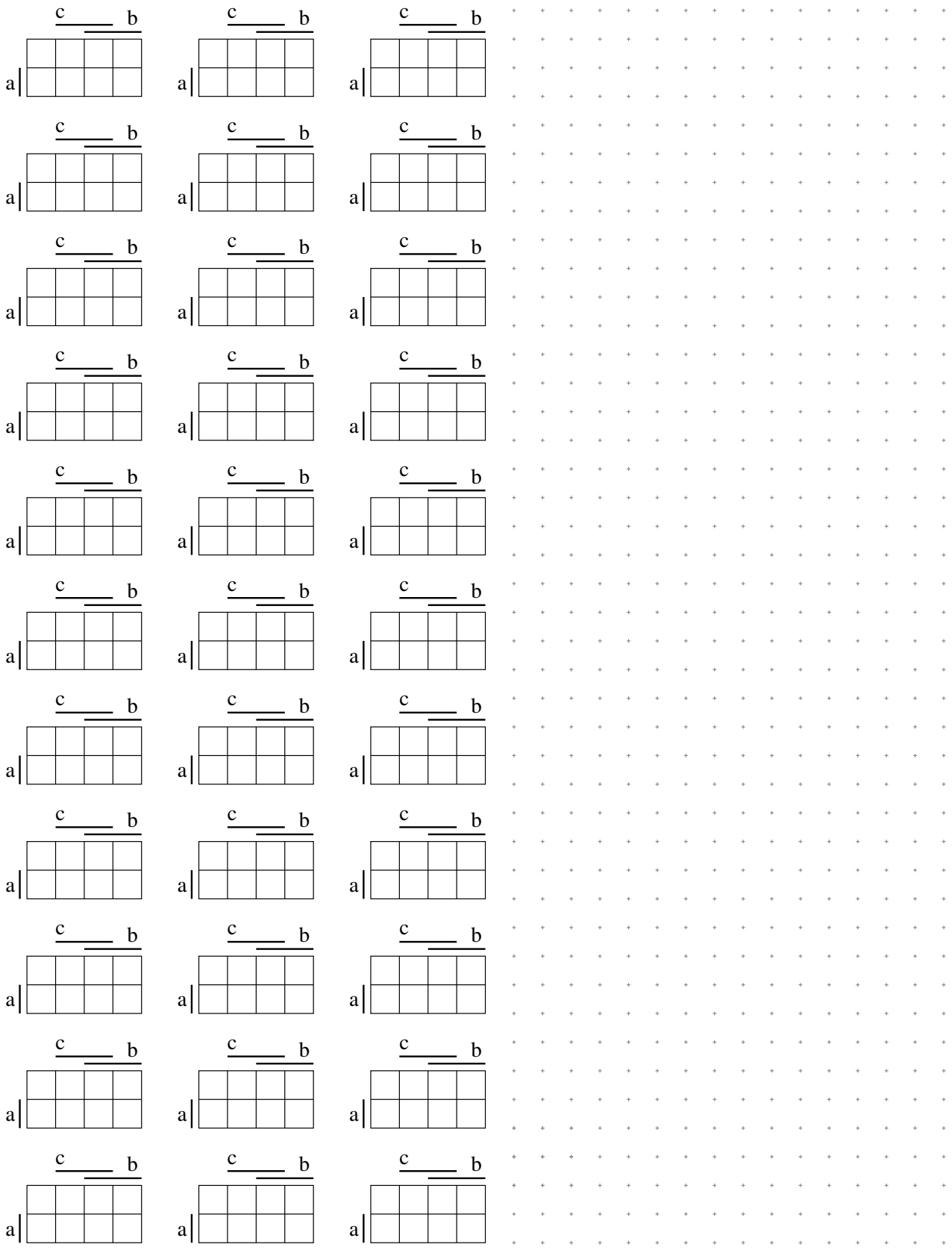
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