E&CE 327 Final

2011t1 (Winter)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the **formulas** you use and **all of your work**.
- The proctors and instructors will **not answer questions**, except in cases where an error on the exam is suspected. If you are confused about a question, write down your **assumptions or interpretation**.
- Justifications of answers will be marked according to **correctness, clarity, and concision**.

			Total Marks	**Approx. Time**	**Page**
Q0	!!Almost Free!!		1	0	3
Q1	Short Answer		20	15	4
Q2	Dataflow Diagram		20	30	5
Q3	Timing Analysis		20	30	7
Q4	Power		20	30	9
Q5	Faults and Testing		20	30	13
Totals			100	135	

Name:_____

UWUserid:_____

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A} \times \mathsf{C} \times \mathsf{V}^2 \times \mathsf{F}) + (\tau \times \mathsf{A} \times \mathsf{V} \times \mathsf{ISh} \times \mathsf{F}) + (\mathsf{V} \times \mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins} \times \mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V} - \mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V} \times \mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q \times \mathsf{Vt}}{k \times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n} \mathsf{PI}_i \times \mathsf{C}_i)}$$

$$\mathsf{A}' = (1 - \mathsf{E}(1 - \mathsf{Pv}))\mathsf{A}$$

$$q = 1.60218 \times 10^{-19}\mathrm{C}$$

$$k = 1.38066 \times 10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Although it has historical significance in the field of image processing, the "Lena" image in the Kirsch edge detector test suite deserves to be replaced. This is your chance to vote for one of the following images to replace "Lena". Your vote should be based purely upon the merits of the image for testing edges and directions. Aesthetics should not influence your opinion.

Q1 (20 Marks) Short Answer

(*estimated time: 15 minutes*)

Q1a (10 Marks) Hardware Description Languages

One of the annoying features of VHDL and Verilog is that it can be difficult to predict what hardware will be synthesized for a VHDL or Verilog program, because the semantics of these languages defines the *behaviour* of a digital system, but says nothing about the *structure* of the hardware.

Would a hardware description language whose semantics defined both the structure and the behaviour of hardware be an improvement over VHDL and Verilog? **For full marks, you must justify your answer.**

	Yes	**No**
Improvement	☐	☐

Q1b (10 Marks) Functional Verification

Your task is to design a small (16×16 pixel) test image for functional verification of Kirsch edge detectors. The goal is to have an image that is small enough that timing simulation can be done quickly, but yet still have high confidence that an edge detector that computes the edges and directions correctly for the test image will work correctly for all images.

Using words and/or pictures, describe an image that meets these goals.

Q2 (20 Marks) Dataflow Diagram

(*estimated time: 30 minutes*)

In this question, you will design a dataflow diagram for the following equation:

$$(a+b) \times (b+c) \times (c+d) \times (d+e)$$

NOTES:

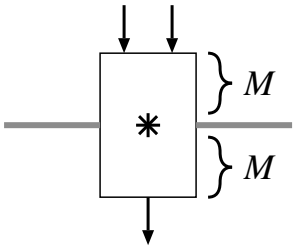
1. There is a maximum of two inputs ports
2. The only algebraic optimizations you may use are commutativity and associativity:

	Commutativity	Associativity
Addition	$\alpha + \beta = \beta + \alpha$	$(\alpha + \beta) + \gamma = \alpha + (\beta + \gamma)$
Multiplication	$\alpha \times \beta = \beta \times \alpha$	$(\alpha \times \beta) \times \gamma = \alpha \times (\beta \times \gamma)$

3. Your goals are, in order of priority, from highest priority to lowest:
   (a) Maximize throughput
   (b) Maximize clock speed
   (c) Minimize area
   (d) Minimize latency
4. All signals are declared as `signed(15 downto 0)`
5. Do not worry about overflow
6. Inputs shall be registered. Outputs may be either combinational or registered.
7. The relative areas of the components are:

16-bit register	2	16-bit input port	5
16-bit 2:1 multiplexer	1	16-bit output port	5
16-bit adder	2		
16-bit multiplier	5		

8. The multiplier has a latency of two clock cycles, throughput of 1/2, and a minimum clock period of M. You may draw a multiplier as shown below. The multiplier has an internal register that is used to hold temporary results for the second clock cycle.



9. Maximum clock period = flop + max(add, M)
10. The dataflow diagram is to be drawn on the next page.

Q2a (14 Marks) Dataflow Diagram

Draw a dataflow diagram that satisfies the requirements and goals given above.

Q2b (6 Marks) Analysis

Based upon your diagram, fill in the table below:

Number of stages		Number of 16-bit registers (not including registers inside the multipliers)	
Latency		Number of 16-bit 2:1 multiplexers	
Minimum clock period		Number of 16-bit adders	
Maximum throughput		Number of 16-bit multipliers	

Q3 (20 Marks) Timing Analysis

(*estimated time: 30 minutes*)

In this question, you will analyze two circuits to determine if a path is a false path.

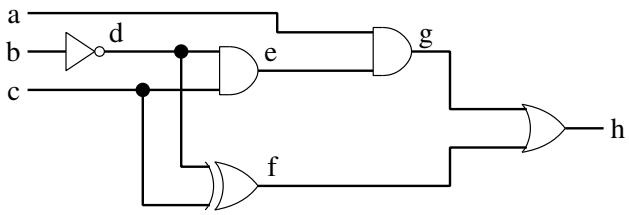
Gate	Delay
	2
	4
	6

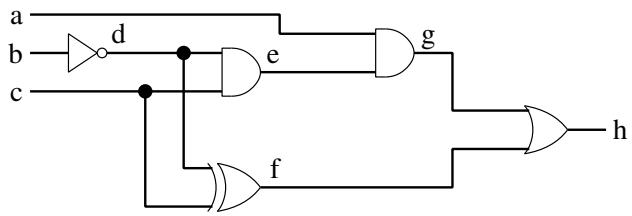
Q3a (10 Marks) First circuit

For the circuit below, find the longest path and determine if the longest path is a false path.

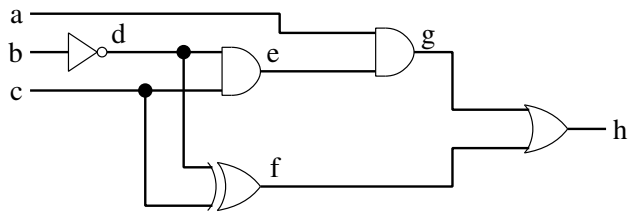
If the longest path is a false path, explain why it is false.

If the longest path is not a false path, give a set of values on the primary inputs that will exercise the path.





Extra copy of first circuit



Extra copy of first circuit

Longest path _____

	Yes	No
Path is false	☐	☐

If path is false, justification:

_____

_____

_____

_____

If path is not false, excitation:

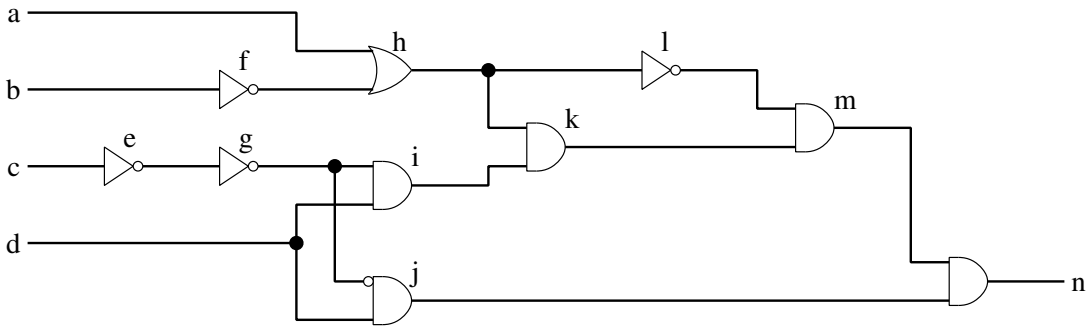
a	b	c

Q3b (10 Marks) Second circuit

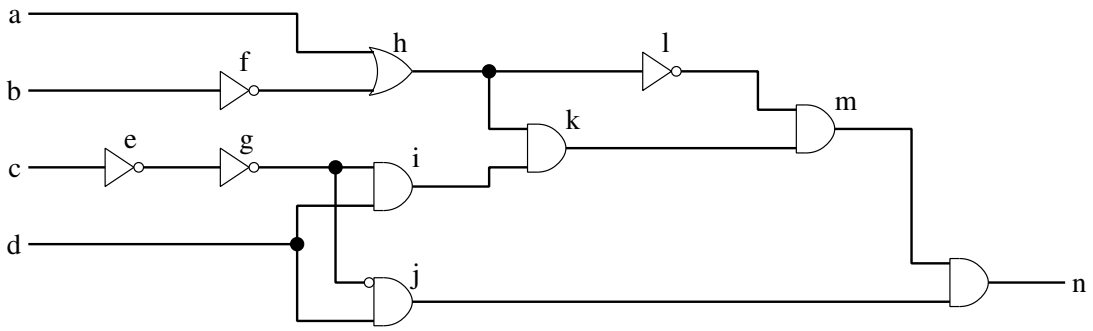
For the circuit below, the longest path $\langle c, e, g, i, k, m, n \rangle$ is a false path. Find the second longest path and determine if it is a false path.

If the second longest path is a false path, explain why.

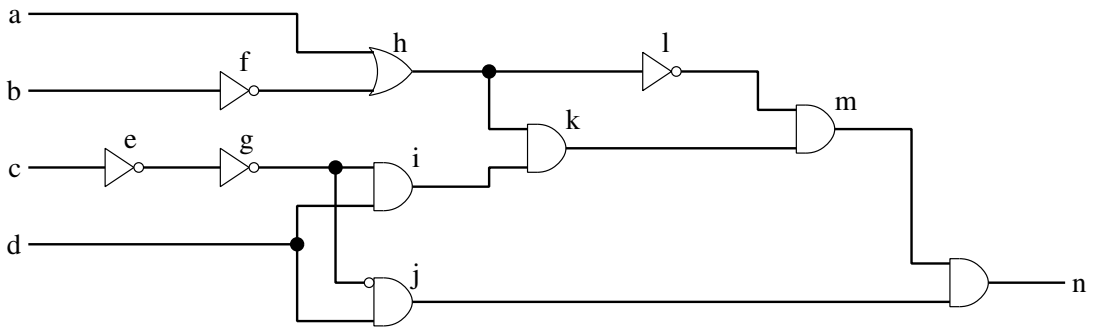
If the second longest path is not a false path, give a set of values on the primary inputs that will exercise the path.



Extra copy of second circuit



Extra copy of second circuit



Second longest path _____

	Yes	**No**
Path is false	☐	☐

If path is false, justification:

_____

_____

_____

_____

If path is not false, excitation:

a	**b**	**c**	**d**
☐	☐	☐	☐

Q4 (20 Marks) Power

(*estimated time: 30 minutes*)

Your manager has asked you to design a clock gating scheme for the circuit described below (the information describes the circuit without any clock gating):

Latency	10 clock cycles
Throughput	1
Clock speed	800 MHz
Percentage of input parcels that are valid	40 %
Average number of consecutive valid parcels	20
Short circuiting power	1 mW
Leakage power	3 mW
Switching power	5 mW

You are evaluating two clock gating schemes:

Option A A single "cool", or gated, clock is used for the entire pipeline.

Option B Each stage of the pipeline has its own gated clock.

Q4a (14 Marks) Clock gating scheme

Your manager has asked you to choose which clock-gating scheme to implement based upon the information above and reasonable assumptions. She has suggested two assumptions:

1. Option A and option B will both have an effectiveness of 100%.
2. The clock-enable circuitry for option A and option B will both have negligible power consumption compared to the main circuit.

If you need to make any additional assumptions for Question Q4a, list them here:

Which clock gating scheme (option A or B) will result in the lowest power consumption, and what will be the total power consumption if you use this scheme?

Option A **Option B**

The scheme that will result in the lowest total power is ☐ ☐

Using this scheme, the total power consumption will be: ☐

Q4b (3 Marks) Burst length

Late on a Friday afternoon, your manager drops by your desk and says that the original estimate for the average number of consecutive valid parcels was too low. Assuming everything else *stays the same*, can you determine whether *increasing* the number of consecutive valid parcels will decrease, have no effect on, or increase the total power consumption? **For full marks, you must justify your answer.**

Effect on total power: **Decrease** ☐ **No effect** ☐ **Increase** ☐

Q4c (3 Marks) Clock speed

Another Friday afternoon, just as you are packing up to head home, your manager drops by again and says that when the first chips come back from fabrication, the maximum clock speed at which they worked correctly was 750 MHz, rather than the 800 MHz of the original circuit on the same fabrication line. Can you make any hypothesis as to what could have caused the drop in clock speed? **For full marks, you must justify your answer.**

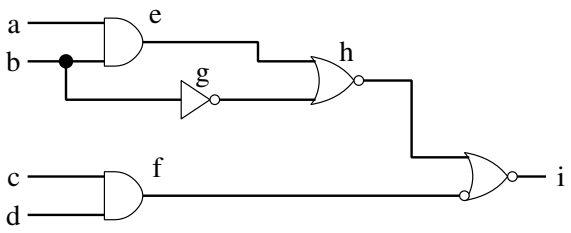
Q5 (20 Marks) Faults and Testing

(*estimated time: 30 minutes*)

The hot topic at last years Manufacturing Faults Conference was the "Single-stuck-at-1" fault model. In keeping with the rapid pace of research in digital hardware, this year, the focus changed to the "Single-stuck-at-0" (SS0) fault model.

Q5a (15 Marks) Test Vectors

Find the minimum set of test vectors to catch all SS0 faults in the circuit below, and list the test vectors in the order to run them, from first to last.



NOTES:

1. If you do not know how to answer the question using the SS0 fault-model, then for part-marks, you may answer the question using the fault model that we use in ECE-327. If you do so, write a $\surd$ in the box: ☐
2. Write an "X" in the box for any test vector that is *not* needed.
3. A colleague who really enjoys Karnaugh maps started to work on this problem, but fell asleep at his desk because he had been up all night working on a project for his son's nursery school. His partially completed work is on the next page. The work that he completed is correct.
4. There are copies of the circuit and Karnaugh-map templates on the pages following this question.

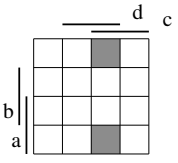
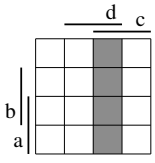
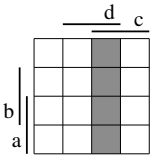
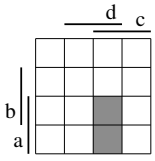
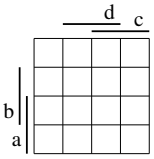
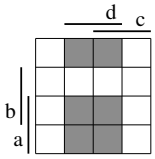
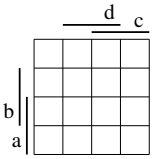
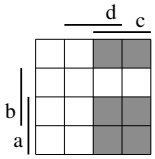
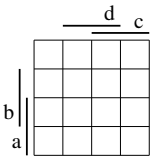
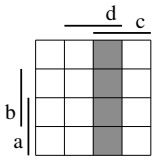
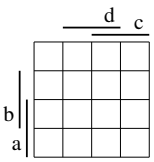
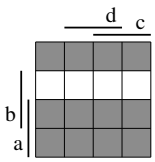
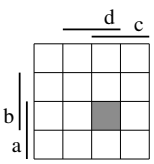
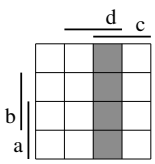
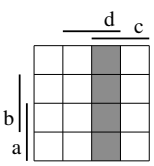
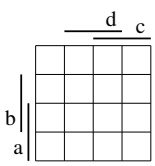
Test vec 1	Test vec 2	Test vec 3	Test vec 4	Test vec 5	Test vec 6	Test vec 7	Test vec 8

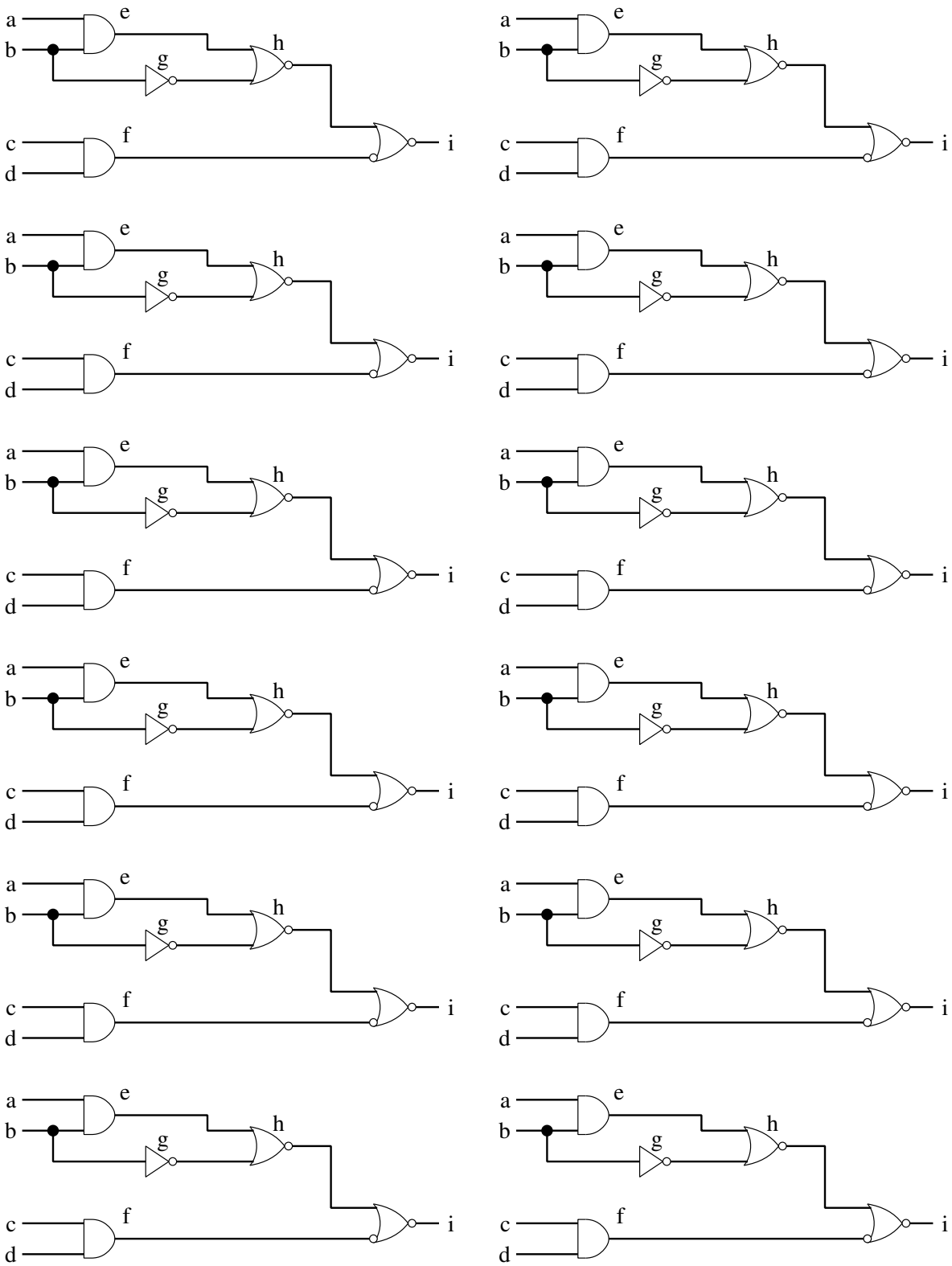
Potentially Useful Information and Worksheet

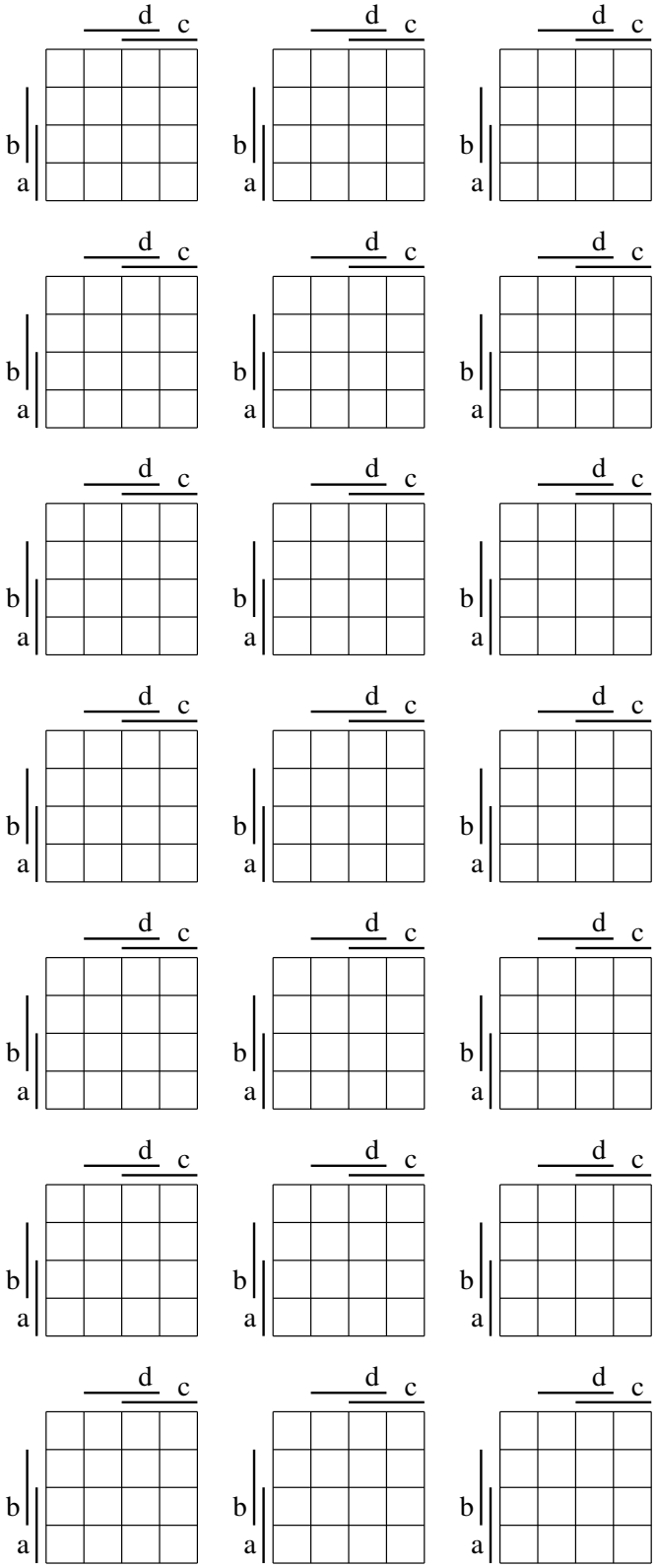
This page contains equations and Karnaugh maps describing the behaviour of circuit with some faults.

NOTES:

1. You do *not* need to fill in this sheet.
2. Some relevant faults might *not* have been been listed.
3. Some of the listed faults might *not* be relevant.

signal	shorted to 0		shorted to 1	
a	$\overline{b}cd$		cd	
b	cd		acd	
c			$ad + \overline{b}d$	
d			$ac + \overline{b}c$	
e			cd	
f			$a + \overline{b}$	
g	$abcd$		cd	
h	cd			


a
b
c
d
e
f
g
h
i


d
c
b
a

Q5b (5 Marks) Detected Faults

For each of the two faulty circuits below, answer whether the set of test vectors that you chose in Question Q5a will detect that the circuit is faulty. **For full marks, you must justify your answer.**

Faults present in circuit	Detected Yes	No
a shorted to 0 and **e** shorted to 0	☐	☐

Justification:

Fault present in circuit	Detected Yes	No
f shorted to 1	☐	☐

Justification: