E&CE 327: Solution to Final Exam

2012t1 (Winter)

Q1 (20 Marks) Short Answer

Q1a (6 Marks) Delta-Cycle Simulation

In delta-cycle simulation, in which mode do processes start, and why do the VHDL simulation semantics require that processes start in this mode?

Answer:

All processes start out postponed.

All processes that start as postponed in a simulation cycle, are given a chance to run in that simulation cycle. Without this rule, processes would remain suspended until an external stimulus was provided to cause them to have a need to run.

Marking:

Mode

2 marks *"Postponed"*

1 mark *"Active" or "Suspended"*

Reason

4 marks *"all processes run"*

2 marks *information is correct, but does not justify answer*

1 mark *some correct infomation*

Q1b (8 Marks) Functional Verification

For each of the two situations below, answer whether the situation is possible. **Briefly justify your answer**

1. The circuit is correct. One of the assertions has a bug. All of the test-vectors pass without any assertion failures.

Answer:

Yes, it is possible. None of the test vectors triggered the buggy assertion, the buggy assertion describes a situation that cannot occur (e.g., "if the microwave oven is on and the power is not connected ..."), or a bug in the instrumentation code masked the bug in the assertion.

Marking:

4 marks *correct answer*

2 marks *information is correct, but does not justify answer*

1 mark *some correct information or "Yes" without justification*

2. The circuit is correct. All of the assertions are correct. Some of the test-vectors fail one of the assertions.

Answer:

Yes, it is possible. A bug in the instumentation code *could cause an assertion to fail when it should not, or an "illegal" test-vector is run (illegal in that it violates the constraints or assumptions about the input data, for example sending valid data while reset is on).*

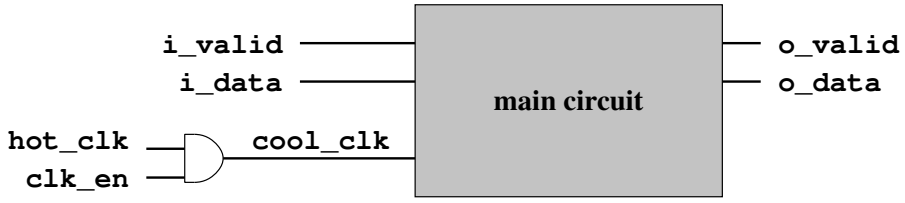
Marking:

4 marks *correct answer*
2 marks *"No, assertions define the correct behaviour"*
1 mark *some correct information or "Yes" without justification*

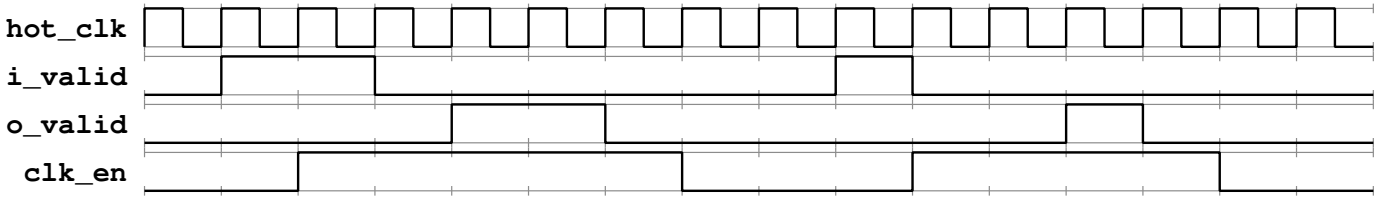
Q1c (6 Marks) Clock Gating

For the system described below, draw the waveform for the `clk_en` signal so that the signal `cool_clk` is turned on for the minimum number of clock cycles such that the main circuit works correctly.

NOTES:
1. The latency through the system is 3 clock cycles.



Answer:



The signal `o_valid` is shown for clarity, it is not required as part of the answer.

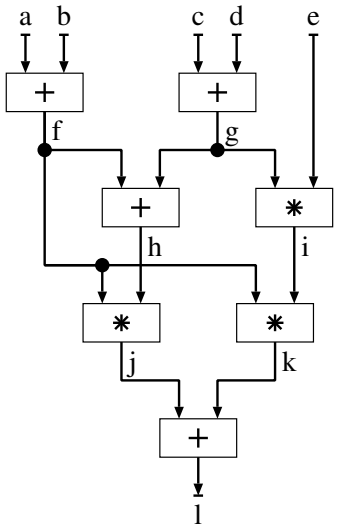
Marking:

6 marks *correct answer*
-1 mark *one or both intervals start one cycle too early/late*
-2 marks *one or both intervals start two cycles too early/late*

-1 mark *one or both intervals end one cycle too early/late*
-1 mark *inconsistent start and/or end behaviour between two intervals*
3 marks *two intervals with clken='1'*
2 marks *one interval with clken='1'*
1 mark *clken='1' entire time*

Q2 (20 Marks) Dataflow Diagram

In this question, you will design and analyze a dataflow diagram for the data-dependency graph below.



NOTES:

1. Timing

Register setup	2 ns
Register hold	1 ns
Register clock-to-Q	3 ns
Clock skew	0.5 ns
Clock jitter	0.7 ns
Clock latency	1 ns
Delay through adder	7 ns
Delay through multiplier	12 ns
Delay through multiplexer	0 ns

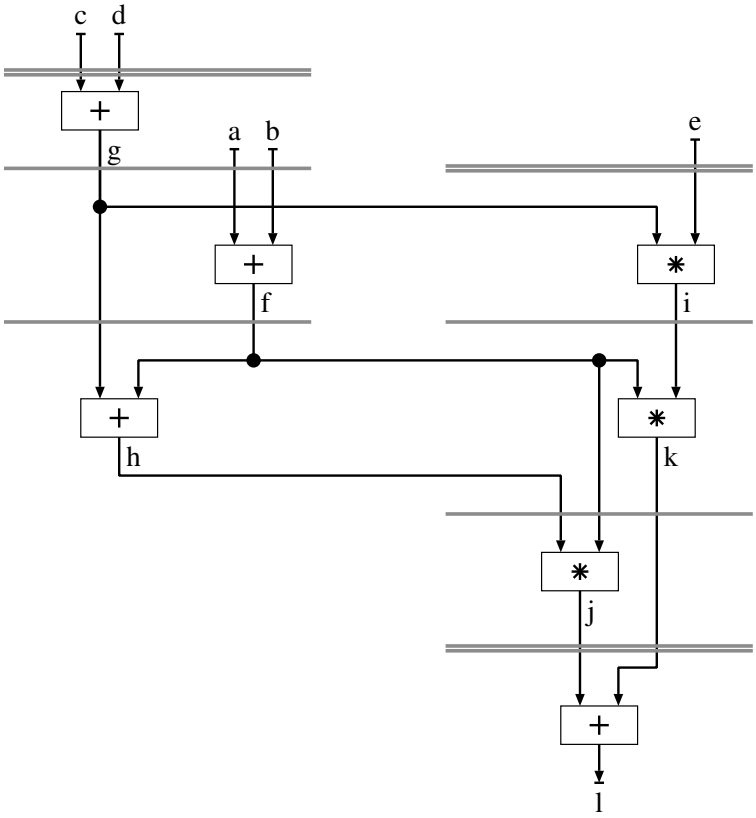
2. Requirements
   (a) Registered inputs.
   (b) Combinational outputs.
   (c) The minimum throughput shall be 1/3
3. Goals (from highest priority to lowest)
   (a) Minimize area
      - Order of priority from highest to lowest: Multipliers, adders, inputs, registers.
      - Multiplexers are free
   (b) Minimize clock period
   (c) Minimize latency
4. You shall *not* use any algebraic optimizations, except commutivity, which might be helpful in simplifying the routing of signals.
5. You shall *label all signals*.
6. You do *not* need to do any allocation.

Q2a (15 Marks) Design

Design a dataflow diagram that satisfies the requirements and maximizes the goals listed above.

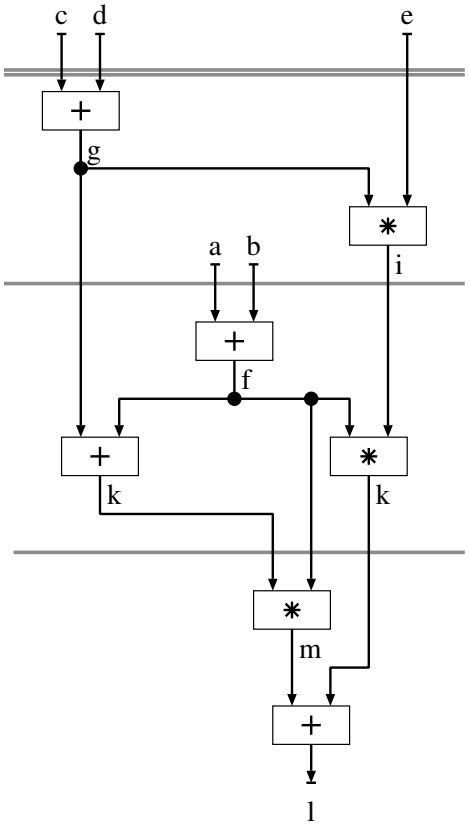
Answer:

1. *Optimal solution (overlapping stages)*



Number of inputs	*2 + 1 +*	*0*	=	*3*
Number of registers	*3 + 3 +*	*2*	=	*8*
Number of multipliers	*0 + 1 +*	*0*	=	*1*
Number of adders	*0 + 1 +*	*1*	=	*2*
Number of outputs	*0 + 0 +*	*1*	=	*1*
Latency				*5*
Throughput	*1/3 1/3*	*1/1*	=	*1/3*
Clock period	*0.5 + 0.7 + 3 + 12 + 2*		=	*19.2 ns*
	skew + jitter + clock-to-Q + mult + setup			

2. Suboptimal solution



Number of inputs	*3*
Number of registers	*4*
Number of multipliers	*1*
Number of adders	*2*
Number of outputs	*1*
Latency	*3*
Throughput	*1/3*
Clock period	*0.5 + 0.7 + 3 + 7 + 12 + 2 = 26.2 ns*

Marking:

Dataflow diagram

- **15 marks** *optimal solution*
- **13 marks** *suboptimal solution (3 inputs)*
- **12 marks** *2-stage pipeline w/ longer period*
- **11 marks** *suboptimal solution with f in first clock cycle (5 inputs)*
- **9 marks** *solution with 2 adds and 1 mult*
- **8 marks** *meets requirements*
- **7 marks** *functionally correct*
- **5 marks** *syntactically correct*
- **-1 mark** *combinational inputs*
- **-1 mark** *registered outputs*

Analysis

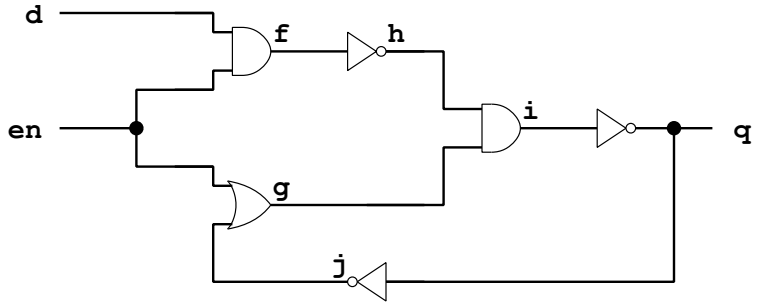
Q2b (5 Marks) Analysis

Answer:

See above

Q3 (15 Marks) Latch Analysis

In this question, you will analyze the circuit below to determine if it is correct implementation of a latch.



NOTES:

1. The delay through each gate is 1 ns.

Q3a (3 Marks) Good or Bad?

Answer:

Yes, the circuit is a correct implementation of a latch.

Marking:

3 marks *correct answer*

1 mark *incorrect answer (if rest of question is answered)*

Q3b (7 Marks) Analysis

Determine if the latch is active-high or active-low and calculate the timing parameters below.

Answer:

Active-high or active-low?	*Active high*	*1 mark*
Clock-to-Q	*4*	*2 marks*
Setup	*5*	*2 marks*
Hold	*0*	*2 marks*

Marking:

latch is correct **1 mark** *answer is* ± 1 *the correct answer*

latch is incorrect **7 marks** *glitch on transition from load to store caused by delay from d to i being longer than delay from en to i*

5 marks *problem on transition from load to store caused by improper choice of gate delays*

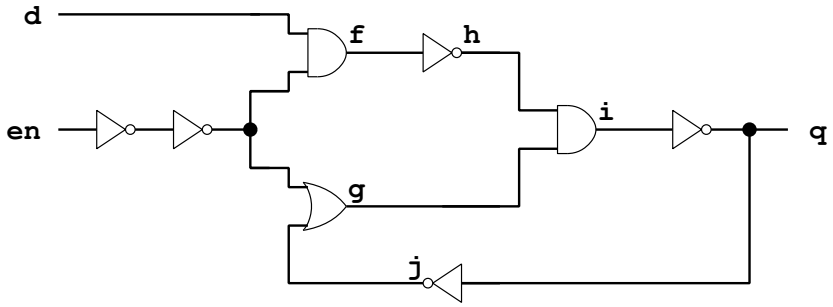
4 marks *glitch on transition from load to store*

2 marks *glitch on transiton from store to load, or no mention of which mode transition has the glitch*

Q3c (5 Marks) Modification

Modify the circuit using the diagram below to *decrease the setup time* by 2 ns.

Answer:



Marking:

latch is correct

1 mark *functionality*
- *q is not inverted*
- *even number of inverters on storage loop*
- *mux between load-path and storage loop works*
- *delay from d to i is greater than or equal to delay from en to i*

1 mark *remains active-high*

1 mark *decreases setup by 2 ns*

$-\frac{1}{2}$ **mark** *use 3 inverters (one each on branches to f and g)*

latch is incorrect

1 mark *q is not inverted*

1 mark *even number of inverters on storage loop*

1 mark *mux between load-path and storage loop works*

1 mark *delay from d to i is greater than or equal to delay from en to i*

1 mark *active high*

For each of the timing parameters below, answer whether your modification to the latch increases, does not change, or decreases the value of the timing parameter.

Answer:

	Increase	*No change*	*Decrease*
Clock-to-Q	$\surd$		
Hold	$\surd$		

Marking:

2 marks *2 correct answers*

1 mark *1 incorrect answer*

$\frac{1}{2}$ **mark** *2 incorrect answers*

Q4 (20 Marks) Critical Path

For the circuit below, the longest path $\langle \mathtt{d}, \mathtt{g}, \mathtt{i}, \mathtt{l}, \mathtt{n}, \mathtt{o}, \mathtt{p}, \mathtt{q} \rangle$ is a false path.

NOTES:

1. Delay through gates: NOT=2, AND=4, OR=4, XOR=6.

Q4a (15 Marks) Second-Longest Path

Find the second-longest path and determine if it is a viable path or a false path.

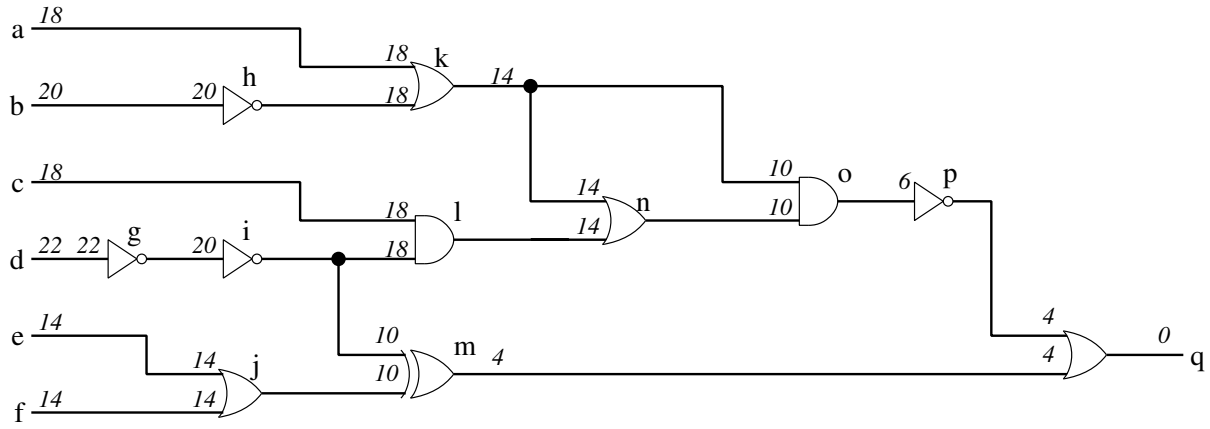
If the second-longest path is *viable*, give a set of values on the primary inputs that will exercise the path.

If the second-longest path is a *false* path, explain why.

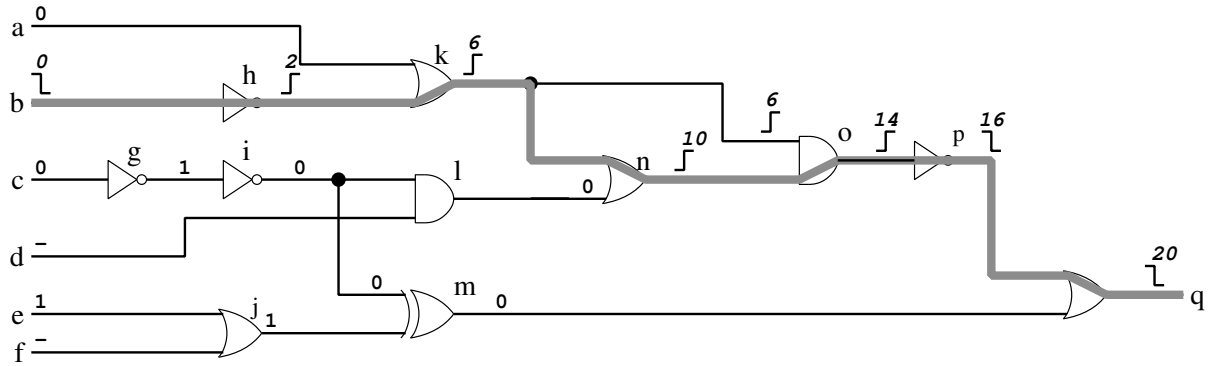
NOTES:

1. If there are multiple second-longest paths with the same delay, choose the path that is alphabetically earlier (e.g., if the second-longest paths are $\langle \mathtt{q}, \mathtt{r}, \mathtt{s}, ... \rangle$ and $\langle \mathtt{q}, \mathtt{r}, \mathtt{u}, ... \rangle$, choose $\langle \mathtt{q}, \mathtt{r}, \mathtt{s}, ... \rangle$)

Answer:



There are many excitations that exercise the critical path. One example is shown below.



Marking:

2 marks *correct path*
1 marks *viable="yes"*
If deriviation is clear and understandable, or said "false"
3 marks *non-controlling values on side inputs*
3 marks *propagate constraints to inputs*
2 marks *conjunction of constraints*
2 marks *Boolean algebra, check for contradiction*
2 marks *translate constraint into excitation*
If derivation is unclear
3 marks *a='0'*
3 marks *b=falling edge*
3 marks *c='0' or d='0'*
3 marks *if d='1' then e='1' or f='1'; if d='0' then e='0' or f='0'*

Q4b (5 Marks) Monotone Speedup

Based upon the two longest paths through the circuit, does this circuit illustrate the benefits of taking into account monotone speedup when determining the critical path? **For full marks, you must justify your answer.**

If you are unable to determine whether this circuit illustrates monotone speedup by analyzing the two longest paths, then explain the concept of monotone speedup and why it is beneficial to take into account monotone speedup when finding the critical path through a circuit.

Answer:

The two paths do not *illustrate monotone speedup. Monotone speedup requires a late-arriving side input. We are able to exercise the critical path without using any late-arriving side inputs.*

Marking:

"No"
5 marks *correct answer*
3 marks *$k \rightarrow o$ is faster than candidate path*
"Yes"
2 marks *$k \rightarrow o$ illustrates monotonic speedup*
"Yes" or "Unable"
1 mark *clock period must stay the same or decrease if part of the circuit becomes faster*
1 mark *makes a path that appears to be false become viable*
1 mark *late side input has a non-controlling value*
1 mark *speed up a previously discovered false path to make the edge come earlier than the edge on the path input*

Q5 (25 Marks) Performance and Power

Waterluvian filters have become so popular that all of the major microprocessor and FPGA companies offer specialized Waterluvian microprocessors, and there is a standard Waterluvian assembly language. This standardization has caused MIPS/Watt to become the dominant measure of optimality for Waterluvian filters.

You are the design manager for a Waterluvian-processor that is implemented on an FPGA. You are making plans for the next version of your system. Michelle Ips, an engineer on your team, has proposed a performance optimization. Walter Att, another engineer on your team, has proposed a clock-gating scheme. You have the resources to implement only one of the two proposals.

NOTES:

1. Statistics for your current Waterluvian filter:

Supply voltage	1.2 V
Threshold voltage	0.4 V
Area	3000 cells
Activity factor	0.23
Leakage power	100 mW
Short circuiting power	3 mW
Switching power	500 mW
Valid incoming parcels	35 %
Average length of continuous sequence of valid parcels	40
Latency	20 clock cycles
Clock speed	500 MHz

2. The average MIPS/Watt of Waterluvian filters increases by 2% each week.
3. Walter Att's clock-gating scheme will use 200 cells, have no effect on performance, and require 15 weeks of effort. Walter does not yet know the effectiveness of his clock gating scheme.
4. Michelle Ips' performance optimization will increase performance by 95%, have no effect on power, and require 35 weeks of effort.
5. Suggested notation:

W	power (watts)	O_0	original (current) optimality
M	performance (MIPS)	O_1	Walter's optimality
O	optimality (MIPS/Watt)	O_2	Michelle's optimality
t	time	$O_{\text{avg}}(t)$	Average optimality at time t

What is the minimum effectiveness that Walter's clock gating scheme must achieve for it to provide the same MIPS/Watt *relative to the average Waterluvian filter at the time that it will be completed* that Michelle's performance optimization will provide *relative to the average Waterluvian filter at the time that it will be completed.*

Answer:

Our overall strategy will be to begin with the optimality of Michelle's solution and work our way toward the efficiency of Walter's clock-gating scheme.

1. *Initial equations (for $i \in \{0,1,2\}$)*

$$\begin{aligned}
W_i &= P_{sw_i} + P_{sh_i} + P_{lk_i} \\
P_{sw_i} &= \tfrac{1}{2} A_i f C_i V^2 \\
\frac{M_i}{W_i} &= O_i \\
M_1 &= M_0 \\
W_2 &= ??? \\
M_2 &= 1.95 M_0 \\
W_2 &= W_0 \\
O_2 &= O_1 \times 1.02^{(35-15)} \\
&= O_1 \times 1.4859
\end{aligned}$$

2. *Total power for Walter's solution*

$$\begin{aligned}
W_1 &= \frac{M_1}{O_1} \\
&= M_0 \left(\frac{1}{O_1} \right) \\
&= M_0 \left(\frac{1.4859}{O_2} \right) \\
&= M_0 (1.48) \left(\frac{W_2}{M_2} \right) \\
&= M_0 (1.48) \left(\frac{W_0}{M_2} \right) \\
&= M_0 (1.48) W_0 \left(\frac{1}{1.95 M_0} \right) \\
&= (1.48) W_0 \left(\frac{1}{1.95} \right) \\
&= 0.7620 W_0
\end{aligned}$$

$$\begin{aligned}
W_0 &= P_{sw.0} + P_{sh.0} + P_{lk.0} \\
&= 500 + 3 + 100 \\
&= 603\text{mW}
\end{aligned}$$

$$\begin{aligned}
W_1 &= 0.7620 \times 603 \\
&= 459.5\text{mW}
\end{aligned}$$

3. Percentage of time with valid parcels in system

$$\begin{aligned} T &= \textit{time window for clock gating analysis} \\ &= \frac{NumPcls}{PctIValid} \\ &= \frac{40}{0.35} \\ &= 114.3 \textit{clock cycles} \\ PctValid &= \frac{NumPcls + Latency}{T} \\ &= \frac{40+20}{114.3} \\ &= 0.5249 \end{aligned}$$

4. Effectiveness of Walter's scheme

$$Eff = \frac{1 - PctClk}{1 - PctValid}$$

$$PctClk = \frac{A_1}{A_0}$$

$$\begin{aligned} W_1 &= W_{1.main} + W_{1.cg} \\ W_1 &= P_{sw.1.main} + P_{sh.1.main} + P_{lk1.main} + \frac{C_{cg}}{C_0} W_0 \\ &= \frac{A_1}{A_0} P_{sw.0} + \frac{A_1}{A_0} P_{sh.0} + P_{lk.0} + \frac{C_{cg}}{C_0} W_0 \\ \frac{A_1}{A_0} &= \frac{W_1 - \left(P_{lk.0} + \frac{C_{cg}}{C_0} W_0 \right)}{P_{sw.0} + P_{sh.0}} \\ &= \frac{459.5 - \left(100 + \frac{200}{3000} 603 \right)}{500 + 3} \\ &= 0.6348 \\ Eff &= \frac{1 - 0.6348}{1 - 0.5249} \\ &= 0.7687 \end{aligned}$$

Marking:

1 mark *clarity of answer*
4 marks *exponential growth*
4 marks *calculation of window*
4 marks *calculation of percentage of time with valid parcels in system*
4 marks *calculation of power with clock gating*
4 marks *treatment of leakage and short-circuiting power*
4 marks *calculation of effectiveness*