First Name

Last Name

First letter of last name

UW Userid

E&CE 327: Final Exam

2012t1 (Winter)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the formulas you use and all of your work.
- **The proctors and instructors will not answer questions, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.**
- **Justifications of answers will be marked according to correctness, clarity, and concision.**

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A} \times \mathsf{C} \times \mathsf{V}^2 \times \mathsf{F}) + (\tau \times \mathsf{A} \times \mathsf{V} \times \mathsf{ISh} \times \mathsf{F}) + (\mathsf{V} \times \mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins} \times \mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V} - \mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V} \times \mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q \times \mathsf{Vt}}{k \times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n} \mathsf{PI}_i \times \mathsf{C}_i)}$$

$$\mathsf{A}' = (1 - \mathsf{E}(1 - \mathsf{Pv}))\mathsf{A}$$

$$q = 1.60218 \times 10^{-19}\mathrm{C}$$

$$k = 1.38066 \times 10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (20 Marks) Short Answer

(*estimated time: 20 minutes*)

Q1a (6 Marks) Delta-Cycle Simulation

In delta-cycle simulation, in which mode do processes start, and why do the VHDL simulation semantics require that processes start in this mode?

Mode: _____

Reason: _____

Q1b (8 Marks) Functional Verification

For each of the two situations below, answer whether the situation is possible. **Briefly justify your answer**

1. The circuit is correct. One of the assertions has a bug. All of the test-vectors pass without any assertion failures.

   Possible Yes ☐ No ☐

2. The circuit is correct. All of the assertions are correct. Some of the test-vectors fail one of the assertions.

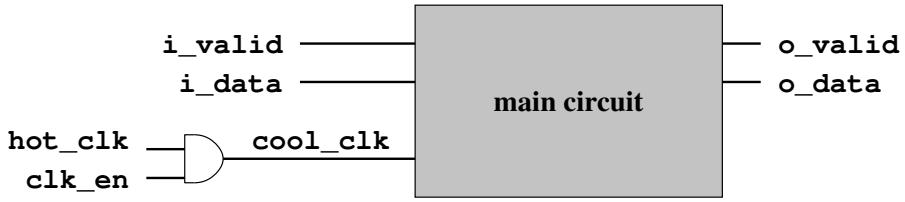
   Possible Yes ☐ No ☐

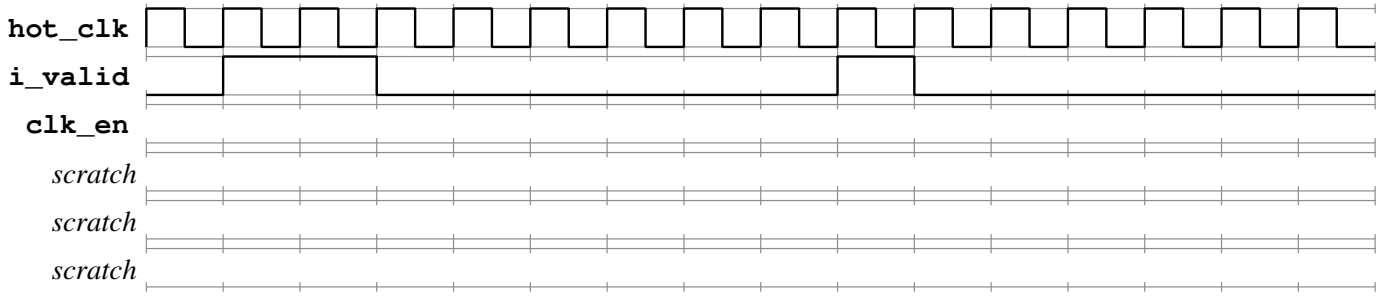
Q1c (6 Marks) Clock Gating

For the system described below, draw the waveform for the `clk_en` signal so that the signal `cool_clk` is turned on for the minimum number of clock cycles such that the main circuit works correctly.

NOTES:

1. The latency through the system is 3 clock cycles.

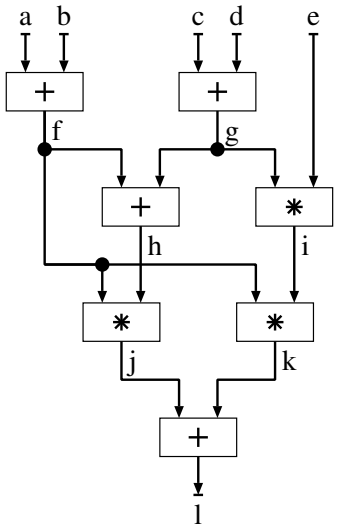




Q2 (20 Marks) Dataflow Diagram

(*estimated time: 30 minutes*)

In this question, you will design and analyze a dataflow diagram for the data-dependency graph below.



NOTES:

1. Timing

Register setup	2 ns
Register hold	1 ns
Register clock-to-Q	3 ns
Clock skew	0.5 ns
Clock jitter	0.7 ns
Clock latency	1 ns
Delay through adder	7 ns
Delay through multiplier	12 ns
Delay through multiplexer	0 ns

2. Requirements
   (a) Registered inputs.
   (b) Combinational outputs.
   (c) The minimum throughput shall be 1/3
3. Goals (from highest priority to lowest)
   (a) Minimize area
      - Order of priority from highest to lowest: Multipliers, adders, inputs, registers.
      - Multiplexers are free
   (b) Minimize clock period
   (c) Minimize latency
4. You shall *not* use any algebraic optimizations, except commutivity, which might be helpful in simplifying the routing of signals.
5. You shall *label all signals*.
6. You do *not* need to do any allocation.

Q2a (15 Marks) Design

Design a dataflow diagram that satisfies the requirements and maximizes the goals listed above.

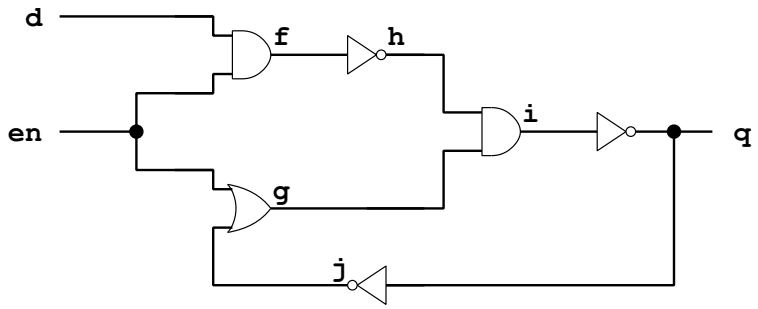
Q2b (5 Marks) Analysis

Number of inputs		Number of multipliers		Latency	
Number of registers		Number of adders		Throughput	
		Number of outputs		Clock period	

Q3 (15 Marks) Latch Analysis

(*estimated time: 15 minutes*)

In this question, you will analyze the circuit below to determine if it is correct implementation of a latch.



NOTES:

1. The delay through each gate is 1 ns.

Q3a (3 Marks) Good or Bad?

	Yes	No
Is the circuit a correct implementation of a latch?	☐	☐

The two remaining parts of this question (Q3b and Q3c) are divided into two columns. Use the left column if you answered *yes*. Use the right column if you answered *no* above.

Q3b (7 Marks) Analysis

If the circuit is a correct implementation of a latch, determine if it is active-high or active-low and calculate the timing parameters below.

Active-high or active-low?	
Clock-to-Q	
Setup	
Hold	

If the circuit is *not* a correct implementation of a latch, explain why.

Q3c (5 Marks) Modification

If the circuit is a correct implementation of a latch, modify the circuit using the diagram below to *decrease the setup time* by 2 ns.

NOTES:

1. You may *not* modify the part of the circuit in the gray rectangle.
2. If you cannot decrease the delay by 2 ns, then decrease the delay to the minimum amount such that the latch still works correctly.

New setup time: ☐

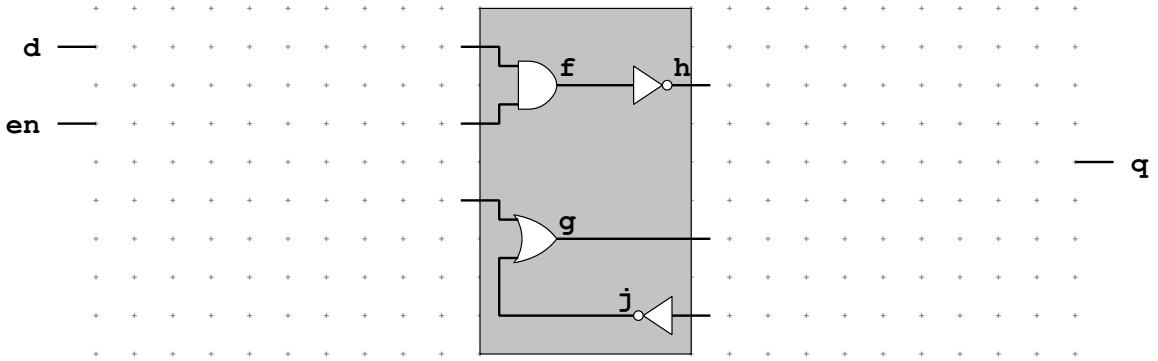
For each of the timing parameters below, answer whether your modification to the latch increases, does not change, or decreases the value of the timing parameter.

	Increase	No change	Decrease
Clock-to-Q	☐	☐	☐
Hold	☐	☐	☐

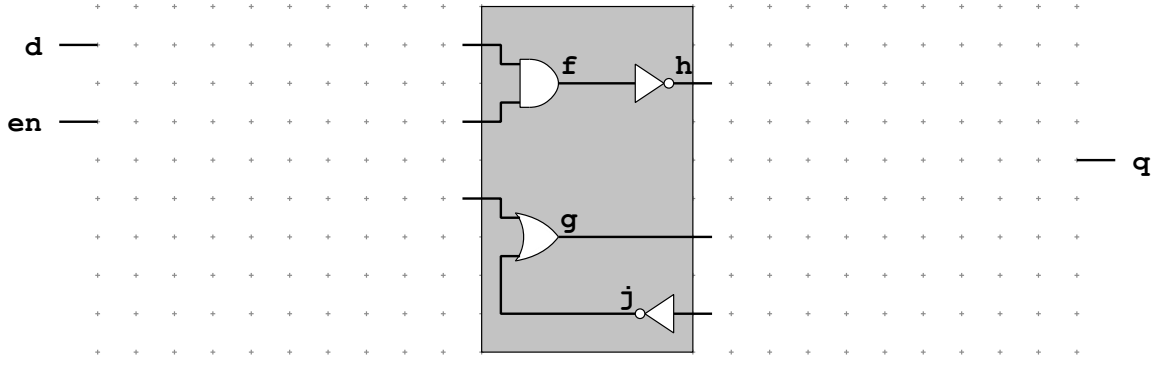
If the circuit is *not* a correct implementation of a latch, modify the circuit using the diagram below to turn it into a correctly functioning latch.

NOTES:

1. Make the minimum modifications necessary.
2. You may *not* modify the part of the circuit in the gray rectangle.



Extra copy for scratch work



Q4 (20 Marks) Critical Path

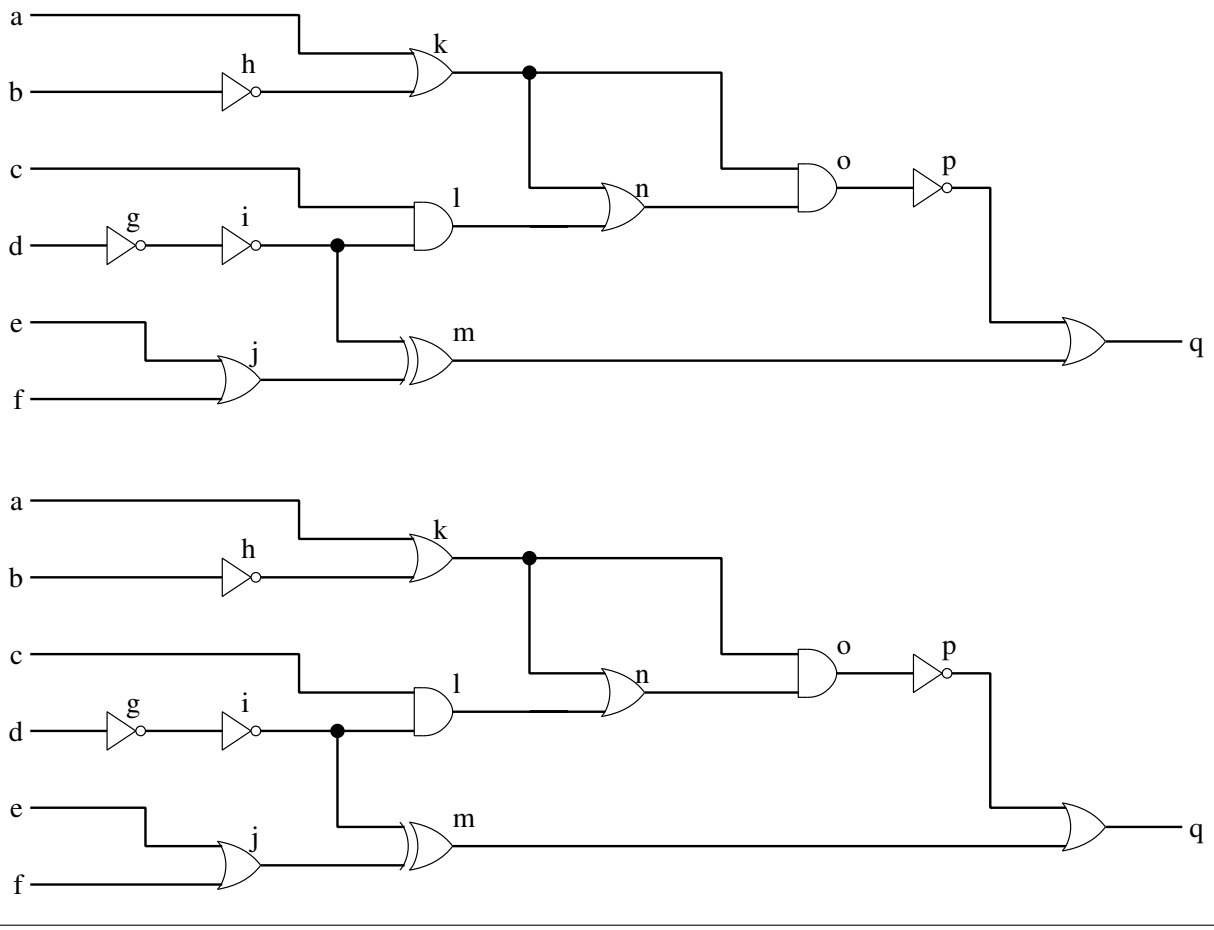
(*estimated time: 30 minutes*)

For the circuit below, the longest path $\langle \mathtt{d}, \mathtt{g}, \mathtt{i}, \mathtt{l}, \mathtt{n}, \mathtt{o}, \mathtt{p}, \mathtt{q} \rangle$ is a false path.

NOTES:

1. Delay through gates: NOT=2, AND=4, OR=4, XOR=6.

Extra copies for scratch work



Q4a (15 Marks) Second-Longest Path

Find the second-longest path and determine if it is a viable path or a false path.

If the second-longest path is *viable*, give a set of values on the primary inputs that will exercise the path.

If the second-longest path is a *false* path, explain why.

NOTES:

1. If there are multiple second-longest paths with the same delay, choose the path that is alphabetically earlier (e.g., if the second-longest paths are $\langle \mathtt{q}, \mathtt{r}, \mathtt{s}, ... \rangle$ and $\langle \mathtt{q}, \mathtt{r}, \mathtt{u}, ... \rangle$, choose $\langle \mathtt{q}, \mathtt{r}, \mathtt{s}, ... \rangle$)

Second-longest path _____ **Viable** ☐ **False** ☐

If viable, excitation: a ☐ b ☐ c ☐ d ☐ e ☐ f ☐

If false, explanation: _____

Q4b (5 Marks) Monotone Speedup

Based upon the two longest paths through the circuit, does this circuit illustrate the benefits of taking into account monotone speedup when determining the critical path? **For full marks, you must justify your answer.**

If you are unable to determine whether this circuit illustrates monotone speedup by analyzing the two longest paths, then explain the concept of monotone speedup and why it is beneficial to take into account monotone speedup when finding the critical path through a circuit.

	Yes	**No**	**Unable to determine**
Based upon the two longest paths, the circuit illustrates the benefits of taking into account the concept of monotone speedup when finding the critical path through a circuit.	☐	☐	☐

Justification, or explanation of monotone speedup:

Q5 (25 Marks) Performance and Power

(*estimated time: 40 minutes*)

Waterluvian filters have become so popular that all of the major microprocessor and FPGA companies offer specialized Waterluvian microprocessors, and there is a standard Waterluvian assembly language. This standardization has caused MIPS/Watt to become the dominant measure of optimality for Waterluvian filters.

You are the design manager for a Waterluvian-processor that is implemented on an FPGA. You are making plans for the next version of your system. Michelle Ips, an engineer on your team, has proposed a performance optimization. Walter Att, another engineer on your team, has proposed a clock-gating scheme. You have the resources to implement only one of the two proposals.

NOTES:

1. Statistics for your current Waterluvian filter:

Supply voltage	1.2 V
Threshold voltage	0.4 V
Area	3000 cells
Activity factor	0.23
Leakage power	100 mW
Short circuiting power	3 mW
Switching power	500 mW
Valid incoming parcels	35 %
Average length of continuous sequence of valid parcels	40
Latency	20 clock cycles
Clock speed	500 MHz

2. The average MIPS/Watt of Waterluvian filters increases by 2% each week.
3. Walter Att's clock-gating scheme will use 200 cells, have no effect on performance, and require 15 weeks of effort. Walter does not yet know the effectiveness of his clock gating scheme.
4. Michelle Ips' performance optimization will increase performance by 95%, have no effect on power, and require 35 weeks of effort.
5. Suggested notation:

W	power (watts)	O_0	original (current) optimality
M	performance (MIPS)	O_1	Walter's optimality
O	optimality (MIPS/Watt)	O_2	Michelle's optimality
t	time	$O_{\text{avg}}(t)$	Average optimality at time t

What is the minimum effectiveness that Walter's clock gating scheme must achieve for it to provide the same MIPS/Watt *relative to the average Waterluvian filter at the time that it will be completed* that Michelle's performance optimization will provide *relative to the average Waterluvian filter at the time that it will be completed*.

If you do not know how to answer the question as stated, you may earn part-marks by using the simplification given below and placing a $\surd$ in the box at the end of the simplification. Using the simplifications will reduce the maximum possible marks to 18.

> I am assuming that my current Waterluvian processor has average optimality now and that Walter's scheme achieves 100% effectiveness. I am solving for the MIPs/Watt that Walter's clock gating scheme will provide *relative to the average Waterluvian filter at the time that it will be completed.* ☐

To ensure that you earn part-marks for all of your correct work, clearly identify the intermediate results that you calculate by drawing a box around them.

Final answer