First Name

Last Name

First letter of last name

UW Userid

E&CE 327 Final

2012t2 (Spring)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the formulas you use and all of your work.
- **The proctors and instructors will not answer questions, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.**
- **Justifications of answers will be marked according to correctness, clarity, and concision.**

			Total Marks	Approx. Time	Page
Q0	!!Almost Free!!		1	0	3
Q1	Dataflow Diagram		20	30	4
Q2	Performance		15	15	6
Q3	Functional Verification		10	10	8
Q4	Latch Analysis		10	10	9
Q5	Critical Path		20	30	10
Q6	Power and Energy		15	20	14
Q7	Clock Gating		10	15	16
Totals			100	130	

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A} \times \mathsf{C} \times \mathsf{V}^2 \times \mathsf{F}) + (\tau \times \mathsf{A} \times \mathsf{V} \times \mathsf{ISh} \times \mathsf{F}) + (\mathsf{V} \times \mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins} \times \mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V} - \mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V} \times \mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q \times \mathsf{Vt}}{k \times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n} \mathsf{PI}_i \times \mathsf{C}_i)}$$

$$\mathsf{A}' = (1 - \mathsf{E}(1 - \mathsf{Pv}))\mathsf{A}$$

$$q = 1.60218 \times 10^{-19}\mathrm{C}$$

$$k = 1.38066 \times 10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

$$(x^y)^z = x^{(yz)}$$

$$(x^y)(x^z) = x^{(y+z)}$$

$$a = b^c \quad \text{is equivalent to:}$$
$$a^{1/c} = b$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (20 Marks) Dataflow Diagram

(*estimated time: 30 minutes*)

In this question, you will design and analyze a dataflow diagram for the equation: $a - (b + c) + (a - b) \times c \times 7 - 3$.

NOTES:

1. Timing

Register setup	2.2 ns
Register hold	1.0 ns
Register clock-to-Q	3.0 ns
Clock skew	0.4 ns
Clock jitter	0.9 ns
Clock latency	0.7 ns
Delay through adder	6.0 ns
Delay through subtracter	7.0 ns
Delay through multiplier	16.0 ns
Delay through multiplexer	0.0 ns

NOTES:

1. Requirements
   (a) Registered inputs.
   (b) Combinational outputs.
   (c) The throughput shall be at least 1/3.
2. Goals (from highest priority to lowest)
   (a) Minimize clock period
   (b) Minimize area
      - Order of priority from highest to lowest: Multipliers, total of adders and subtracters, inputs, registers.
      - Multiplexers are free
   (c) Maximize throughput
3. You may use *algebraic optimizations.*
4. You may schedule the input values to arrive in any order, but you may read each input value only once.
5. You do *not* need to do any allocation.

Q1a (15 Marks) Design

Design a dataflow diagram that satisfies the requirements and maximizes the goals listed above. (There is more space on the next page.)

Q1b (5 Marks) Analysis

Number of inputs

Number of registers

Number of multipliers

Number of adders

Number of subtracters

Number of outputs

Latency

Throughput

Clock period

Q2 (15 Marks) Performance

(*estimated time: 15 minutes*)

With the recent discovery of the Higgs-boson-like particle, you have decided that the next hot area in digital hardware will be to develop filters for detecting and analyzing subatomic particles. You have created a startup company, Bozo Filters Inc, and are working on a new boson-detection filter.

One of your engineers, Olivia, has proposed a performance optimization that will provide a performance gain of 15% compared to the current design, but will delay the project by 10 weeks. The project leader, Claire, wants to stick with her current design. Your task is to choose between option O (Olivia's performance optimization) and option C (Claire's current design).

You do *not* know how much the performance of the average boson-detection filter increases each week, because boson-detection filters are such a new type of product.

Because of the uncertainy in the data (amount of performance gain, delay in schedule, rate of performance increase), you decide that you will pursue Olivia's optimization only if it provides a significant advantage over Claire's current design. More precisely, you decide that you will choose Olivia's optimization only if: the ratio of the performance of Olivia's optimization compared to the average boson filter at the time that Olivia's design is done will be 5% higher than the ratio of the performance of Claire's design compared to the average boson filter at the time that Claire's design is done.

What is the maximum increase in average performance per week for boson filters such that you will choose Olivia's optimization over Claire's current design?

NOTES:

1. Some new equations have been added to the page of "potentially useful information", which might be useful in solving this problem.

Maximum increase in average performance per week

Q3 (10 Marks) Functional Verification

(*estimated time: 10 minutes*)

Your friend, Imran, is a functional verification manager for a secret project. His group is falling behind schedule and he asks you for some advice. His original plan had been to develop assertions, coverage monitors, and reference models for his system, but he now has time for only two of the three tasks. He is considering three options:

Option 1 Assertions and coverage monitors, but no reference models.

Option 2 Assertions and reference models, but no coverage monitors.

Option 3 Coverage monitors and reference models, but no assertions.

Without knowing anything about Imran's system, offer your best advice for how he should choose between the three options.

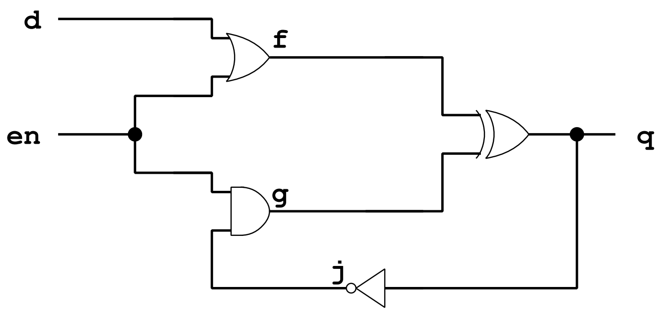
NOTES:

1. Your advice may be conditional based upon potential characteristics of the system. For example, you may write "If you use Altera, then you should choose option 1, because Google has 6.7 million hits for 'altera coverage monitors' but only 0.6 million hits for 'altera reference model' ".

Q4 (10 Marks) Latch Analysis

(*estimated time: 10 minutes*)

In this question, you will analyze the circuit below to determine if it is correct implementation of a latch.



NOTES:

1. The delay through each gate is 1 ns.

Q4a (3 Marks) Good or Bad?

	Yes	No
Is the circuit a correct implementation of a latch?	☐	☐

Q4b (7 Marks) Analysis

This part of the question is divided into two columns. Use the left column if you answered *yes* above. Use the right column if you answered *no* above.

If the circuit is a correct implementation of a latch, determine if it is active-high or active-low and calculate the timing parameters below.

Active-high or active-low?	
Clock-to-Q	
Setup	
Hold	

If the circuit is *not* a correct implementation of a latch, explain why.

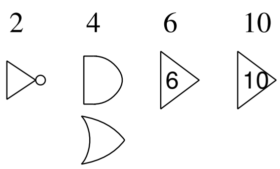
Q5 (20 Marks) Critical Path

(*estimated time: 30 minutes*)

For the circuit below, the longest path ⟨c, g, j, m, n, q, r, s, t⟩ and the second-longest path ⟨c, g, j, k, p, s, t⟩ are both false paths.

NOTES:

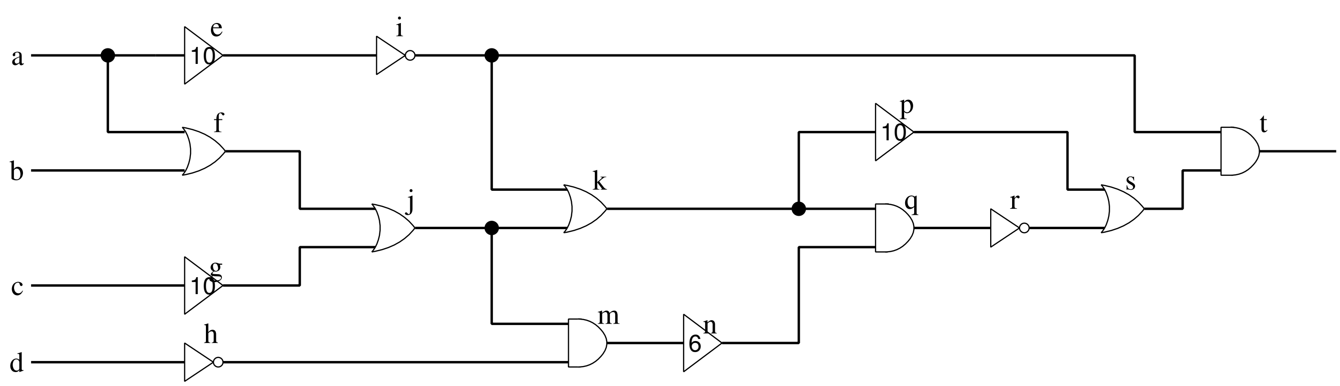
1. A *buffer* is drawn as a triangle with the delay through buffer written inside the triangle. The output of the buffer is simply a delayed version of the input waveform.
2. The delays through the gates are:



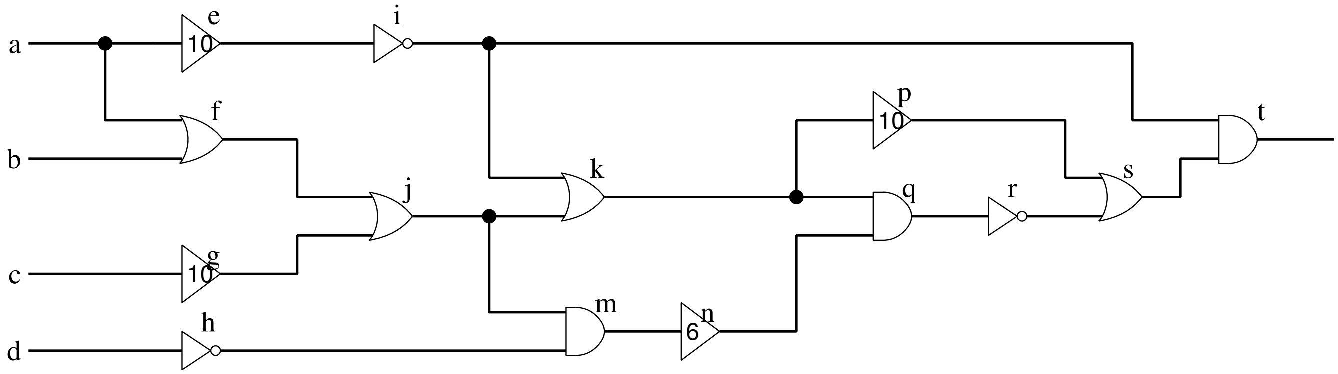
3. The equations for some steady-state (static) conditions:

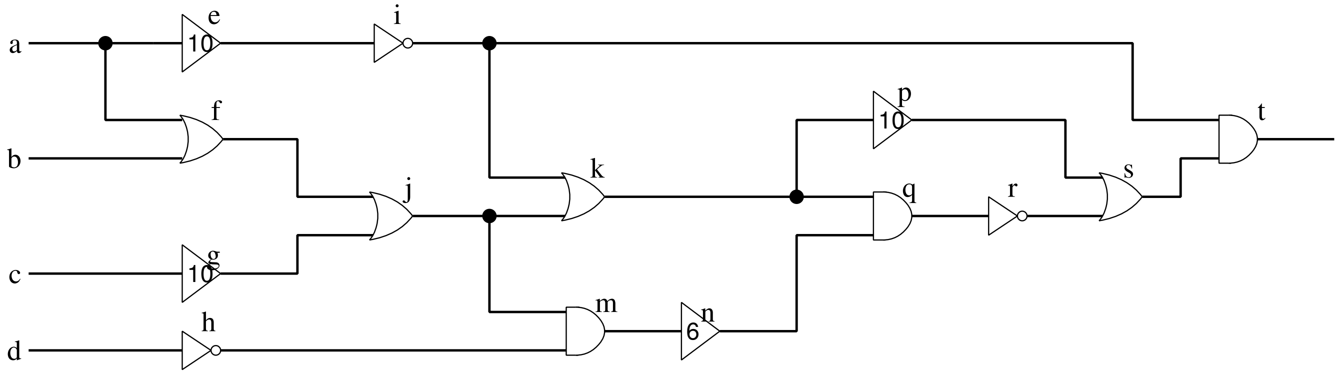
$e = a$	$\overline{e} = \overline{a}$
$f = a + b$	$\overline{f} = \overline{a}\overline{b}$
$g = c$	$\overline{g} = \overline{c}$
$h = \overline{d}$	$\overline{h} = d$
$i = \overline{e}$ $= \overline{a}$	$\overline{i} = a$
$j = f + g$ $= a + b + c$	$\overline{j} = \overline{a}\overline{b}\overline{c}$
$k = i + j$ $= \overline{a} + a + b + c$ $=$ True	$\overline{k} =$ False

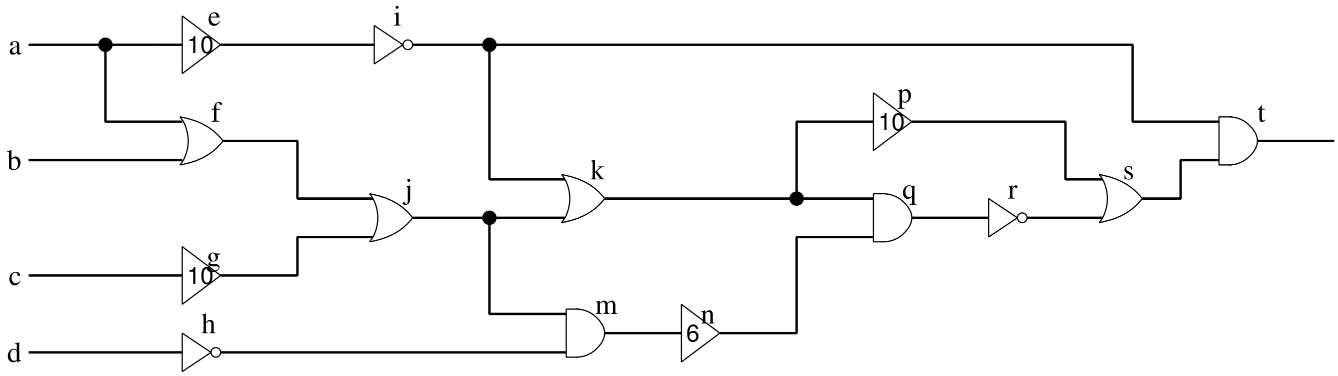
$m = jh$ $= (a + b + c)\overline{d}$	$\overline{m} = \overline{a}\overline{b}\overline{c} + d$
$n = m$ $= (a + b + c)\overline{d}$	$\overline{n} = \overline{a}\overline{b}\overline{c} + d$
$p = k$ $=$ True	$\overline{p} =$ False
$q = kn$ $= (a + b + c)\overline{d}$	$\overline{q} = \overline{a}\overline{b}\overline{c} + d$
$r = \overline{q}$ $= \overline{a}\overline{b}\overline{c} + d$	$\overline{r} = (a + b + c)\overline{d}$
$s = p + r$ $=$ True	$\overline{s} =$ False
$t = is$ $= \overline{a}$	$\overline{t} = a$

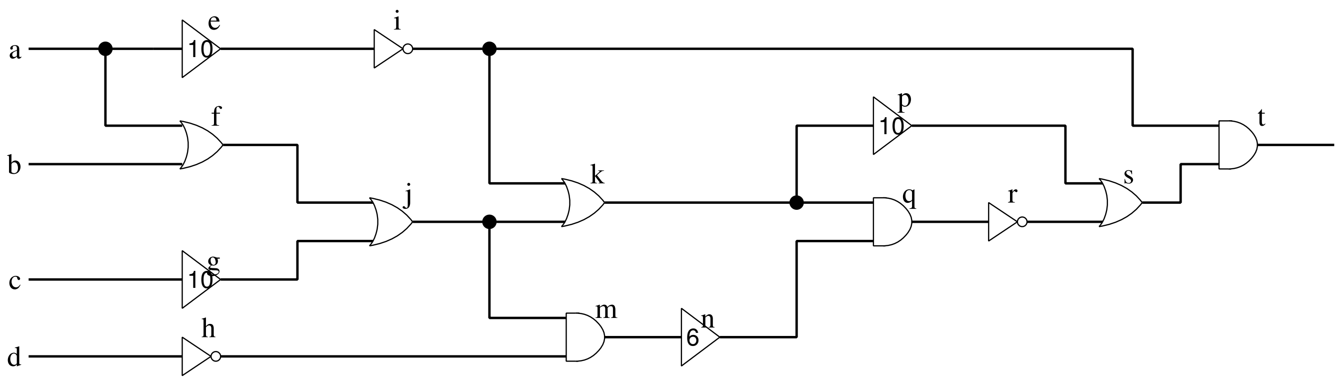


Extra copies for scratch work









Q5a (15 Marks) Third-Longest Path

Find the third-longest path and determine if it is a viable path or a false path.

If the third-longest path is *viable*, give a set of values on the primary inputs that will exercise the path.

If the third-longest path is a *false* path, explain why.

NOTES:

1. If there are multiple third-longest paths with the same delay, choose the path that is alphabetically earlier (e.g., if the third-longest paths are $\langle \texttt{q}, \texttt{r}, \texttt{s}, ... \rangle$ and $\langle \texttt{q}, \texttt{r}, \texttt{u}, ... \rangle$, choose $\langle \texttt{q}, \texttt{r}, \texttt{s}, ... \rangle$)
2. The answer shall be written on the next page.

		Viable	**False**
Third-longest path	____________	☐	☐

	a	b	c	d
If viable, excitation:	☐	☐	☐	☐

If false, explanation: ______________________

Q5b (5 Marks) Monotone Speedup

Based upon the three longest paths through the circuit, does this circuit illustrate the benefits of taking into account monotone speedup when determining the critical path? **For full marks, you must justify your answer.**

If you are unable to determine whether this circuit illustrates monotone speedup by analyzing the three longest paths, then explain the concept of monotone speedup and why it is beneficial to take into account monotone speedup when finding the critical path through a circuit.

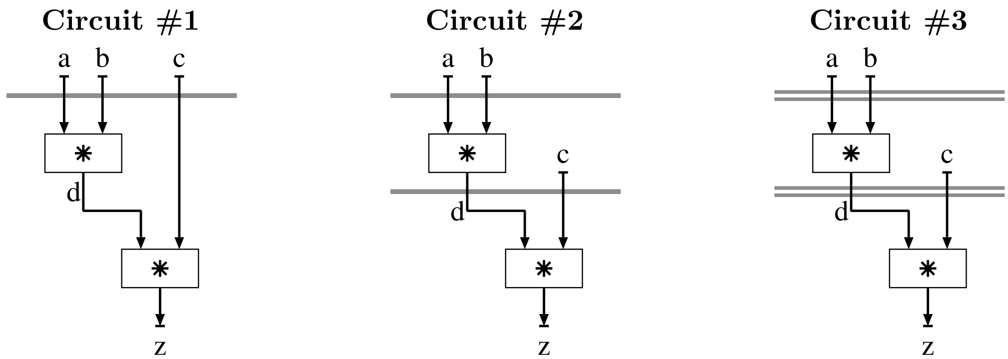
	Yes	**No**	**Unable to determine**
Based upon the three longest paths, the circuit illustrates the benefits of taking into account the concept of monotone speedup when finding the critical path through a circuit.	☐	☐	☐

Justification, or explanation of monotone speedup:

Q6 (15 Marks) Power and Energy

(*estimated time: 20 minutes*)

In this question, you will compare the power and energy consumption of three different circuits that implement the equation $z = a \times b \times c$.



NOTES:

1. All three circuits use the same type of FPGA chip.
2. Each of three circuits is run at its maximum clock speed and maximum throughput.
3. The areas and delays of input ports, output ports, registers, and multiplexers are much less than the area of a multiplier.

Q6a (10 Marks) Power Comparison

Compare the *power consumption* of the circuits by writing one of "<", "=", or ">" in each box below. **For full marks, you must justify your answer.**

Circuit 1	☐	Circuit 2
Circuit 2	☐	Circuit 3

Q6b (5 Marks) Energy Comparison

Compare the *energy consumption per parcel* of circuits 2 and 3 by writing one of "<", "=", or ">" in the box below. **For full marks, you must justify your answer.**

Circuit 2 ☐ Circuit 3

Q7 (10 Marks) Clock Gating

(*estimated time: 15 minutes*)

You are designing a clock-gating scheme for a Kirsch edge detector.

NOTES:

1. For adjacent pixels on the *same row* of the image, there are exactly 3 bubbles between valid pixels.
2. At the *end of a row*, there are exactly 100 bubbles before the first valid pixel of the next row.
3. At the *end of an image*, there are exactly 100 bubbles before the first valid pixel of the next image.
4. The latency is 8 clock cycles.
5. The image size is 64×64 pixels.

What is the absolute *minimum* power consumption that you could achieve with clock-gating, as a percentage of the edge-detector's original power?

If you do not know how to answer the question as stated, you may earn part-marks (maximum of 7) by assuming that there are *no bubbles between valid pixels in the same row* (*i.e.*, the system is fully pipelined) and placing a √ in the box. ☐

List any assumptions that you make (*e.g.*, "frictionless surfaces and point masses"):

Analysis:

Power consumption with clock gating ☐