First Name _____ Last Name _____ First letter of last name [ ]

UW Userid _____

ECE 327 Final

2013t1 (Winter)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the formulas you use and all of your work.
- **The proctors and instructors will not answer questions, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.**
- **Justifications of answers will be marked according to correctness, clarity, and concision.**

			Total Marks	Approx. Time	Page
Q0	!!Almost Free!!		1	0	3
Q1	Simulation		10	5	4
Q2	Area Analysis		10	10	5
Q3	Pipelining		10	15	6
Q4	Performance		20	30	7
Q5	Timing Analysis		20	30	9
Q6	Energy Model		15	20	11
Q7	Clock Gating		15	20	13
Totals			100	130	

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A} \times \mathsf{C} \times \mathsf{V}^2 \times \mathsf{F}) + (\tau \times \mathsf{A} \times \mathsf{V} \times \mathsf{ISh} \times \mathsf{F}) + (\mathsf{V} \times \mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins} \times \mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V} - \mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V} \times \mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q \times \mathsf{Vt}}{k \times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n} \mathsf{PI}_i \times \mathsf{C}_i)}$$

$$\mathsf{A}' = (1 - \mathsf{E}(1 - \mathsf{Pv}))\mathsf{A}$$

$$q = 1.60218 \times 10^{-19}\mathrm{C}$$

$$k = 1.38066 \times 10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

$$(x^y)^z = x^{(yz)}$$

$$(x^y)\,(x^z) = x^{(y+z)}$$

$$a = b^c \quad \text{is equivalent to:}$$
$$a^{1/c} = b$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (10 Marks) Simulation

(*estimated time: 5 minutes*)

Q1a (5 Marks) Advantage of Delta-Cycle Simulation

What is the most significant advantage of delta-cycle simulation over RTL simulation, and how does delta-cycle simulation achieve this advantage?

Advantage: _____

Achieved by: _____

Q1b (5 Marks) Advantage of RTL Simulation

What is the most significant advantage of RTL simulation over delta-cycle simulation, and how does RTL simulation achieve this advantage?

Advantage: _____

Achieved by: _____

Q2 (10 Marks) Area Analysis

(*estimated time: 10 minutes*)

Calculate the mininum number of FPGA cells needed to implement the VHDL code below.

NOTES:

1. The signal `a` is `std_logic`.
2. The signals `b`, `c`, `d`, `e`, and `z` are 12-bit `unsigned`.
3. Each FPGA cell has a 4:1 LUT with carry-in and carry-out signals, and a 1-bit register. All four of the normal inputs to the LUT may be used at the same time as the carry-in signal to the LUT.
4. For full marks, you must justify your answer with a drawing and/or text.

```
process begin
  wait until rising_edge(clk);
  if a='1' then
    z <= b+c+d;
  else
    z <= b+e+d;
  end if;
end process;
```

Number of FPGA cells: ☐

Justification:

Q3 (10 Marks) Pipelining

(*estimated time: 15 minutes*)

In this question, you will optimize the dataflow diagram below. First, try to find an optimization that satisfies Option 1 below. If it is impossible to satisfy the goals of Option 1, then find an optimization that satisfies the goals of Option 2.

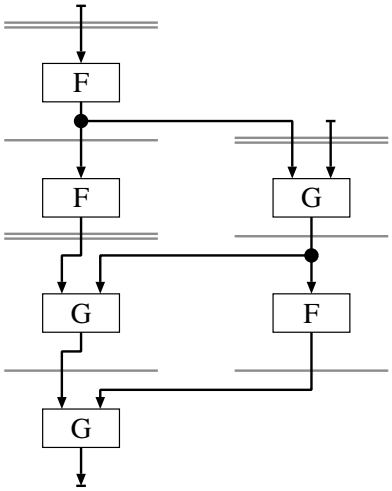
Option 1 Increase throughput *without* any increase in latency, clock period, or area.

Option 2 Optimization goals in order of decreasing importance:

1. Minimum clock period
2. Minimum area; in order of decreasing importance: F, G, Registers, Inputs, Multiplexers
3. Maximum throughput
4. Minimum latency

NOTES:

1. Draw the optimized DFD in the space to the left of the original DFD.
2. Compare the original and optimized DFDs by filling in the tables below the DFDs.
3. Inputs shall be registered, outputs shall be combinational.
4. The function `G` is commutative.
5. The only algebraic optimization that is allowed is commutativity.



	Yes	No
Optimization option 1 is possible	☐	☐

	Original	Optimized
Latency		
Throughput		
Number of F		
Number of G		
Number of registers		
Number of inputs		

In the optimized column, for aspects (*e.g.*, latency) of the optimized dataflow diagram that are the same as the original dataflow diagram, write "Same".

Q4 (20 Marks) Performance

(*estimated time: 30 minutes*)

You work for Inchworm Productions, a company that designs Waterluvian filters. You just released your current product, which has below average performance. Your manager has asked you to analyze the performance gains needed for the performance of future Inchworm products to be 10% above average in two years.

NOTES:

1. The average performance of Waterluvian filters doubles every 18 months.
2. The average Waterluvian filter now is 20% faster than the current Inchworm product.

By what percentage must your performance increase each year so that the product you release in two years will be 10% faster than the average Waterluvian filter in two years?

Worksheet continues on next page

Performance increase each year:

Q5 (20 Marks) Timing Analysis

(*estimated time: 30 minutes*)

You have just been promoted to a research and development group working on a new cell library for ASICs (*e.g.*, implementations of AND gates, OR gates, flip-flops, *etc.*).

Your new group does not yet have a product, but they already have hired a branding consultant who has come up with a name, "Precidel" (for "precise delay") and a slogan: "*Precidel: same delay, every day*".

The goal of the Precidel cell library is to eliminate the variability in delay through gates. For example, each Precidel AND gate will always have a delay of precisely 1.0 ns.

Normal (*i.e.*, non-Precidel) gates have variability in delay. Due to manufacturing tolerances, there is variability in delay across different AND gates (*e.g.*, one AND gate will have a delay of 1.1 ns and another will have a delay of 0.9 ns). Due to changes in supply voltage and temperature there is variability in delay across time for an individual gate (*e.g.*, today a particular AND gate has a delay of 1.1 ns and tomorrow the same gate will have a delay of 0.9 ns).

Your job is to work on the timing analysis tool for Precidel circuits. Your first task is to choose a definition for *viability*. Your manager has given you three possible definitions of viability to choose from:

A : A path is viable *if-and-only-if* for each gate along the path:
the side input has a non-controlling value.

B : A path is viable *if-and-only-if* for each gate along the path:
the side input has a non-controlling value
or the side input arrives late and the path input has a controlling value

C : A path is viable *if-and-only-if* for each gate along the path:
the side input arrives early and has a non-controlling value
or the side input arrives late and the path input has a controlling value

Worksheet is on next page

Which definition (A–C) is the best choice for the definition of viability for Precidel circuits? [ ]

Justify your answer by describing the most significant advantage of your chosen definition over each of the other two definitions.

My choice is better than [ ] because:

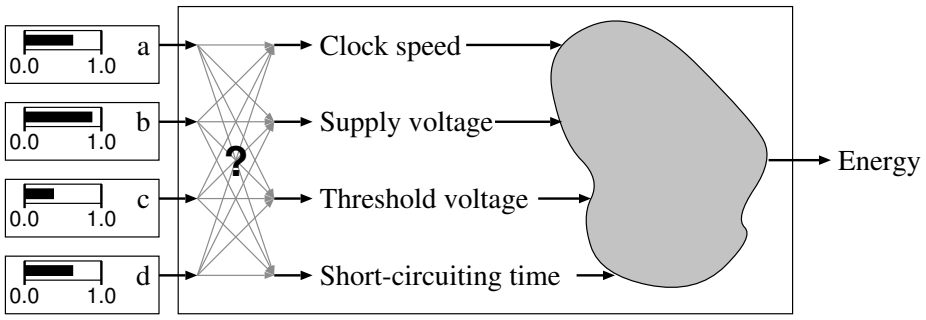
My choice is better than [ ] because:

Q6 (15 Marks) Energy Model

(*estimated time: 20 minutes*)

You have just started your co-op job at Silicon Waffles, a startup company working on a new power and energy analysis tool. The previous co-op student wrote a program to calculate the *total energy consumption* of a 6-bit one-hot counter for six clock cycles. The model is functionally correct, but the program is written so poorly that no one can understand it. Your job is to reverse engineer the meaning of the input variables by running the program and examining the output.

The inputs are named `a`, `b`, `c`, and `d`. These inputs control the circuit parameters of clock speed, supply voltage, threshold voltage, and short-circuiting time. But, no one knows which input corresponds to which circuit parameter:



The inputs `a`, `b`, `c`, and `d` are scaling factors that range between 0.0 and 1.0. Each scaling factor controls the value of a circuit parameter: 0.0 = minimum realistic value, 0.5 = average value, 1.0 = maximum realistic value.

For example, if this was a model for the amount of pollution generated by a vehicle on a highway and the parameter for vehicle speed ranged from 80 km/hr to 120 km/hr, then the relationship between the input and speed would be as follows:

input	speed
1.0	120 km/hr
0.5	100 km/hr
0.0	80 km/hr

The output value for energy consumption ranges between 0 and 1000.

It easy to run many tests and analyze the results, because it takes less than 2 seconds to run the program for a given set of input values.

Your answer shall describe a sequence of steps that you could use to determine which input corresponds to which circuit parameter.

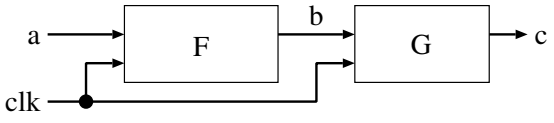
An example answer that is in the correct format, but has no helpful technical content:

1. Run a series of tests that gradually increase the inputs together from 0.0 to 1.0.
2. If energy consumption increases as the variables increase, then threshold voltage = a, because "a" is the first letter in "aagaard". Otherwise, threshold voltage = d, because "d" is the last letter in "aagaard".
3. Set the input for threshold voltage to 1.0. For each of the remaining three inputs, make the chosen input oscilate as a sine wave and hold the other inputs constant at 0.5. The input that causes the energy consumption to oscilate corresponds to clock speed.

Q7 (15 Marks) Clock Gating

(*estimated time: 20 minutes*)

In this question you will analyze the potential power savings of a clock gating scheme for the system below.



	F	**G**
Latency	15	20
Throughput	1	1
Area	200	180
Activity factor	0.20	0.30
Supply voltage	1.2 V	1.2 V
Clock speed	500 MHz	500 MHz

Calculate the maximum percentage of power of the original system that could be saved with a clock gating scheme is 90% effective.

NOTES:

1. The typical sequence of inputs is 25 valid parcels followed by 55 bubbles.
2. You may use either a single clock-enable state machine for both F and G, or one clock enable state machine for F and one for G. If you use two clock enable state machines, each state machine is 90% effective for the circuit (F or G) whose clock it enables.

Worksheet continues on next page

Percentage of power that is saved: