First Name _____ Last Name _____ First letter of last name [ ]

UW Userid _____

ECE 327 Final

2014t1 (Winter)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the formulas you use and all of your work.
- **The proctors and instructors will not answer questions, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.**
- **Justifications of answers will be marked according to correctness, clarity, and concision.**

			Total Marks	Approx. Time	Page
Q0	!!Almost Free!!		1	0	3
Q1	Simulation		5	7	4
Q2	Retiming		10	18	5
Q3	Dataflow Diagram Design		20	20	7
Q4	Optimality		15	20	9
Q5	Longest Path		10	15	11
Q6	Glitches		10	15	13
Q7	Power and Performance		15	20	14
Q8	Clock Gating		15	20	16
Totals			100	135	

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A} \times \mathsf{C} \times \mathsf{V}^2 \times \mathsf{F}) + (\tau \times \mathsf{A} \times \mathsf{V} \times \mathsf{ISh} \times \mathsf{F}) + (\mathsf{V} \times \mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins} \times \mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V} - \mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V} \times \mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q \times \mathsf{Vt}}{k \times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n} \mathsf{PI}_i \times \mathsf{C}_i)}$$

$$\mathsf{A}' = (1 - \mathsf{E}(1 - \mathsf{Pv}))\mathsf{A}$$

$$q = 1.60218 \times 10^{-19}\mathrm{C}$$

$$k = 1.38066 \times 10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

$$(x^y)^z = x^{(yz)}$$

$$(x^y)\,(x^z) = x^{(y+z)}$$

$$a = b^c \quad \text{is equivalent to:}$$
$$a^{1/c} = b$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (5 Marks) Simulation

(*estimated time: 7 minutes*)

What would happen if you tried to use the register-transfer-level simulation algorithm to simulate a circuit that the algorithm could not simulate? Obviously there will be a problem. Describe where in the simulation algorithm a problem will first occur and describe what the problem will be.

Example:

> The problem will first occur when the simulation time is incremented to 3.14159265358979323846 ns.
>
> The computer running the simulation will be teleported to Kepler-186f.

The problem will first occur: _____

Description of problem: _____

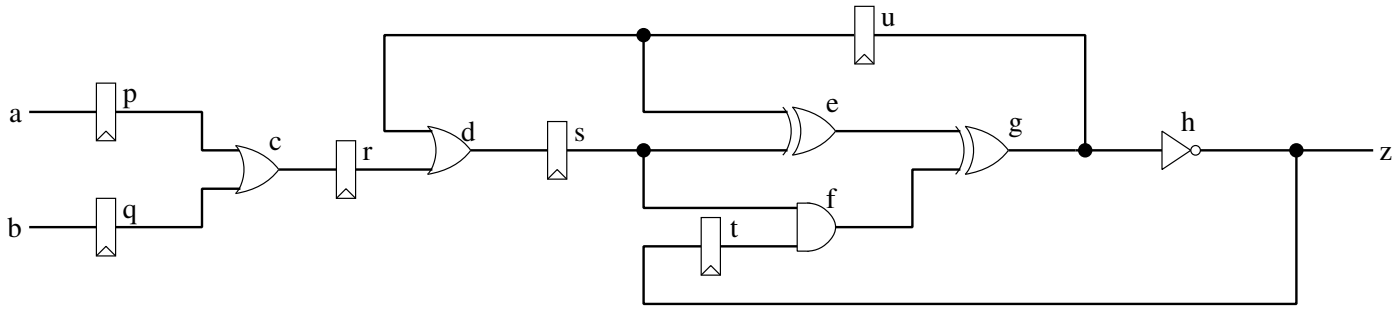
Q2 (10 Marks) Retiming

(*estimated time: 18 minutes*)

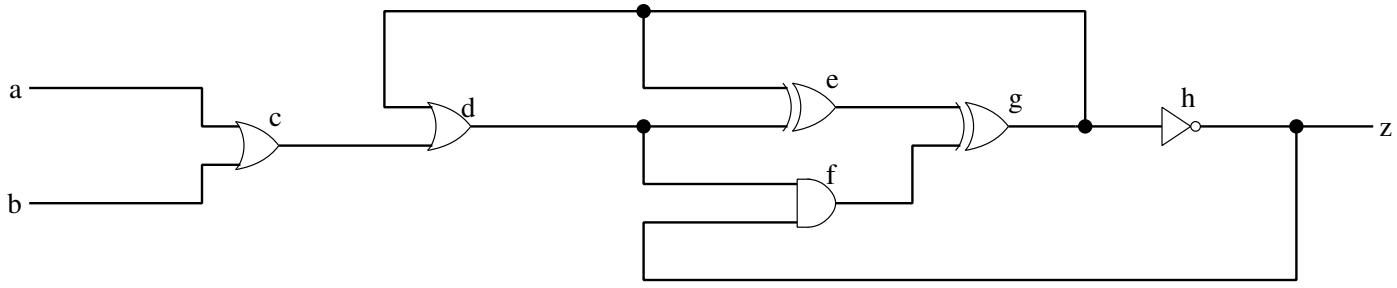
Use retiming to modify the circuit below without changing the behaviour of the output `z`.

NOTES:

1. Goals, in order of *decreasing* importance:
   (a) Minimize the number of registers in the circuit.
   (b) Make `z` be the output of a register.
2. The inputs and combinational gates shall *not* be modified.

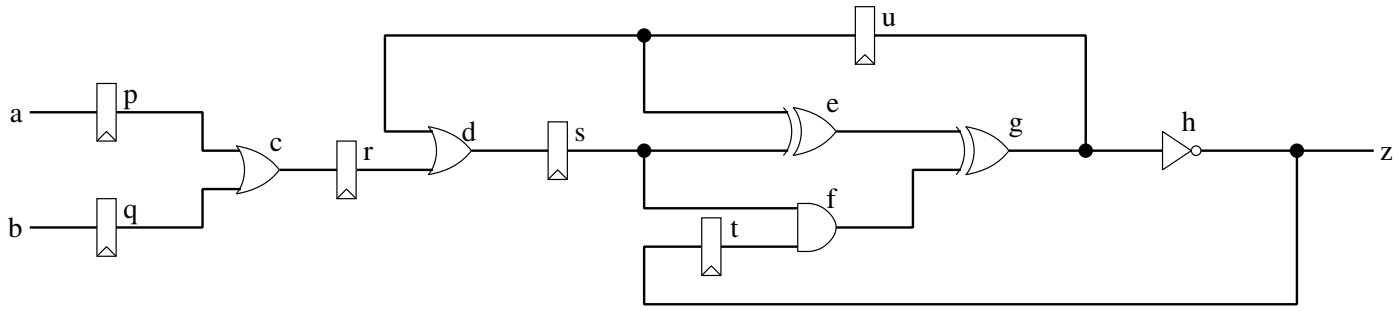


Draw the flip-flops after retiming:



Extra copies of figure are on next page

Extra copy for scratch work



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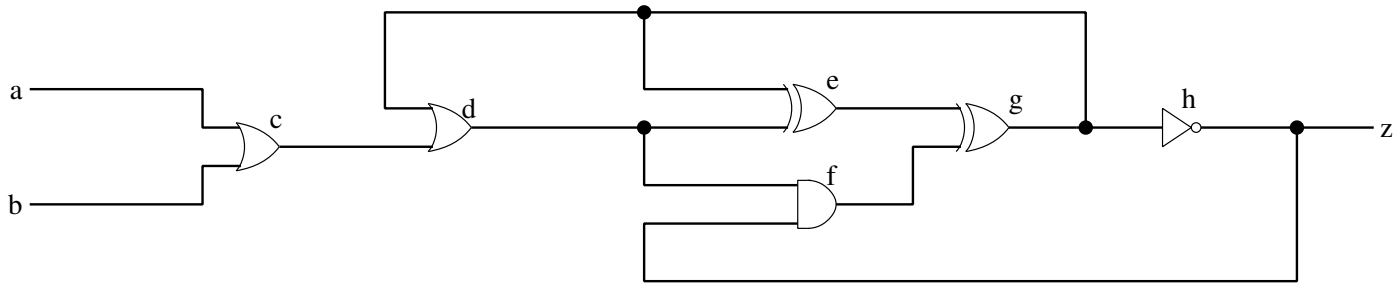

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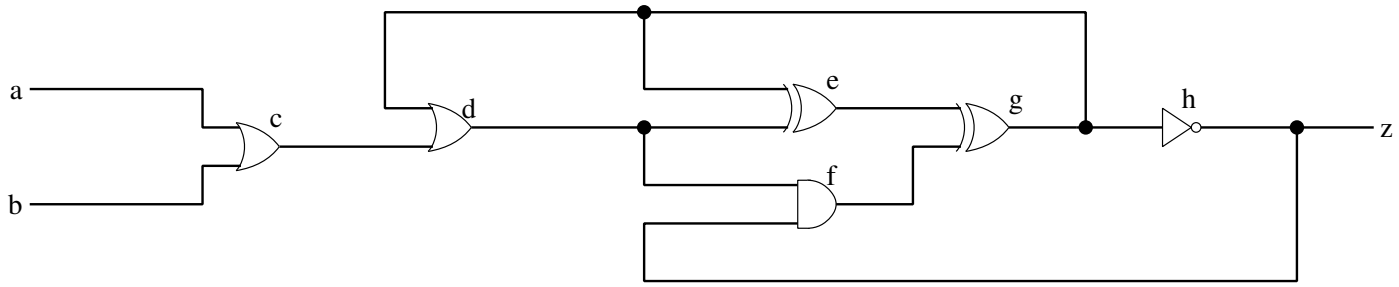


Q3 (20 Marks) Dataflow Diagram Design

(*estimated time: 20 minutes*)

Draw a dataflow diagram for the system described below:

```
M[b+c] = a;
     p = M[d];
     z = p + e + f;
```

NOTES:

1. The inputs are `a`, `b`, `c`, `d`, `e`, and `f`.
2. It is guaranteed that `b+c` $\neq$ `d`.
3. The output is `z`.
4. The *inputs* shall be registered.
5. The *output* may be either registered or combinational.
6. The memory shall be *single-ported*.
7. Optimization goals, in order of *decreasing* importance:
   (a) Maximum *throughput*
   (b) Minimum number of *inputs*
   (c) Minimum *latency*
   (d) Minimum number of *adders*
   (e) Minimum number of *registers* (*excluding memory*)
   (f) Minimum *clock period*
8. You may use *algebraic optimizations*, as long as the values of `z` and `M` are correct.
9. Memory read, memory write, and a 2-input adder all have the same delay of t.
10. The memory shall have registered inputs and combinational outputs (same as in class).
11. Input values may be read in any clock cycle, but each input value shall be read exactly once.
12. You do *not* need to do any allocation.

Work space is on the next page

Latency		Number of inputs	
Throughput		Number of registers	
Clock period		Number of adders	

Q4 (15 Marks) Optimality

(*estimated time: 20 minutes*)

For Waterluvian filters, optimality is a ratio of the number of pixels produced and the resources (time and hardware) used to produce the pixels:

$$Opt = \frac{Pixels}{Time \times Hardware}$$

From this basic concept, we can define different versions of optimality using different measures of time and hardware.

The *consumers' measure of optimality* for Waterluvian filters is the number of pixels produced per second by a Waterluvian chip:

$$\begin{aligned} Opt_c &= \text{consumers' measure of optimality} \\ &= \frac{Pixels}{Sec \times Chip} \end{aligned}$$

As the size of transistors decreases with each new generation of chips:

- The delay through an FPGA cell decreases
- The number of cells per chip increases

We define the *design optimality* as a measure that is independent of the characteristics of a particular FPGA chip. For design optimality:

- The base unit of time is the delay through a single FPGA cell.
- For area, we count the number of FPGA cells that the Waterluvian filter uses.

$$\begin{aligned} D &= \text{delay through a single FPGA cell} \\ Opt_d &= \text{design optimality} \\ &= \frac{Pixels}{D \times Cells} \end{aligned}$$

Using the data below, calculate the average *percentage change in design optimality per month* for Waterluvian filters.

- Consumer's optimality increases by 2.5% per month
- Delay through an FPGA cell decreases by 1% per month
- Number of cells per chip doubles every 2 years

Work space is on next page

Percentage change in design optimality per month [ ]

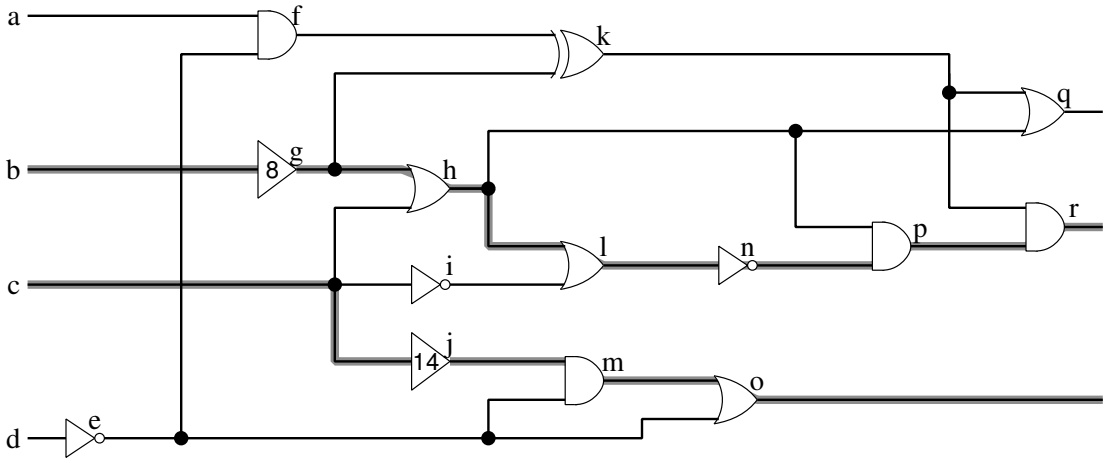
Q5 (10 Marks) Longest Path

(*estimated time: 15 minutes*)

In the circuit below, the two longest paths, $\langle \mathtt{b}, \mathtt{g}, \mathtt{h}, \mathtt{l}, \mathtt{n}, \mathtt{p}, \mathtt{r} \rangle$ and $\langle \mathtt{c}, \mathtt{j}, \mathtt{m}, \mathtt{o} \rangle$ are false paths. Find the third longest path.

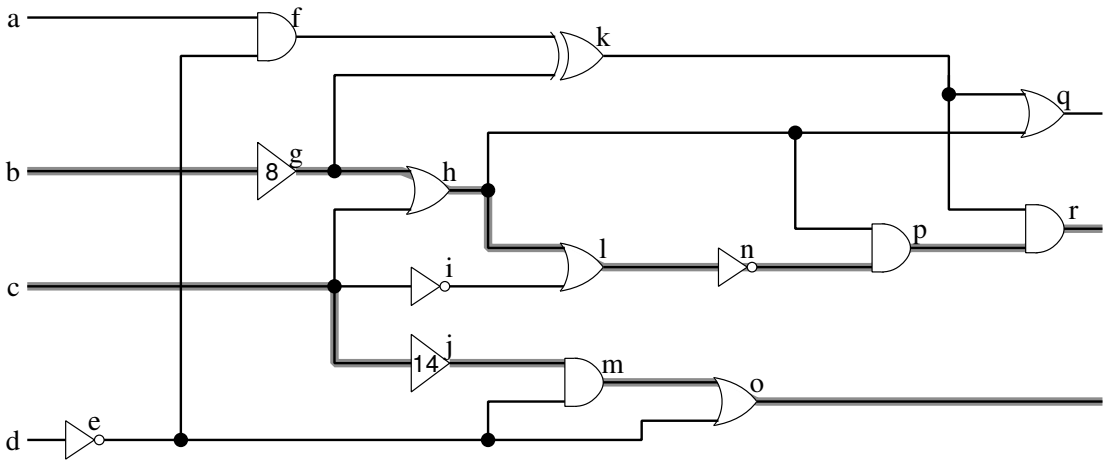
NOTES:

1. A *buffer* is drawn as a triangle with its delay written inside the triangle. The output of the buffer is simply a delayed version of the input.



Additional copy of circuit and work space on next page

Extra copy for scratch work



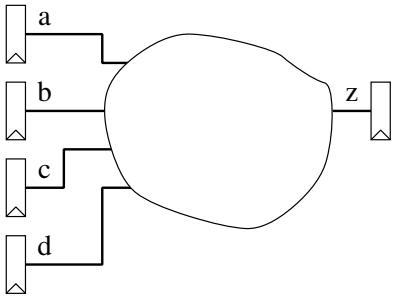
Q6 (10 Marks) Glitches

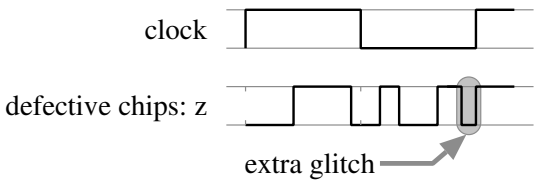
(*estimated time: 15 minutes*)

You have begun to manufacture a new circuit, but a few of the chips are defective. The post-silicon verification engineers have identified that the defective chips have a setup violation on the critical path.

NOTES:

1. The critical path is from `b` to `z`. The specific gates in the circuit are irrelevant to this question.
2. The critical path was found by running timing simulation for all possible excitations of each combinational path using the maximum delay of each gate. (This complete simulation was feasible because it is a small circuit.)
3. The setup violation is the extra glitch in the waveform below, which does not occur in timing simulation with maximum delays or with correct chips.





What is the most likely cause of the extra glitch? **For full marks, you must justify your answer.**

Q7 (15 Marks) Power and Performance

(*estimated time: 20 minutes*)

You are the project leader for a Waterluvian filter and are planning to switch to a new FPGA chip.

Summary of characteristics of new and old FPGA chips:

Characteristic	**Ratio of value on New FPGA to Old FPGA**
Capacitance per cell	0.20
Area per cell	0.25
Delay per cell	0.30
Supply voltage	1.00

Your task is to determine the maximum performance gain that you can achieve by switching to the new FPGA chip.

NOTES:

1. Performance is measured in mega-pixels per second.
2. The only change that you may make to your design is to adjust (add, delete, and/or move) clock cycle boundaries.
3. The *total power consumption* (Watts) and the *power density* (Watts per mm^2) must stay the same or decrease when you switch to the new FPGA chip.

   If you do not know how calculate the power density, you may earn *part marks* by writing a $\surd$ in the box below and ignoring power density.

   I am ignoring power density. ☐

Work space is on next page

1. List any assumptions you need:

2. What is the maximum performance gain that can be achieved?

Maximum performance gain

3. What is the primary limitation to further increases in performance?

Q8 (15 Marks) Clock Gating

(*estimated time: 20 minutes*)

After 16-months of covert surveillance of Piazza groups, Interpol has determined that a professor at an obscure Canadian university outside of Toronto is using Waterluvian filters to make counterfeit Bitcoins. Because of your expertise in Waterluvian filters, you have been hired by Interpol to infiltrate this criminal organization and pose as the project leader for the next generation Waterluvian filter.

An intern from some other university was assigned the task of adding clock-gating to the Waterluvian filter. When doing the power analysis, the component *without* clock gating has lower power than the component *with* clock gating. Unfortunately, the intern has now returned to school and the organization's policy prevents any communication with students once they have finished their employment.

NOTES:

1. The two components are identical except for the addition of clock gating.
2. Both components were analyzed for the same FPGA chip, clock speed, and supply voltage.
3. The clock gating is functionally correct.

Based only upon the information above, give two hypotheses for the most likely reason that adding clock gating caused the power consumption to increase.

Hypothesis 1:

Hypothesis 2:

Describe how you could determine the reason that the power increased. Your analysis may use the simulation and synthesis tools you used in ece327 (*e.g.*, the uw-* scripts with Modelsim, Precision-RTL, and Quartus).