First Name

Last Name

First letter of last name

UW Userid

ECE 327 Final

2014t2 (Spring)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the formulas you use and all of your work.
- **The proctors and instructors will not answer questions, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.**
- **Justifications of answers will be marked according to correctness, clarity, and concision.**

			Total Marks	Approx. Time	Page
Q0	!!Almost Free!!		1	0	3
Q1	Dataflow Diagram		20	25	4
Q2	Allocation and Control		20	30	6
Q3	Latch Design and Analysis		15	20	9
Q4	Elmore		15	20	11
Q5	Power and Performance		15	20	13
Q6	Clock Gating		15	20	15
Totals			100	135	

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A}\times\mathsf{C}\times\mathsf{V}^2\times\mathsf{F}) + (\tau\times\mathsf{A}\times\mathsf{V}\times\mathsf{ISh}\times\mathsf{F}) + (\mathsf{V}\times\mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins}\times\mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V}-\mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V}\times\mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q\times\mathsf{Vt}}{k\times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n}\mathsf{PI}_i\times\mathsf{C}_i)}$$

$$\mathsf{A}' = (1-\mathsf{E}(1-\mathsf{Pb}))\mathsf{A}$$

$$q = 1.60218\times10^{-19}\mathrm{C}$$

$$k = 1.38066\times10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

$$(x^y)^z = x^{(yz)}$$

$$(x^y)(x^z) = x^{(y+z)}$$

$$a = b^c \quad \text{is equivalent to:}$$
$$a^{1/c} = b$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (20 Marks) Dataflow Diagram

(*estimated time: 25 minutes*)

In this question, you will design and analyze a dataflow diagram for the equation:

$$a+b+c+10-3\times a\times b-3\times b\times c$$

NOTES:

1. Requirements:
   (a) Registered inputs.
   (b) Combinational outputs.
   (c) The throughput shall be at least 1/3.
2. Goals, from highest priority to lowest:
   (a) Minimize clock period
   (b) Minimize area, from highest priority to lowest:
      • Multipliers
      • Adders and subtracters
      • Inputs
      • Registers
      • *Multiplexers are free*
   (c) Maximize throughput
3. You may use *algebraic optimizations*.
4. You may schedule the input values to arrive in any order, but you may read each input value only once.
5. You do *not* need to do any allocation.

On the next page, draw a dataflow diagram that satisfies the requirements and is optimized according to the goals above.

Q2 (20 Marks) Allocation and Control

(*estimated time: 30 minutes*)

This question examines the implementation of a dataflow diagram.

Q2a: perform allocation and draw a control table

Q2b: choose a state encoding

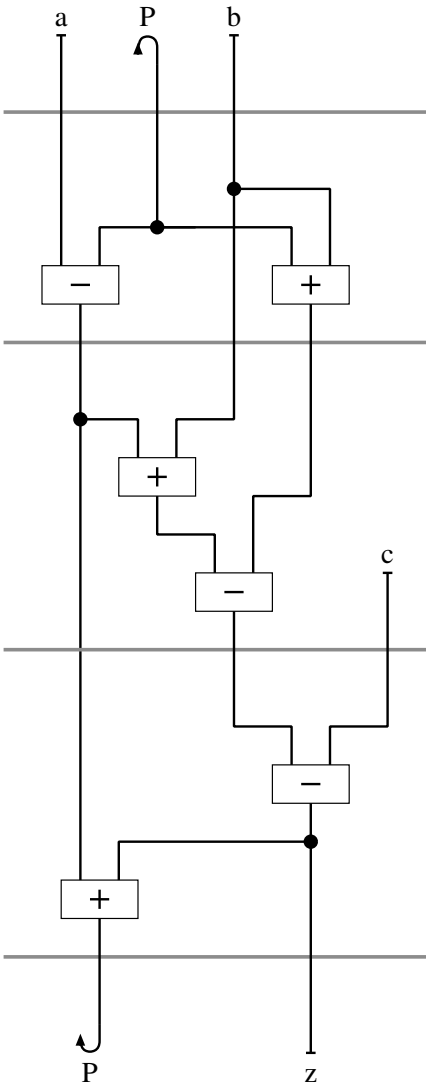
Q2c: write VHDL code for the datapath registers

Q2a (10 Marks) Allocation and Control Table

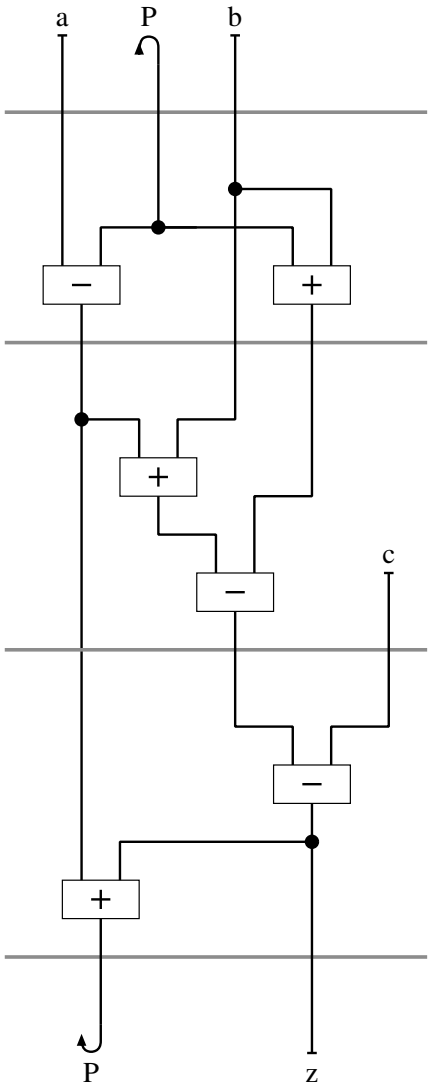
For the dataflow diagram on the next page: perform input/output allocation, datapath allocation, and register allocation; then draw the control table.

NOTES:

1. You may use 2:1 multiplexers, and may combine 2:1 multiplexers to create larger multiplexers.
2. The optimization goals, in order of highest priority to lowest, are to minimize the number of:
   (a) Input ports
   (b) Output ports
   (c) Registers
   (d) Adders
   (e) Subtracters
   (f) 2:1 multiplexers and chip enables
3. You shall *not* perform scheduling optimizations on the dataflow diagram.
4. The *only* algebraic optimization that you may perform is *commutativity*.
5. You shall *not* perform don't-care instantiation



Extra copy for scratch work



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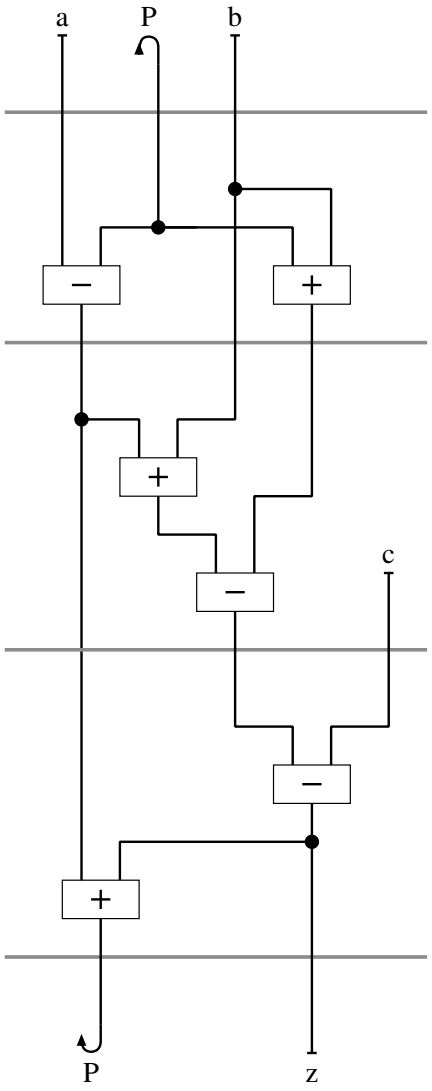


Control Table:

Q2b (3 Marks) State Encoding

What is the best choice for the state encoding for your system, and how many bits will you need for your state signal(s)?

NOTES:

1. The system is required to support an indeterminate number of bubbles.

State encoding:	
Number of bits in state signal(s):	
Name(s) of state signal(s) (needed for Q2c)	

Q2c (7 Marks) VHDL Coding

Write the VHDL code for each datapath register in your design.

NOTES:

1. Your VHDL code may use your registers (`r1`...`r`*n*), inputs (`i1`...`i`*n*), adders (`a1`...`a`*n*), subtracters (`s1`...`s`*n*), and state signal(s).
2. Use don't-care instantiation and peephole optimizations to simplify the control circuitry.
3. The primary marking criteria are the functional correctness and simplicity of your control circuitry, not the details of VHDL syntax.

Q3 (15 Marks) Latch Design and Analysis

(*estimated time: 20 minutes*)

You were recently hired by Juju Circuits of Arendelle. Your manager, Anna, was called away on a family emergency and has left you with the job of finishing a latch design for a customer named Hans.

Your task is:

Q3a Add gates and wires to the interiors of *box1*, *box2*, and *box3* in the diagram below to complete the design of the required latch.

Q3b Analyze the timing parameters of the latch, or explain why the circuit cannot be used to construct a latch.

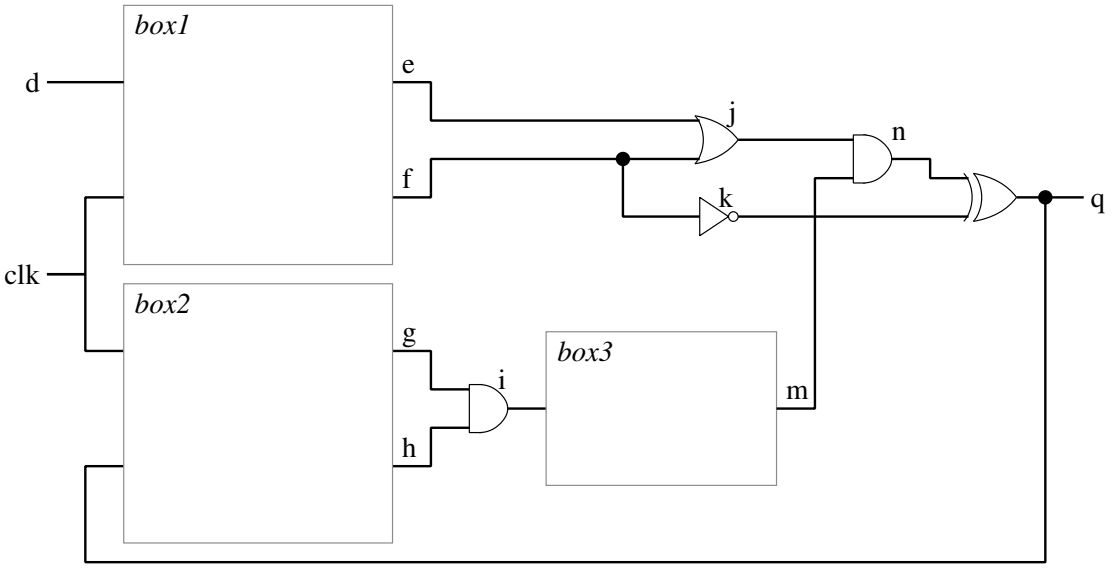
NOTES:

1. The latch shall be *active low*.
2. The existing gates and wires in the circuit shall *not* be changed.
3. The only connections between the gates that you add inside the boxes and the rest of the circuit shall be the signals:

	Inputs	Outputs
box1	`d`, `clk`	`e`, `f`
box2	`clk`, `q`	`g`, `h`
box3	`i`	`m`

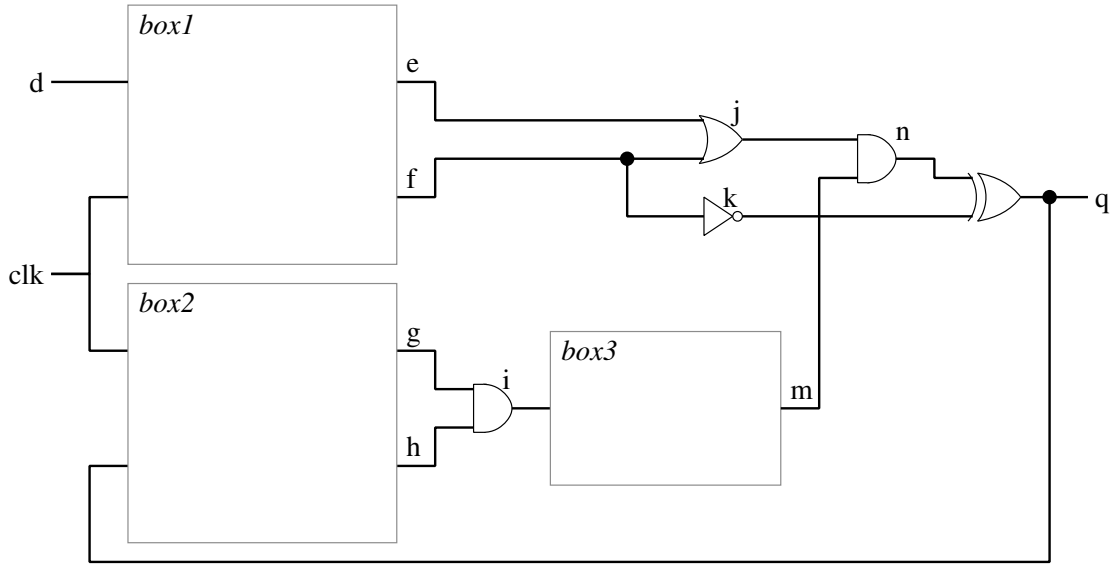
4. Optimization goals, from highest priority to lowest:
   - Minimize clock-to-Q
   - Minimize area
5. The delay through each gate is 1 ns.

Q3a Latch Design



There are additional copies of the latch for scratch work on the next page

Extra copy for scratch work



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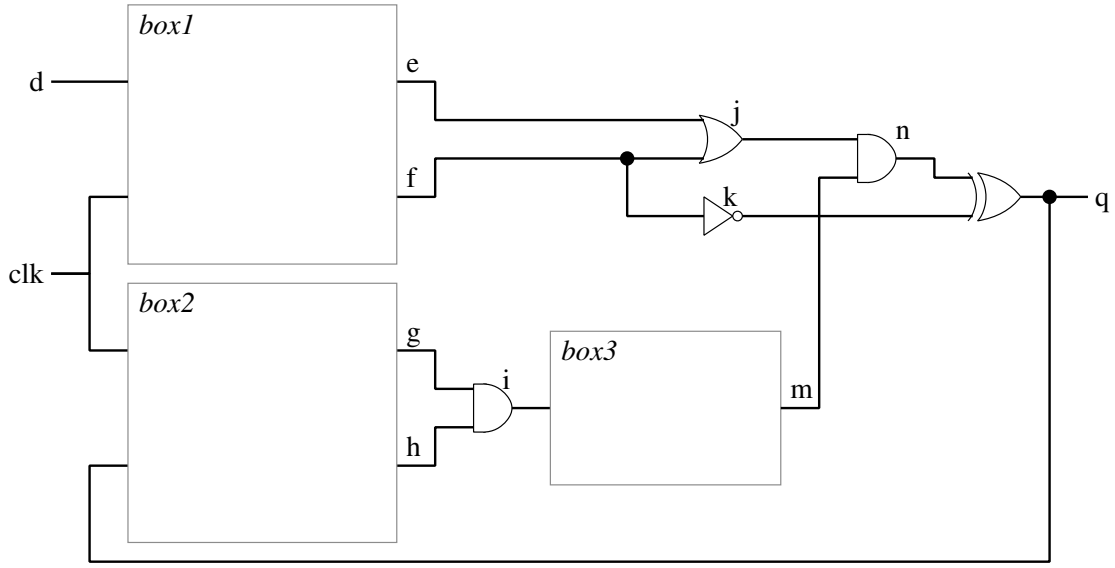


Q3b Latch Analysis or Explanation

If you were able to design a correctly functioning active-low latch, then calculate the timing parameters, otherwise, explain why the circuit cannot be used to construct an active-low latch.

Explanation: _____

Clock to Q | **Setup** | **Hold**

Q4 (15 Marks) Elmore

(*estimated time: 20 minutes*)

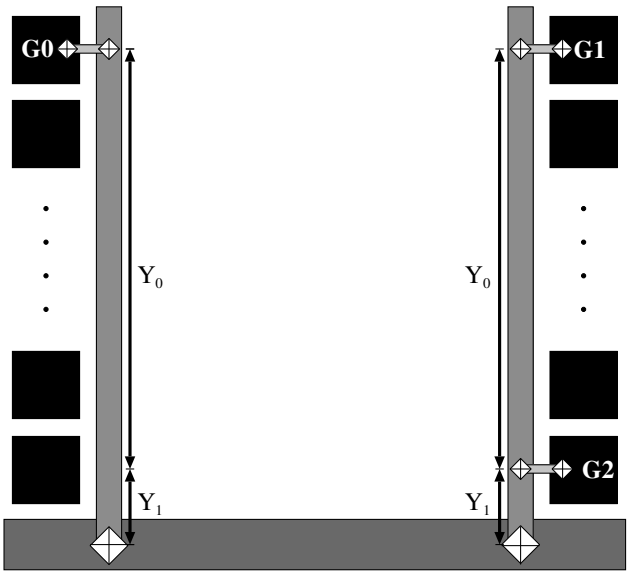
You were recently hired by Fred and George Weasley to develop a circuit for a new autopilot system for a high-speed personal aircraft. A high clock speed is very important to provide sufficient stability and performance.

Your task is to analyze the delay *from G0 to G1* for the two layouts below. If one layout has a smaller delay, then choose that layout, otherwise find an equation for the ratio $Y0/Y1$ in terms of C_L, C_Y, and C_Z such that the two layouts have the same delay.

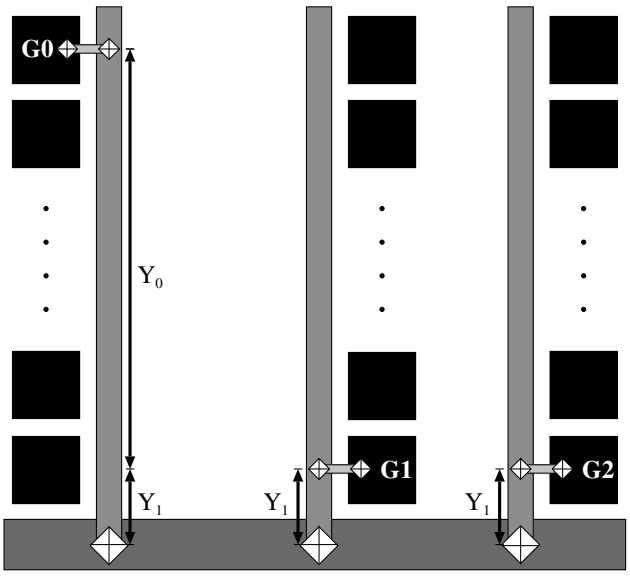
NOTES:

1. G0 is the source gate. G1 and G2 are the load gates.
2. A "switchbox" is equivalent to an "antifuse" or "via".
3. The capacitance of a node on a wire is independent of the location of the node on the wire.
4. The resistance of level-1 wires is negligible, because they are extremely short.
5. The resistance between nodes on a level-2 wire is proportional to the distance between the nodes.
6. The resistance of level-3 wires is negligible, because the cross-section of the wire is so large.
7. **For full marks, you must justify your answer.**

Symbol	Description	Capacitance	Resistance
	Gate	C_L	0
	Switchbox	0	0
	Level 1 wire	0	0
	Level 2 wire	C_Y	proportional to distance
	Level 3 wire	C_Z	0



Layout-1



Layout-2

Space for your justification and answer are on the next page

Layout with least delay from G0 to G1
OR equation for Y0/Y1 for equal delay

Q5 (15 Marks) Power and Performance

(*estimated time: 20 minutes*)

You are the project leader for a Waterluvian filter. You currently use the Cyclops-1 FPGA chip and are planning to upgrade to the Cyclops-2. The changes from the Cyclops-1 to the Cyclops-2 for various characteristics are given in the table below:

Characteristic	Cyclops-2
Delay for flip-flops and LUTS	$\frac{1}{2}$ of Cyclops-1
Area of flip-flops and LUTS	$\frac{1}{2}$ of Cyclops-1
Supply voltage	no change
Threshold voltage	no change
Number of LUTs	no change
Number of flip-flops	no change
Number of I/O pins	no change

You are considering two options for how to take advantage of the Cyclops-2:

Option 1: Speed demon Double the clock speed and make no changes to the design.

Option 2: Braniac Keep the clock speed the same, but change the design at the register-transfer level to double the length of the critical path. For example, if the critical path on the Cyclops-1 is Flop+Add, the critical path for the Cyclops-2 will be Flop+2Add. Assume that this change will not affect the number of FPGA cells in the design.

Use the table on the next page to describe the effects that each option will have on a variety of criteria.

NOTES:

1. Waterluvian filters are used in image processing. Their input and output are images with 1920x1200 pixels. The exact algorithm performed on the image is irrelevant and unknown even to those who invented the filter.
2. Your analysis should be *quantitative*, *justified*, and *brief*. For example, writing "profits will double because Speed demon is a cool name" will earn more marks than writing "profits will increase".
3. The environment is able to send the input image and receive the output image at whatever throughput and clock speed you choose.

	Speed demon	Braniac
Power consumption of the Waterluvian filter		
Energy per pixel		
Time from first input available until first output produced		
Performance in megapixels per second		

Q6 (15 Marks) Clock Gating

(*estimated time: 20 minutes*)

You are the project leader for a Waterluvian filter that is 45% over its power budget. Your clock-gating design group did a preliminary design, and then everyone went away on holidays. It is now your task to finish their work.

NOTES:

1. 25% of the clock cycles have an incoming parcel.
2. The latency of the main circuit is 20 clock cycles.
3. The maximum throughput of the main circuit is 0.5.

   If you do not know how to answer the question for a throughput of 0.5, you may earn part marks by writing a $\surd$ in the box immediately below and ignoring throughput.

   I am ignoring *throughput* ☐
4. The average behaviour of the system is to receive a sequence of 15 parcels at the maximum throughput, then receive a contiguous sequence of some number of bubbles.

   If you chose to ignore throughput above, then you shall assume that the 15 parcels arrive contiguously.
5. For the main circuit by itself, without clock gating:
   - 5% of the power consumption is short-circuiting power
   - 9% of the power consumption is leakage power
6. The area of the clock-enable state machine will be 12% of the area of the main circuit.

What is the minimum clock-gating effectiveness that is needed to reduce the total power consumption to be within budget?

The next page is also for scratch work and your answer

Minimum effectiveness