
ECE 327 Solution to Final

2016t2 (Spring)

		Total	Approx.	
		Marks	Time	Page
Q1	VHDL Semantics	10	10	2
Q2	DFD	20	30	4
Q3	Performance	10	10	6
Q4	Paths and Time	15	20	8
Q5	Elmore	15	20	11
Q6	Power and Performance	20	30	14
Q7	Clock Gating	10	10	18
<hr/> Totals		100	130	

Q1 (10 Marks) VHDL Semantics

(estimated time: 10 minutes)

In delta-cycle simulation, in which mode do processes start, and why do the VHDL simulation semantics require that processes start in this mode?

Answer:

All processes start out resumed.

All processes that start as resumed in a simulation cycle are given a chance to run in that simulation cycle. Without this rule, processes would remain suspended until an external stimulus was provided to cause them to have a need to run.

Marking:**Mode**

2 marks *“Postponed”*

1 mark *“Active” or “Suspended”*

Reason

3 marks *“... all processes run ...”*

1.5 marks *information is correct, but does not justify answer*

Fill in the blanks in the sentence below:

A delta cycle is a simulation cycle in which time does not advance

Marking:

1 mark *Each correct answer*

0.5 marks *“infinitesimally small moment in time” as alternative to “simulation cycle”*

When doing delta-cycle simulation, how do you know that you are at the end of a simulation round?

Answer:

There are no visible assignments in the simulation cycle, or alternatively, all signals kept their previous visible value.

Marking:

3 marks *correct answer*

1.5 marks *correct information, but does not justify the answer*

Q2 (20 Marks) DFD

(estimated time: 30 minutes)

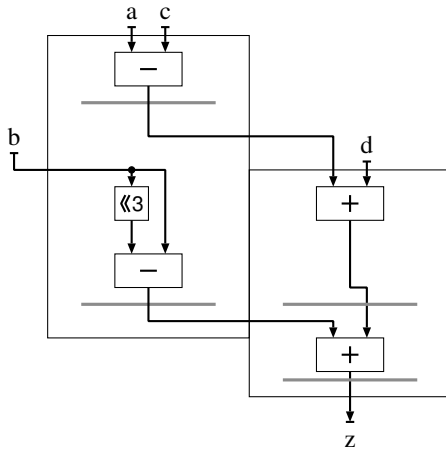
Your task is to design a dataflow diagram for the equation: $z = a + 7b - c + d$.

NOTES:

1. The design will be implemented on a FPGA
2. Outputs shall be registered
3. Optimization goals, in order of decreasing importance:
 - (a) Minimize *internal* area (this area is everything *except* input and output ports)
 - (b) Minimize clock period
 - (c) Minimize latency
 - (d) Maximize throughput
4. All signals are declared as: `signed(15 downto 0)`.
5. You may ignore the possibility of overflow.
6. A 16-bit multiplier consumes 64 LUTs.
7. Adders and subtractors consume the normal number of LUTs as taught in class.
8. You may ignore the area consumed by multiplexers.
9. You may schedule the input values to arrive in any order, but you may read each input value only once.
10. You do *not* need to do any allocation.
11. Algebraic optimizations are allowed, so long as the externally visible behaviour remains unchanged.

Answer:

Optimal design 20 marks max



Throughput: 1/2
 Latency: 3
 Clock period: $\max(\text{add}, \text{sub}) + \text{flop}$
 Area: 32 LUTs, 32 flop : 32 cells total

Marking:

+15 marks Dataflow diagram drawing

+10 marks Minimize area

+2 marks use $(8 - 1) \times b$, not $7b$

+1 marks use left-shift, not mult

+2 marks 1 add

+2 marks 1 sub

+1 marks comb inputs

+2 marks minimum number of regs (2 regs)

+2 marks Minimize latency

- Overlapping pipe stages if pipelined
- Put multiple operations in single clock cycle

+3 marks Maximize throughput

3 marks Pipelining with max possible tput

1 mark Pipelining with lower tput

+5 marks Analysis

+1 mark Each for throughput, latency, clock period

+2 marks Area

Q3 (10 Marks) Performance*(estimated time: 10 minutes)*

The average rate of performance increase in your market segment is 90% per year. Your product is currently 20% below average in performance. What annual rate of performance increase must you achieve in order to catch up to the average performance in 3.5 years?

Answer:

1. Initial equations:

$$P_{\text{avg}}(t) = P_{\text{avg}0} \times 1.9^t$$

$$P_0 = 0.8P_{\text{avg}0}$$

$$P_1 = P_{\text{avg}}(3.5)$$

$$P_1 = P_0 \times n^{3.5}$$

2. Solve for n : annual rate of performance increase for our system.

$$P_1 = P_0 \times n^{3.5}$$

$$n^{3.5} = \frac{P_1}{P_0}$$

$$= \frac{P_{\text{avg}}(3.5)}{0.8P_{\text{avg}0}}$$

$$= \frac{P_{\text{avg}0} \times 1.9^{3.5}}{0.8P_{\text{avg}0}}$$

$$= \frac{1.9^{3.5}}{0.8}$$

$$n^{3.5} = 11.82$$

$$n = 11.82^{1/3.5}$$

$$= 2.03$$

3. Final answer:

Our performance must increase at an annual rate of 103%.

Marking:

- +3 marks** *equation for exponential increase in performance over time*
- +1 mark** *equation for current performance of our product*
- +1 mark** *equation for future performance of avg product*
- +1 mark** *equation for future performance of our product*
- +2 marks** *correct algebra*
- +2 marks** *correct description of answer*

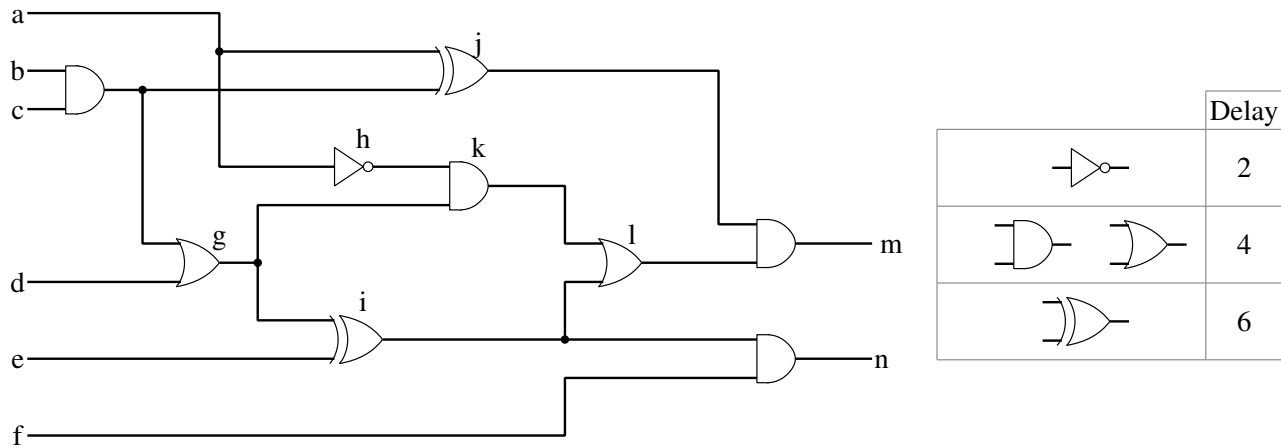
Q4 (15 Marks) Paths and Time

(estimated time: 20 minutes)

In this question, you will analyze paths and excitations for the circuit below.

NOTES:

1. An extra copy of the circuit is provided for scratchwork with each part of the question.
2. Except for gate “i” in Q4c, all gates have the delays specified in the table below.

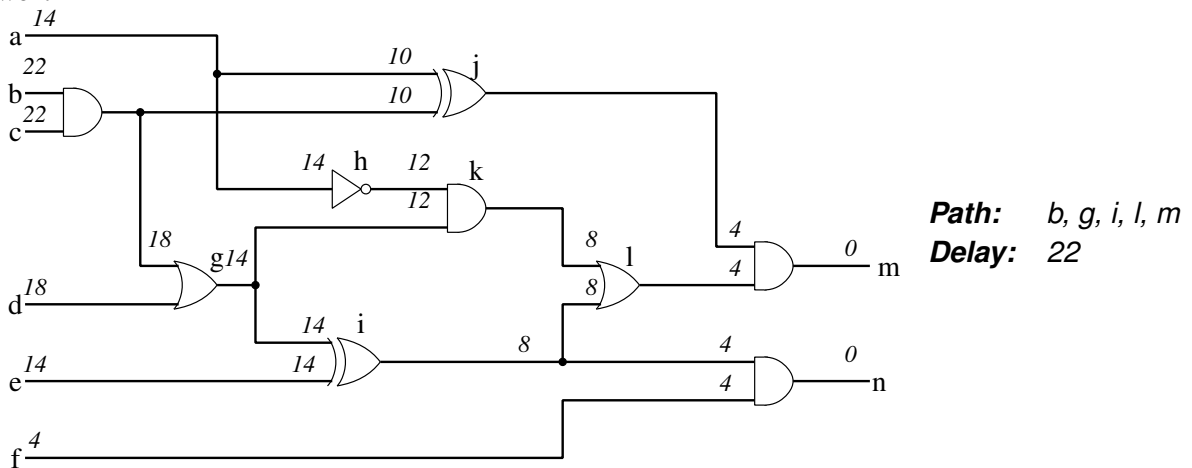


Q4a What is the longest path through the circuit and what is the delay along this path?

NOTES:

1. If there is more than one longest path, choose the path that is alphabetically earlier (e.g., if the longest paths are $\langle q, r, s, \dots \rangle$ and $\langle q, r, u, \dots \rangle$, choose $\langle q, r, s, \dots \rangle$).

Answer:



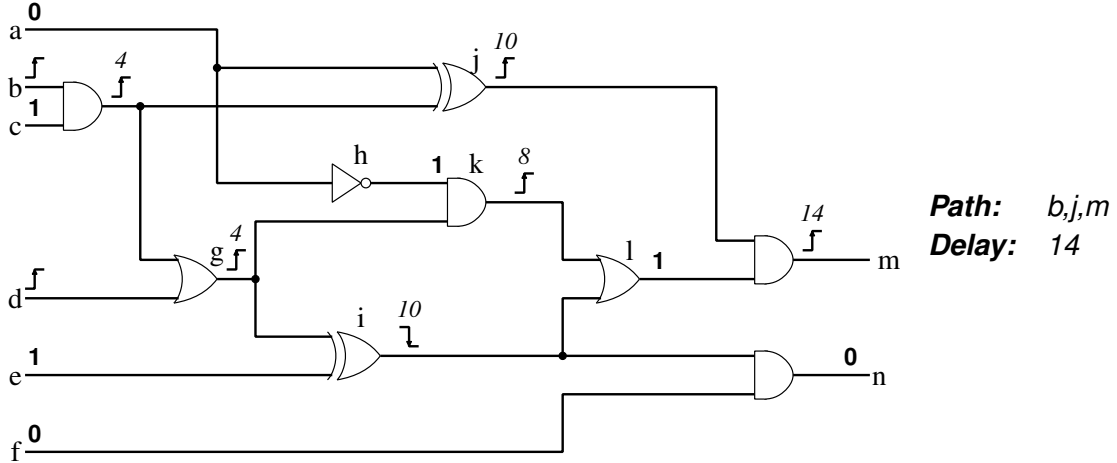
Marking:

- +3 marks path
- +1 mark delay

Q4b What path is exercised by the excitation below, and what is the delay along this path?

Excitation: $a='0'$, $b='f'$, $c='1'$, $d='f'$, $e='1'$, $f='0'$.

Answer:



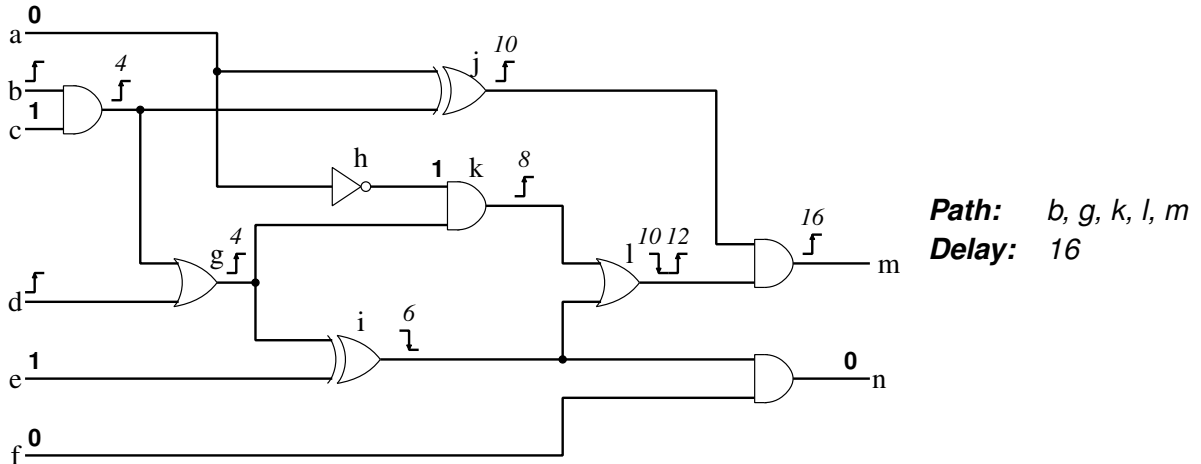
Marking:

+3 marks *path*

+1 mark *delay*

Q4c Because of manufacturing variability, on a physical chip, different instances of the same gate (e.g., the “i” and “j” instances of xor) might have different delays. If the delay of “i” is 2 and the delay of all of the other gates do not change, what path is exercised by the excitation from Q4b, and what is the delay along this path?

Answer:



Marking:

+3 marks *path*

+1 mark *delay*

Q4d Does this question illustrate the importance of the monotone speedup correctness criterion? **For full marks, you must justify your answer.**

Answer:

Yes, this question illustrates the importance of the monotone speedup correctness criterion, because when we reduced the delay through i , the delay through the circuit increased from 14 to 16.

If our critical path analysis algorithm did not satisfy monotone speedup correctness, then we might incorrectly conclude that the excitation could experience a maximum delay of 14, when in fact by reducing the delay through i , the circuit has a delay of 16 for this excitation.

Marking:

+1 mark *monotone speedup related to reduced delay*

+1 mark *monotone speedup related to edges propagating*

+1 mark *monotone speedup related to output edges arriving later than with slow gate*

Q5 (15 Marks) Elmore

(estimated time: 20 minutes)

In this question, you will use the Elmore delay model to analyze the circuits below (A, B, C, and D) with respect to the maximum clock speed of each circuit.

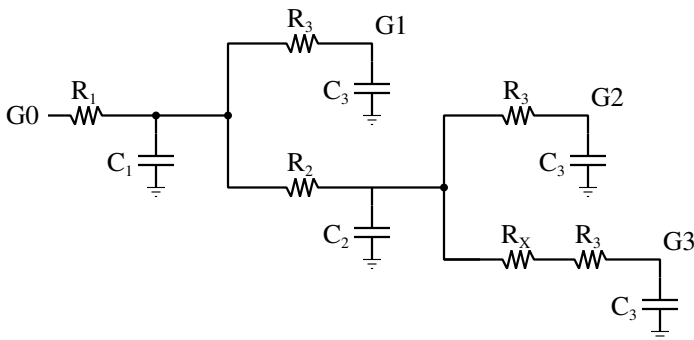
NOTES:

1. Each of the gates (G0, G1, G2, and G3) is a flip-flop.
2. Each resistor R_i and capacitor C_i has the same value in each circuit.

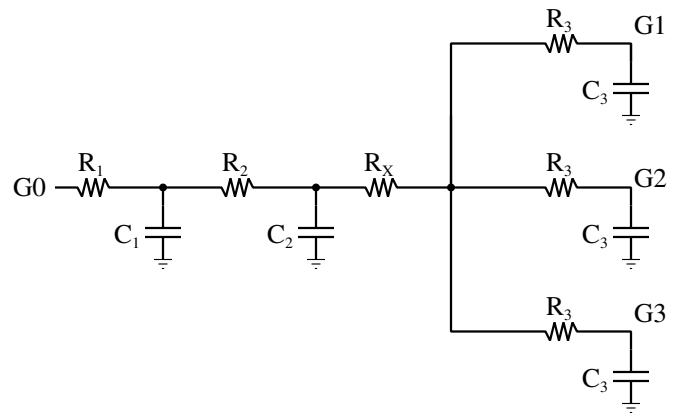
For example, the R_1 resistors have the same value in each circuit, and the R_2 resistors have the same value in each circuit; but the value of R_1 might be different from the value of R_2 .

3. If multiple circuits have the same maximum clock speed, write the identifiers for the circuits (A, B, C, or D) on the same line in the ranking.

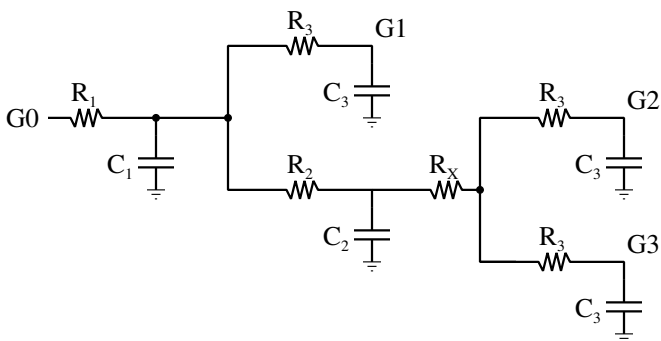
A



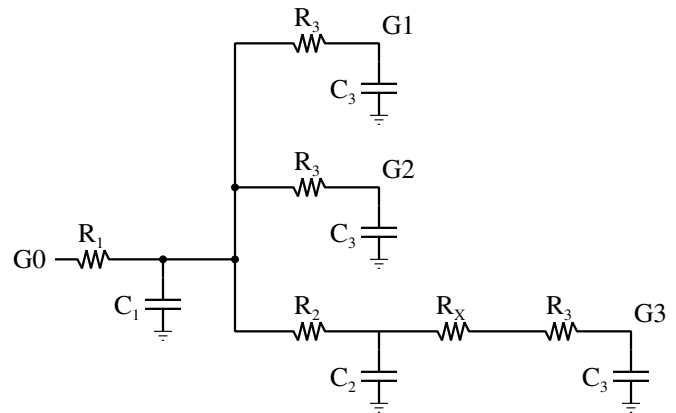
B



C



D



Use the next page to answer the question

Rank the circuits (A, B, C, and D) from fastest to slowest in terms of the maximum clock speed of the circuit. **For full marks, you must justify your answer.**

Answer:

Strategy:

1. The minimum clock period for each circuit will be determined by the delay to the slowest gate in the circuit.
2. Find the slowest gate in each circuit.
3. Compare the equations for the delays of the circuits.

1. Slowest gate in each circuit

Each of the gates has an R_3 resistor and a C_3 capacitor.

A Because of R_2 , the gates G_2 and G_3 are slower than G_1 .

Because of R_X , the gate G_3 is slower than G_2 .

Therefore, G_3 is the slowest gate.

B All three gates have equal delay.

C Because of R_X , the gates G_2 and G_3 are slower than G_1 .

G_2 and G_3 have equal delay.

D Because of R_2 and R_X , the gate G_3 is slower than G_1 and G_2 .

2. Ranking of circuits

- R_1 has the same set of downstream capacitors in each circuit.
- Each of the R_3 s has the same downstream capacitance in each circuit.
- Therefore, the differences will come from R_2 and R_X .

	R_2	R_X
A	$C_2 + 2C_3$	C_3
B	$C_2 + 3C_3$	$3C_3$
C	$C_2 + 2C_3$	$2C_3$
D	$C_2 + 1C_3$	$1C_3$

Circuit

Fastest 1 **D**

2 **A**

3 **C**

Slowest 4 **B**

Marking:

- +2 marks** *maximum clock speed determined by slowest gate*
- +6 marks** *Elmore equations*
- +4 marks** *identify slowest gate on each circuit*
- +3 marks** *analysis of Elmore equations and final conclusions*

Q6 (20 Marks) Power and Performance*(estimated time: 30 minutes)*

Your company, Waterluvian Inc, has entered the market of ectoplasm visualizers with the first-generation Ectoplasm Visual System (EVS-1). The EVS-1 was so successful that Metaphysical Money, a venture capital firm in New York, has acquired Waterluvian Inc. Your new project is to develop a next-generation Ectoplasm Visual System (EVS-2) that consumes less power than your EVS-1.

EVS-2 will use the same FPGA chip as EVS-1, but will use a lower supply voltage. In addition, two of the engineers on your team, Alberto and Dina, have proposed optimizations.

	EVS-1	Alberto's area optimization	Dina's delay optimization
Setup	0.5ns	• reduce area by 25%	• increase area by 15%
Hold	0.3ns	• increase propagation delay by 15%	• reduce propagation delay by 25%
Clock-to-Q	0.8ns		
Propagation delay	5.0ns		
Supply voltage	1.2 V		
Threshold voltage	0.7 V		

NOTES:

- The optimality of ectoplasm visualizers is measured by: $\frac{\text{ClockSpeed}}{\text{Area}}$
- Alberto and Dina's optimizations are measured using a supply voltage of 1.2 V.
- EVS-2 will use:
 - supply voltage of 1.1 V
 - either Alberto's area optimization or Dina's delay optimization

Your tasks are:

- Choose the optimization for EVS-2 that will reduce power consumption the most.
- Calculate the minimum power consumption that EVS-2 will use as a percentage change from the power of EVS-1. (For example, "EVS-2 will use n% more/less power than EVS-1".)
- Calculate the maximum optimality that you predict EVS-2 will achieve as a percentage change from the optimality of EVS-1. (For example, "EVS-2's optimality will be n% greater/less than EVS-1's optimality".)

Answer:

Choose Alberto, because area is proportional to power, so reducing area will reduce power consumption.

Assumptions:

- 1. Clock jitter and clock skew are negligible*
- 2. Leakage power and short-circuiting power are negligible*
- 3. The optimizations will not change the activity factor*

Strategy:

1. Use info on Alberto's optimization to find minimum clock period with Alberto's optimization and original VDD.
2. Decreasing VDD will increase delay. Find minimum clock period with Alberto's optimization and new VDD.
3. Calculate new optimality.
4. Calculate new power:

$$\text{Power} \propto \frac{\text{Area} \times VDD^2}{\text{ClkPeriod}}$$

1. EVS-1 clock period: T_{tot1}

$$\begin{aligned} T_{\text{tot1}} &= T_{\text{co1}} + T_{\text{pd1}} + T_{\text{su1}} \\ &= 0.8 + 5.0 + 0.5 \\ &= 6.30\text{ns} \end{aligned}$$

2. EVS-1 optimality: O_1

$$\begin{aligned} O_1 &= \frac{1}{T_{\text{tot1}} \times A_1} \\ &= \frac{1}{6.30 \times A_1} \end{aligned}$$

3. EVS-2 clock period with original supply voltage: T_{tot2}

$$\begin{aligned} T_{\text{pd2}} &= 1.15T_{\text{pd1}} \\ &= 1.15 \times 5.0 \\ &= 5.75\text{ns} \end{aligned}$$

$$\begin{aligned} T_{\text{tot2}} &= T_{\text{co1}} + T_{\text{pd2}} + T_{\text{su1}} \\ &= 0.8 + 5.75 + 0.5 \\ &= 7.05\text{ns} \end{aligned}$$

4. EVS-2 clock period with reduced supply voltage: T'_{tot2}

$$\begin{aligned}
 T'_{\text{tot2}} &= \frac{VDD_2}{(VDD_2 - V_{\text{th}}^2)} \frac{(VDD_1 - V_{\text{th}}^2)}{VDD_1} T_{\text{tot2}} \\
 &= \frac{1.1}{(1.1 - 0.7)^2} \frac{(1.2 - 0.7)^2}{1.2} 7.05 \text{ ns} \\
 &= 6.875 \times 0.2083 \times 7.05 \text{ ns} \\
 &= 10.10 \text{ ns}
 \end{aligned}$$

5. O'_2

$$\begin{aligned}
 O'_2 &= \frac{1}{T'_{\text{tot2}} \times A_2} \\
 &= \frac{1}{10.10 \times 0.75 A_1} \\
 &= \frac{1}{7.57 A_1}
 \end{aligned}$$

6. Change in optimality

$$\begin{aligned}
 \Delta O &= \frac{O_1 - O'_2}{O_1} \\
 &= \frac{1/6.30 - 1/7.57}{1/6.30} \\
 &= 16.78\% \text{ less}
 \end{aligned}$$

7. EVS-2 power: P'_2

$$\begin{aligned}
 \frac{P'_2}{P_1} &= \frac{A_2 \times VDD_2^2 \times T_{\text{tot1}}}{A_1 \times VDD_1^2 \times T'_{\text{tot2}}} \\
 &= \frac{0.75 A_1 \times 1.1^2 \times 6.30}{A_1 \times 1.2^2 \times 10.10} \\
 &= \frac{5.717}{14.54} \\
 &= 0.3931 \\
 &= 61\% \text{ less}
 \end{aligned}$$

Marking:

+1 marks *Choice of optimization*

+3 marks *Assumptions*

+16 marks *Main problem*

+1 marks *area with optimization*

+2 marks *clock period is $t_{co}+t_{pd}+t_{su}$*

+2 marks *clock period with optimization*

+2 marks *clock period with reduced supply voltage*

+2 marks *new optimality*

+2 marks *new power consumption*

+2 marks *percentage change calculations*

+3 marks *clarity of strategy and neatness*

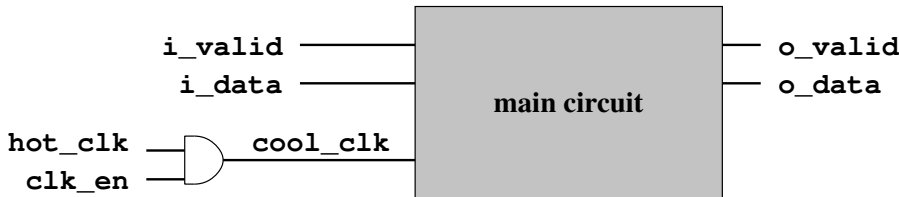
Q7 (10 Marks) Clock Gating

(estimated time: 10 minutes)

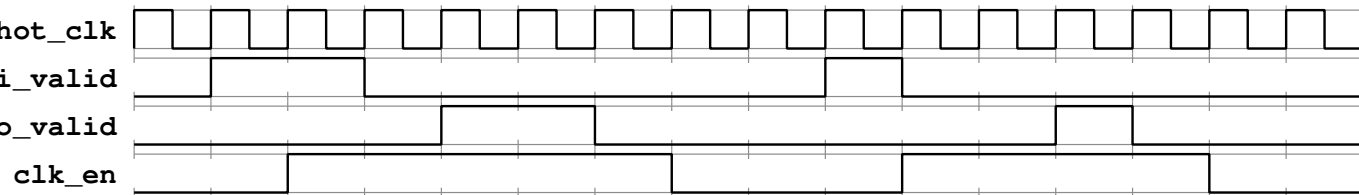
For the system described below, draw the waveform for the `clk_en` signal so that the signal `cool_clk` is turned on for the minimum number of clock cycles such that the main circuit works correctly.

NOTES:

1. The latency through the system is 3 clock cycles.



Answer:



The signal `o_valid` is shown for clarity, it is not required as part of the answer.

Marking:

10 marks

- 1 mark one or both intervals start one cycle too early/late
- 2 marks one or both intervals start two cycles too early/late
- 2 marks inconsistent start behaviour between two intervals
- 1 mark one or both intervals end one cycle too early/late
- 2 marks one or both intervals end two cycles too early/late
- 2 marks inconsistent end behaviour between two intervals

3 marks two intervals with `clken='1'`

2 marks one interval with `clken='1'`

1 mark `clken='1'` entire time