ECE 327 Final

2016t2 (Spring)

Instructions and General Information

- 100 marks total
- There are extra pages for scratch work at the end of the exam.
- If you need *additional scratch* paper, request some from a proctor. The work done on the *additional scratch* paper will not be marked. **All answers to be marked must be on the exam paper, which includes the pages at the end of the exam.**
- The proctors and instructors will **not answer questions**, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.
- **Justifications** of answers will be marked according to correctness, clarity, and concision.
- To earn part marks, you must show the formulas you use and all of your work.

Potentially Useful Information

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (10 Marks) VHDL Semantics

(*estimated time: 10 minutes*)

In delta-cycle simulation, in which mode do processes start, and why do the VHDL simulation semantics require that processes start in this mode?

Mode: _____

Reason: _____

Fill in the blanks in the sentence below:

A delta cycle is a _____

in which _____ .

When doing delta-cycle simulation, how do you know that you are at the end of a simulation round?

Q2 (20 Marks) DFD

(*estimated time: 30 minutes*)

Your task is to design a dataflow diagram for the equation: `z = a + 7b - c + d`.

NOTES:

1. The design will be implemented on a FPGA
2. Outputs shall be registered
3. Optimization goals, in order of decreasing importance:
   (a) Minimize *internal* area (this area is everything *except* input and output ports)
   (b) Minimize clock period
   (c) Minimize latency
   (d) Maximize throughput
4. All signals are declared as: `signed( 15 downto 0 )`.
5. You may ignore the possibility of overflow.
6. A 16-bit multiplier consumes 64 LUTs.
7. Adders and subtracters consume the normal number of LUTs as taught in class.
8. You may ignore the area consumed by multiplexers.
9. You may schedule the input values to arrive in any order, but you may read each input value only once.
10. You do *not* need to do any allocation.
11. Algebraic optimizations are allowed, so long as the externally visible behaviour remains unchanged.

Next page is for DFD and analysis

Analysis:

Throughput:		Clock period:	
Latency:		Area	

Q3 (10 Marks) Performance

(*estimated time: 10 minutes*)

The average rate of performance increase in your market segment is 90% per year. Your product is currently 20% below average in performance. What annual rate of performance increase must you achieve in order to catch up to the average performance in 3.5 years?

Annual rate of performance increase:

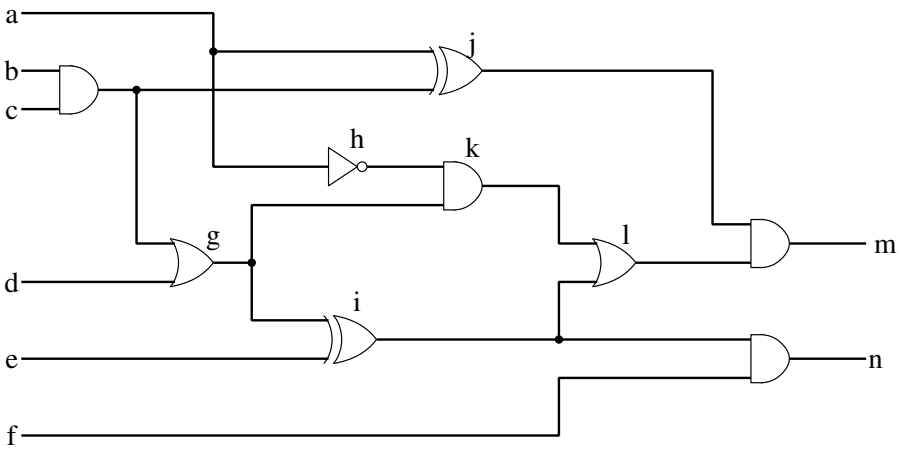
Q4 (15 Marks) Paths and Time

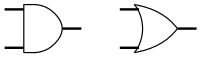
(*estimated time: 20 minutes*)

In this question, you will analyze paths and excitations for the circuit below.

NOTES:

1. An extra copy of the circuit is provided for scratchwork with each part of the question.
2. Except for gate "i" in Q4c, all gates have the delays specified in the table below.

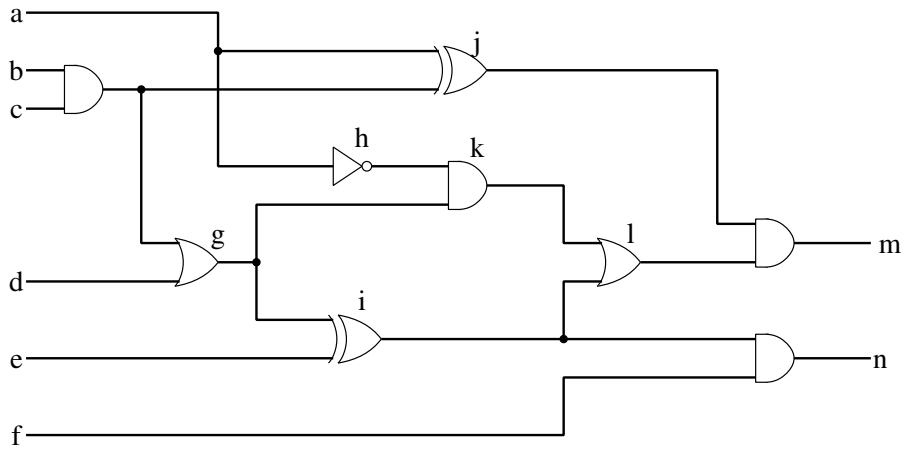


	Delay
	2
	4
	6

Q4a What is the longest path through the circuit and what is the delay along this path?

NOTES:

1. If there is more than one longest path, choose the path that is alphabetically earlier (e.g., if the longest paths are $\langle \mathtt{q}, \mathtt{r}, \mathtt{s}, ... \rangle$ and $\langle \mathtt{q}, \mathtt{r}, \mathtt{u}, ... \rangle$, choose $\langle \mathtt{q}, \mathtt{r}, \mathtt{s}, ... \rangle$).

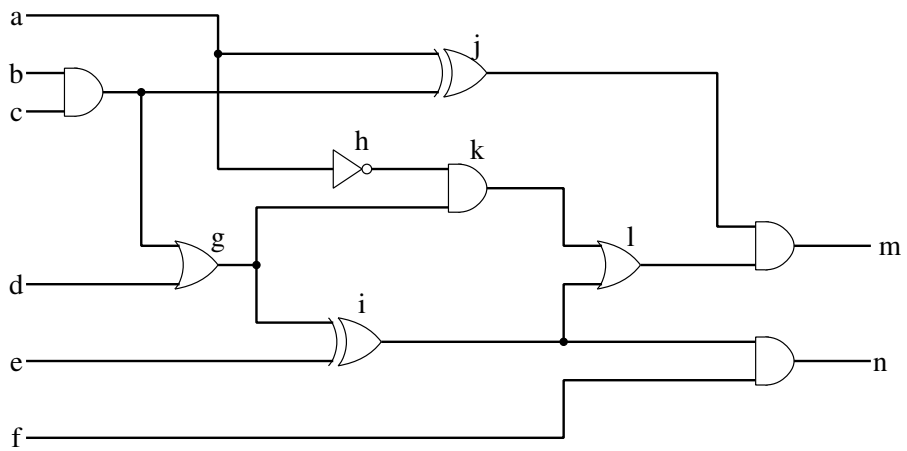


Path: _____ **Delay:** _____

This question continues on the next page

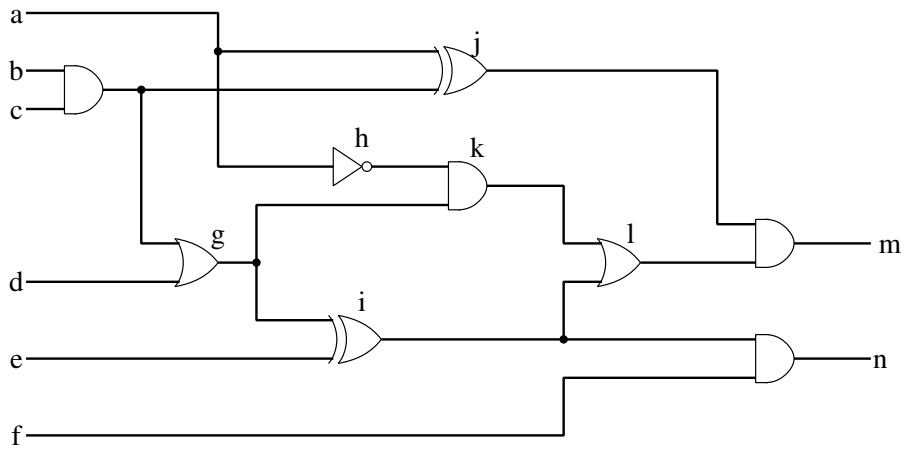
Q4b What path is exercised by the excitation below, and what is the delay along this path?

Excitation: a='0', b=⎍, c='1', d=⎍, e='1', f='0'.



Path: _____ **Delay:** _____

Q4c Because of manufacturing variability, on a physical chip, different instances of the same gate (*e.g.*, the "i" and "j" instances of `xor`) might have different delays. If the delay of "i" is 2 and the delay of all of the other gates do not change, what path is exercised by the excitation from Q4b , and what is the delay along this path?



Path: _____ **Delay:** _____

Q4d Does this question illustrate the importance of the monotone speedup correctness criterion? **For full marks, you must justify your answer.**

Q5 (15 Marks) Elmore

(*estimated time: 20 minutes*)

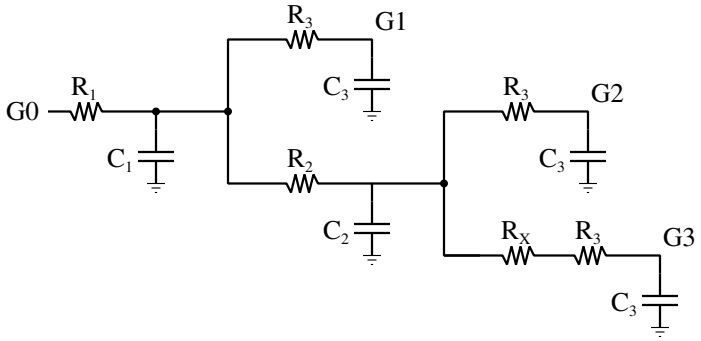
In this question, you will use the Elmore delay model to analyze the circuits below (A, B, C, and D) with respect to the maximum clock speed of each circuit.

NOTES:

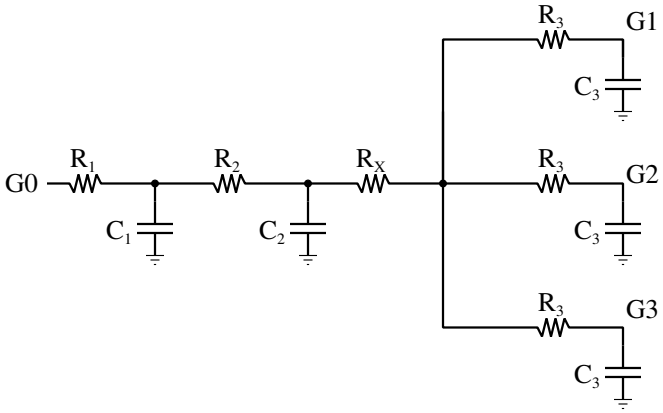
1. Each of the gates (G0, G1, G2, and G3) is a flip-flop.
2. Each resister R_i and capacitor C_i has the same value in each circuit.

   For example, the R_1 resistors have the same value in each circuit, and the R_2 resistors have the same value in each circuit; but the value of R_1 might be different from the value of R_2.
3. If multiple circuits have the same maximum clock speed, write the identifiers for the circuits (A, B, C, or D) on the same line in the ranking.

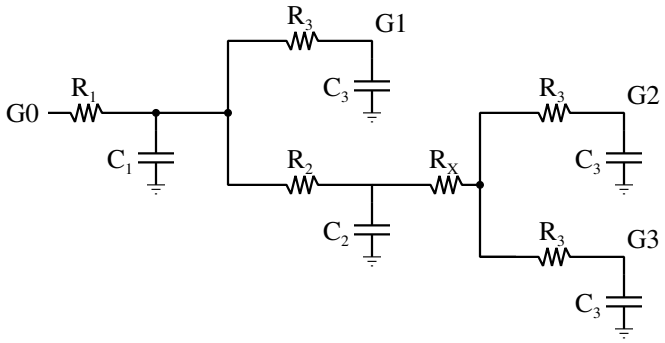
A



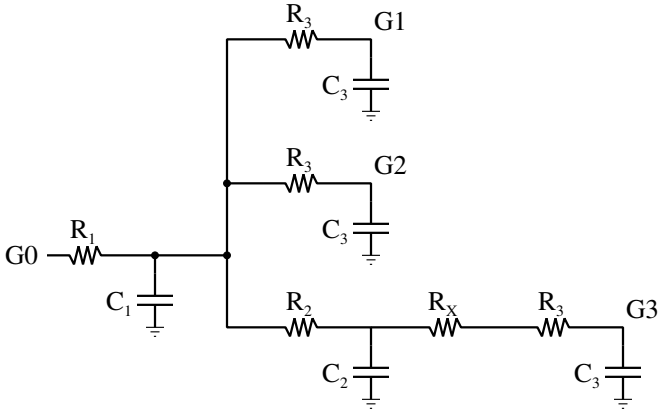
B



C



D



Use the next page to answer the question

Rank the circuits (A, B, C, and D) from fastest to slowest in terms of the maximum clock speed of the circuit. **For full marks, you must justify your answer.**

	Circuit
Fastest 1	
2	
3	
Slowest 4	

Q6 (20 Marks) Power and Performance

(*estimated time: 30 minutes*)

Your company, Waterluvian Inc, has entered the market of ectoplasm visualizers with the first-generation Ectoplasm Visual System (EVS-1). The EVS-1 was so successful that Metaphysical Money, a venture capital firm in New York, has acquired Waterluvian Inc. Your new project is to develop a next-generation Ectoplasm Visual System (EVS-2) that consumes less power than your EVS-1.

EVS-2 will use the same FPGA chip as EVS-1, but will use a lower supply voltage. In addition, two of the engineers on your team, Alberto and Dina, have proposed optimizations.

EVS-1	
Setup	0.5ns
Hold	0.3ns
Clock-to-Q	0.8ns
Propagation delay	5.0ns
Supply voltage	1.2 V
Threshold voltage	0.7 V

Alberto's area optimization

- reduce area by 25%
- increase propagation delay by 15%

Dina's delay optimization

- increase area by 15%
- reduce propagation delay by 25%

NOTES:

1. The optimality of ectoplasm visualizers is measured by: $\frac{\text{ClockSpeed}}{\text{Area}}$
2. Alberto and Dina's optimizations are measured using a supply voltage of 1.2 V.
3. EVS-2 will use:
   - supply voltage of 1.1 V
   - either Alberto's area optimization or Dina's delay optimization

Your tasks are:

1. Choose the optimization for EVS-2 that will reduce power consumption the most.
2. Calculate the minimum power consumption that EVS-2 will use as a percentage change from the power of EVS-1. (For example, "EVS-2 will use n% more/less power than EVS-1".)
3. Calculate the maximum optimality that you predict EVS-2 will achieve as a percentage change from the optimality of EVS-1. (For example, "EVS-2's optimality will be n% greater/less than EVS-1's optimality".)

Optimization choice:

Alberto ☐

Dina ☐

Assumptions:

Workspace is on next page

Change in power: [ ] %

Change in optimality: [ ] %

Q7 (10 Marks) Clock Gating

(*estimated time: 10 minutes*)

For the system described below, draw the waveform for the `clk_en` signal so that the signal `cool_clk` is turned on for the minimum number of clock cycles such that the main circuit works correctly.

NOTES:

1. The latency through the system is 3 clock cycles.