First Name

Last Name

First letter of last name

UW Userid

ECE 327 Final

2017t1 (Winter)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- No books, no notes, no computers. Calculators are allowed
- If you need extra paper, request some from a proctor.
- Write neatly.
- To earn part marks, you must show the formulas you use and all of your work.
- **The proctors and instructors will not answer questions, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.**
- **Justifications of answers will be marked according to correctness, clarity, and concision.**

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A}\times\mathsf{C}\times\mathsf{V}^2\times\mathsf{F}) + (\tau\times\mathsf{A}\times\mathsf{V}\times\mathsf{ISh}\times\mathsf{F}) + (\mathsf{V}\times\mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins}\times\mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V}-\mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V}\times\mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q\times\mathsf{Vt}}{k\times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n}\mathsf{PI}_i\times\mathsf{C}_i)}$$

$$\mathsf{A}' = (1-\mathsf{E}(1-\mathsf{Pb}))\mathsf{A}$$

$$q = 1.60218\times10^{-19}\mathrm{C}$$

$$k = 1.38066\times10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

$$(x^y)^z = x^{(yz)}$$

$$(x^y)(x^z) = x^{(y+z)}$$

$$a = b^c \quad \text{is equivalent to:}$$
$$a^{1/c} = b$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (5 Marks) VHDL Semantics

(*estimated time: 10 minutes*)

Is it possible for a simulation round to contain exactly one simulation cycle? **For full marks, you must justify your answer in terms of the VHDL semantics.**

Q2 (15 Marks) Area Analysis

(*estimated time: 25 minutes*)

Calculate the minimum number of FPGA cells required to implement the VHDL code below.

NOTES:

1. The code implements the equation: `z = min(a+b, b+c)`.
2. The signals `a`, `b`, `c`, `ab`, `bc`, `diff` and `z` are all declared to be `signed( 15 downto 0 )`.
3. The inputs are `a`, `b`, and `c`.
4. The output is `z`.
5. Optimizations are allowed, as long as the externally visible input-to-output behaviour of the system does not change.
6. For full marks, you must justify your answer with a drawing and/or text.

```
process begin
  wait until rising_edge(clk);
  ab        <= a + b;
  bc        <= b + c;
end process;

diff      <= ab - bc;
ab_lt_bc  <= diff(15);
z         <= ab when ab_lt_bc = '1' else bc;
```

Number of FPGA cells:

Q3 (20 Marks) Performance

(*estimated time: 25 minutes*)

You work for Blueberry Solutions, a leading innovator in hardware system design. Your cousin just completed an IPO of her software company and used some of the money to purchase Blueberry Solutions. She's promoted you from the drudgery of optimizing Waterluvian filters to the glamourous world of edge detectors.

Two of your group members have proposed performance optimizations for your next edge detector circuit. You have the resources to implement only one of the optimizations.

NOTES:

1. Performance is measured in MPPS: Mega-Pixels Per Second.
2. Eric Edge has proposed an optimization that will increase MPPS by 90% for pixels that are on an edge, but will delay the project release date by 25 weeks.
3. Mark Dark has proposed an optimization that will increase MPPS by 30% for pixels that are *not* on an edge, but will delay the project release date by 5 weeks.
4. Your current design has the same performance for all pixels, regardless of whether they are on an edge.
5. The average MPPS of edge detectors increases by 2% each week.

What percentage of pixels must be on an edge for Eric's optimization to provide the same performance *relative to the average edge-detector when the product will be released* as Mark's optimization will provide *relative to the average edge-detector when the product will be released*. **For full marks, you must justify your answer.**

Workspace continues on next page

Percentage of pixels on an edge [ ]

Q4 (10 Marks) Latch Design

(*estimated time: 15 minutes*)

The circuit below is a correct active-high latch.

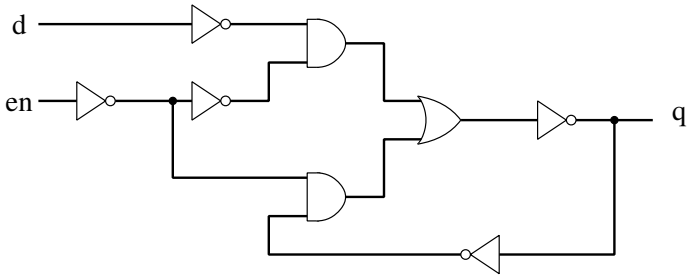
Is it possible to modify the circuit to decrease $T_{su} - T_{ho}$, that is, reduce the difference between the setup time and the hold time?

If **yes**, then draw the modified latch and calculate the new setup and hold times.

If **no**, the justify why you cannot reduce $T_{su} - T_{ho}$.

NOTES:

1. Each gate has a delay of 1 time unit.
2. If you modify the latch:
   - Your modified latch must be a correctly working active-high latch.
   - Make the minimum modifications necessary.



	Yes	**No**
$T_{su} - T_{ho}$ can be reduced	☐	☐

If you modified the latch:

Setup ☐

Hold ☐

Q5 (15 Marks) Monotone Speedup

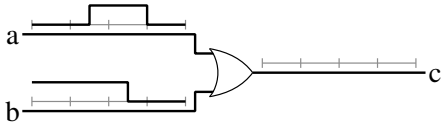
(*estimated time: 15 minutes*)

Use *one* of the excitations and circuits below to demonstrate a problem that can occur if your critical path algorithm does not satisfy the monotone speedup correctness criterion.

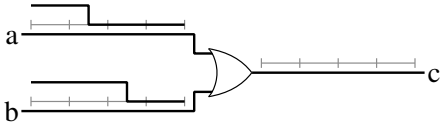
Instructions:

1. Write down any assumptions you use.
2. Choose one of the excitations and circuits (A, B, C, or D).
3. For the excitation you chose, draw the waveform for `c`.
4. Draw a modified excitation that illustrates the problem.
5. For your modified excitation, use the same gate as the excitation you chose (*e.g.*, OR for A or B, AND for C or D).
6. Briefly explain the problem.

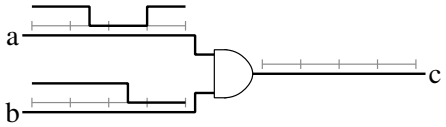
A



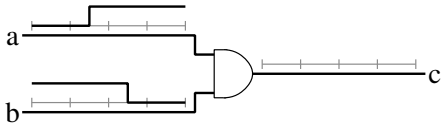
B



C



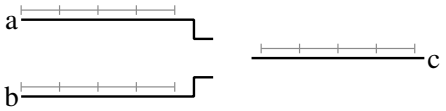
D



List any assumptions you use:

Excitation to use: ☐

Modified excitation:



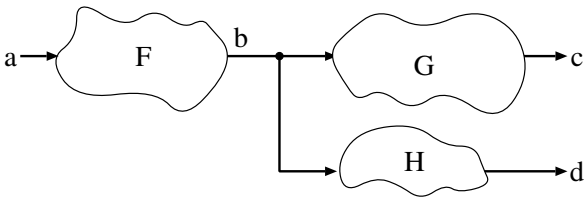
Explanation:

Q6 (20 Marks) Power and Delay

(*estimated time: 25 minutes*)

You've just returned from an extended, and well-deserved, holiday of kite-surfing and trekking in New Zealand. When you return, you discover two surprises. Spring has arrived early in Waterloo, and your employer, Blueberry Solutions, is making a bold move out of the world of FPGAs and into ASICs.

With ASICs, you have options to choose different supply voltages for different parts of your chip. Your task is to choose the supply voltages for modules F, G, and H below so as to minimize power consumption without increasing delay above the delay where all three modules use the medium supply voltage (V_m).



Voltages

V_h	1.20 V	High VDD
V_m	1.15 V	Medium VDD
V_l	1.00 V	Low VDD
V_{th}	0.70 V	Threshold voltage

	Delay with V_m	**Area**
F	150 ps	500 GE
G	250 ps	600 GE
H	100 ps	300 GE

NOTES:

1. Delay is measured in pico-seconds (ps), which is 10^{-12} seconds.
2. Area is measured in gate equivalents (GE), where 1 GE is the area of a 2-input NAND gate. The NAND gate is used because it is the smallest 2-input gate in a cell library.
3. The modules F, G, and H are purely combinational.

List any assumptions you use:

Workspace is on the next page

Supply Voltage

F

G

H

Q7 (15 Marks) Clock Gating

(*estimated time: 15 minutes*)

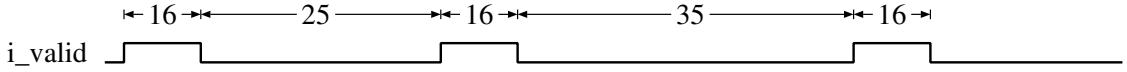
Your task is to minimize the energy per parcel for the system described below.

NOTES:

1. The system uses a "cycle count" clock gating scheme.
2. The latency is 20 clock cycles.
3. Parcels always arrive in a sequence of 1 parcel per clock cycle for 16 consecutive clock cycles, followed by some number of bubbles.
4. You have two choices for the "bubble schedule" (the number of bubbles that come after the 16 parcels):

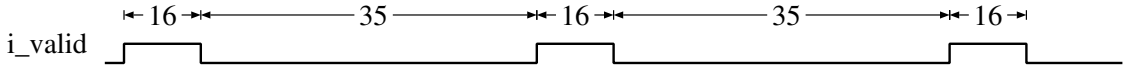
A The number of bubbles ranges from 25 to 35 with a uniform distribution.

Example waveform:



B The number of bubbles is always 35.

Example waveform:



List any assumptions you use:

Workspace is on the next page

Which bubble schedule will result in the minimum energy per parcel?

Bubble schedule with minimim energy per parcel: [ ]