ECE 327 Final

2019t1 (Winter)

Instructions and General Information

- 100 marks total
- There are extra pages for scratch work at the end of the exam.
- If you need *additional scratch* paper, request some from a proctor. The work done on the *additional scratch* paper will not be marked. **All answers to be marked must be on the exam paper.**
- The proctors and instructors will **not answer questions**, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.
- **Justifications** of answers will be marked according to correctness, clarity, and concision.
- To earn part marks, you must show the formulas you use and all of your work.

		Total Marks	**Approx. Time**	**Page**
Q0	!!Almost Free!!	1	0	2
Q1	Hardware Design	20	25	3
Q2	DFD	20	25	5
Q3	Performance	16	25	7
Q4	Elmore Delay	16	25	9
Q5	Work	14	20	11
Q6	Clock Gating	14	20	13
Totals		100	140	

ECE-327 Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A} \times \mathsf{C} \times \mathsf{V}^2 \times \mathsf{F}) + (\tau \times \mathsf{A} \times \mathsf{V} \times \mathsf{ISh} \times \mathsf{F}) + (\mathsf{V} \times \mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins} \times \mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V} - \mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V} \times \mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q \times \mathsf{Vt}}{k \times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n} \mathsf{PI}_i \times \mathsf{C}_i)}$$

$$\mathsf{A}' = (1 - \mathsf{E}(1 - \mathsf{Pb}))\mathsf{A}$$

$$q = 1.60218 \times 10^{-19}\mathrm{C}$$

$$k = 1.38066 \times 10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

$$(x^y)^z = x^{(yz)}$$

$$(x^y)(x^z) = x^{(y+z)}$$

$$a = b^c \quad \text{is equivalent to:}$$
$$a^{1/c} = b$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

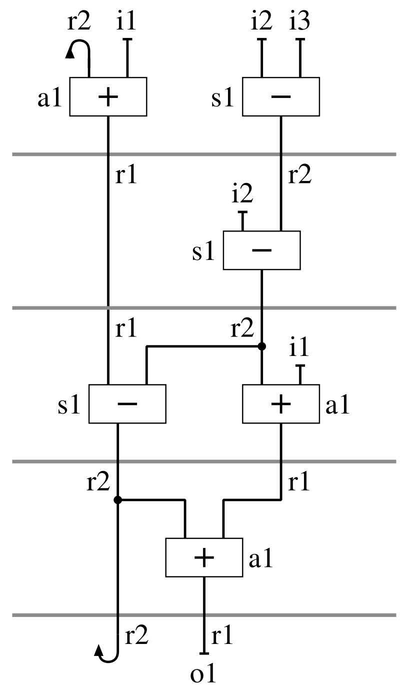
Q1 (20 Marks) Hardware Design

(*estimated time: 25 minutes*)

Design the hardware (draw a diagram of the hardware) to implement the dataflow diagram below.

NOTES:

1. Your system shall support an ASAP parcel schedule
2. Your drawing shall include both datapath and control circuitry, including the gates for the state machine.
3. Your drawing shall use the standard building blocks of RTL hardware: adders, subtracters, multiplexers, flip-flops, AND gates, OR gates, *etc.*
4. Marks will be earned for functional correctnes, simplicity and elegance of the design, and neatness of the drawing.



Q2 (20 Marks) DFD

(*estimated time: 25 minutes*)

You have graduated and are starting your dream job of designing hardware. Your first task is to design and analyze a dataflow diagram for the equation:

$$z = F^3(a) + 2F^2(a) \bullet F(a) \bullet F(a)$$

NOTES:

1. All of the signals are 16 bit `unsigned`.
2. F is a top-secret function (rumoured to be a key component in Waterluvian filters). The only information you have been given about F is:
   - F is purely combinational.
   - The input and output are both 16 bit `unsigned`.
   - $F^2(a) = F(F(a))$ (A chain of 2 Fs).
   - $F^3(a) = F(F(F(a)))$ (A chain of 3 Fs).
3. The area estimates of the components are:

Adder	A
F	A
Multiplier	3A

4. The maximum area of the datapath is 9A.
5. Optimization goals, in order of decreasing importance
   - Minimize clock period
   - Maximize throughput
   - Minimize area of datapath components (sum of the area of adders, Fs, and multipliers)
   - Minimize number of registers
   - Minimize latency
6. Algebraic optimizations *are* allowed, as long as the final output (z) is correct.
7. You may ignore the area consumed by multiplexers.
8. You do *not* need to do any allocation.

Q2a (17 Marks) Design

Draw your dataflow diagram.

Q2b (3 Marks) Analysis

Clock period		**Adders**		**Registers**	
Throughput		F**s**		**Latency**	
		Multipliers			
		Total datapath area			

Q3 (16 Marks) Performance

(*estimated time: 25 minutes*)

You have heard rumours that Waterluvian filters can be helpful in medical imaging to diagnose mysterious abdominal pains. You have decided to jump on this latest fad and create a startup company "Waterluvian advanced systems for tomagraphy engineering" (Waste).

Your task is to choose which FPGA chip to use for your Waterluvian filter. Using an FPGA chip with hardware multipliers increases performance, but also increases cost.

NOTES:

1. Performance of Waterluvian filters is measured in megapixels per second (MPPS).
2. Performance increases by 4 MPPS for each multiplier on the FPGA.
3. The average price for a Waterluvian filter increases by 1% for each increase of 1 MPPS in performance.
4. The cost of an FPGA without any multipliers is $10.
5. The cost of the FPGA increases by $0.20 for each multiplier.
6. Profit is measured as the price that you charge for the Waterluvian filter minus the cost of the FPGA chip. (You shall ignore non-recurring engineering (NRE) costs.)
7. **For full marks, you must justify your answer.**

Which option will give you a higher profit for your Waterluvian filter: using an FPGA without any multipliers or using an FPGA with 20 multipliers?

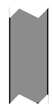
Q4 (16 Marks) Elmore Delay

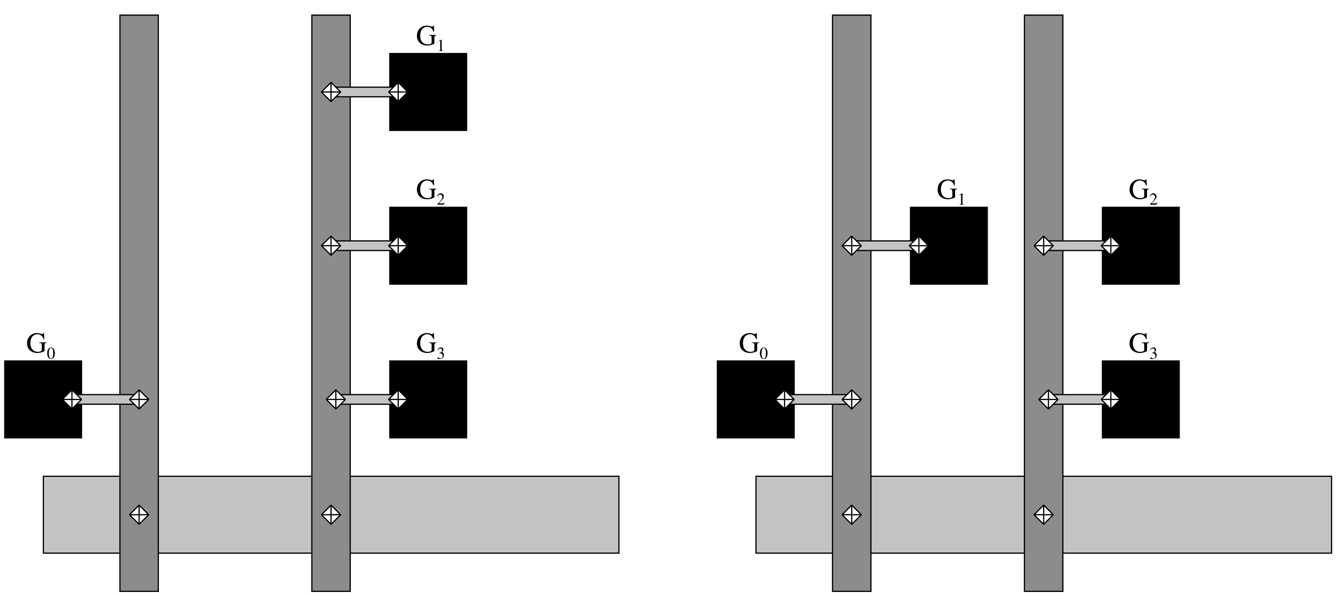
(*estimated time: 25 minutes*)

To maximize the clock speed of your Waterluvian filter, you are doing place-and-route of the FPGA cells by hand. Which layout below will have the higher clock speed?

NOTES:

1. The source gate is G_0, the other gates ($G_1 - G_3$) are destinations.
2. If you do not have sufficient information to answer the question, find an equation for the relationship between C_X, C_Y, and C_L such that the two layouts have the same delay (An example equation is: $C_X = C_Y + C_L$).
3. The capacitance of a wire is independent of distance and location on the wire.
4. **For full marks, you must justify your answer.**

Symbol	Description	Capacitance	Resistance
	Interconnect level 3	C_X	0
	Interconnect level 2	C_Y	0
	Interconnect level 1	0	0
	Gate	C_L	0
	Switchbox	0	R



Layout 1 **Layout 2**

Layout with higher clock speed:

Q5 (14 Marks) Work

(*estimated time: 20 minutes*)

What is the minimum set of parameters needed to calculate the impact on the amount of work your battery powered Waterluvian filter can accomplish on 1 battery charge if you decrease VDD by 20%?

NOTES:

1. The impact on work is measured as a percentage, *e.g.*, "with a 20% decrease in VDD, the filter can process at most 10% fewer pixels".
2. All of the parameters below refer to the original system, before VDD is reduced.
3. If there are multiple sets that have the same number of parameters, choose the set with the minimum sum of the indices (*e.g.*, 1: Clock frequency + 2: Cycles per instruction = 3 is better than 1: Clock frequency + 3: Power = 4).
4. **For full marks, you must justify your answer.**

Index	Parameter	Needed? Yes	Needed? No
1	Clock frequency	☐	☐
2	Cycles per instruction	☐	☐
3	Power	☐	☐
4	Energy in battery	☐	☐
5	VDD	☐	☐
6	Threshold voltage	☐	☐
7	Number of instructions to process one pixel	☐	☐
8	Millions of instructions per second	☐	☐

Q6 (14 Marks) Clock Gating

(*estimated time: 20 minutes*)

Your manager has told you that she wants to use clock gating to reduce power consumption. In your Waterluvian filter, there are 6 candidate modules to which you could apply clock gating. But, your manager has said that there is time to design and implement clock gating for only one module. Which one of the modules below should you choose?

NOTES:

1. The time to design and implement clock gating is the same for each module.
2. Each row has at most 2 unique values (*e.g.*, 1.2 and 1.4 for VDD). To make it easier to see the differences between the modules, gray boxes are used to distinguish the two values.
3. **For full marks, you must justify your answer.**

	Module					
	1	**2**	**3**	**4**	**5**	**6**
VDD (V)	1.2	1.2	1.4	1.4	1.4	1.4
Clock frequency (MHz)	500	500	500	600	600	600
Area (FPGA cells)	200	200	200	300	300	200
Latency (cycles)	6	6	6	6	6	6
Activity factor	0.25	0.25	0.25	0.30	0.25	0.25
Average number of contiguous parcels	10	10	10	10	10	10
Average number of contiguous bubbles	70	14	70	14	14	14

List any assumptions that you use:

Module that is best choice for clock gating: [ ]

This page is for scratch work for any question

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