ECE 327 Final

2020t1 (Winter)

Instructions and General Information

- 100 marks total
- There are extra pages for scratch work at the end of the exam.
- If you need *additional scratch* paper, request some from a proctor. The work done on the *additional scratch* paper will not be marked. **All answers to be marked must be on the exam paper.**
- The proctors and instructors will **not answer questions**, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.
- **Justifications** of answers will be marked according to correctness, clarity, and concision.
- To earn part marks, you must show the formulas you use and all of your work.

ECE-327 Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A}\times\mathsf{C}\times\mathsf{V}^2\times\mathsf{F}) + (\tau\times\mathsf{A}\times\mathsf{V}\times\mathsf{ISh}\times\mathsf{F}) + (\mathsf{V}\times\mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins}\times\mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V}-\mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V}\times\mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q\times\mathsf{Vt}}{k\times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n}\mathsf{PI}_i\times\mathsf{C}_i)}$$

$$\mathsf{A}' = (1-\mathsf{E}(1-\mathsf{Pb}))\mathsf{A}$$

$$q = 1.60218\times10^{-19}\mathrm{C}$$

$$k = 1.38066\times10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

$$(x^y)^z = x^{(yz)}$$

$$(x^y)(x^z) = x^{(y+z)}$$

$$a = b^c \quad \text{is equivalent to:}$$
$$a^{1/c} = b$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (1 Mark) Honesty Declaration

(*estimated time: 1 minutes*)

In the space below, write a sentence stating that you promise that you will not discuss the exam with anyone until the exam period is over.

Q2 (1 Mark) Ten Years from Now...

(*estimated time: 1 minutes*)

Ten years from now, what, if anything other than the lack of TimBits, will you remember about this course?

Q3 (20 Marks) VHDL Coding

(*estimated time: 60 minutes*)

Write a synthesizable VHDL program named max2 that satisfies the following specification:

1. The input signals shall be:
   - `clk, reset i_valid : std_logic`
   - `i_data : unsigned( 7 downto 0 )`
2. The outputs shall be:
   - `o_done : std_logic`
   - `o_max1, o_max2 : unsigned( 7 downto 0 )`
3. The system receives a sequence of 8 input values and outputs the two highest values from the sequence.
4. Each parcel of input data is denoted by a single clock cycle of `i_valid='1'`.
5. The environment guarantees that there are at least 2 bubbles between each `i_valid='1'`.
6. Within 3 clock cycles after the 8th input value in a sequence has been received (`i_valid='1'`), the system shall set `o_done='1'`, `o_max1` to the maximum value in the sequence, and `o_max2` to the second highest value in the sequence. That is, if the 8th `i_valid='1'` happens at time t, then `o_done='1'` must happen between t and $t+3$ inclusive.
7. When `o_done='1'`, the system shall hold `o_done`, `o_max1`, and `o_max2` constant until `reset='1'` or `i_valid='1'`.
8. The system shall allow multiple sequences to be sent consecutively without a `reset='1'` between the end of one sequence and the beginning of the next sequence.

Marking: The importance of various characteristics of the design in decreasing order of importance

- Synthesizability
- Correct functionality
- Elegance of design and cleanliness of code

Q4 (12 Marks) RTL Simulation

(*estimated time: 15 minutes*)

Rewrite (decompose and sort) the code below to prepare it for RTL simulation. If the code is not compatible with RTL simulation, then explain why.

NOTES:

1. Do not perform any logical or arithmetic optimizations.
2. Ignore the elaboration error in the multiplication operations caused by the VHDL ”feature” that the length of the output of a multiplication is sum of the lengths of the inputs.

Original program

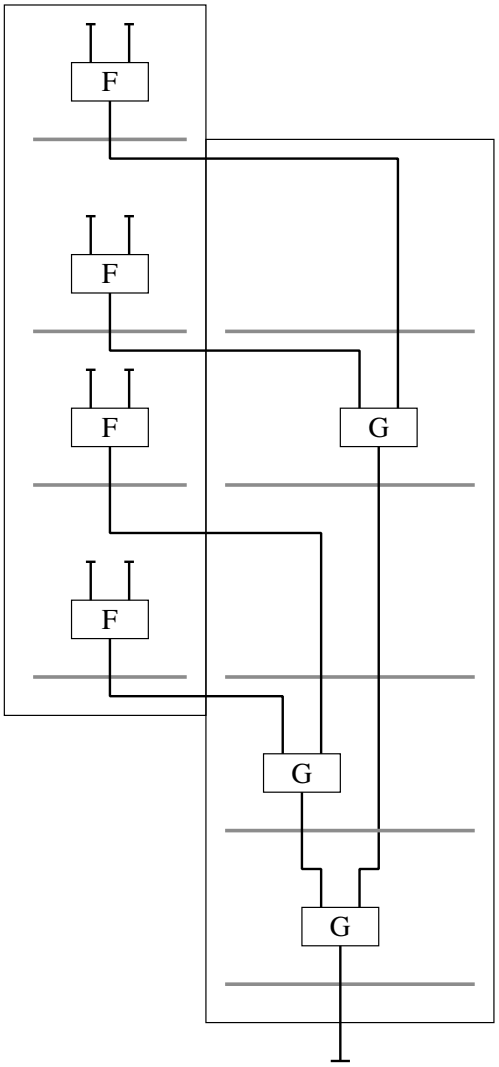
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity sim is
end entity;

architecture main of sim is

  signal clk, a, b : std_logic;
  signal e, f, g, q, r, s, t : unsigned( 7 downto 0 );

begin
```

```
  process begin
    clk <= '0';
    wait for 5 ns;
    clk <= '1';
    wait for 5 ns;
  end process;

  process begin
    a <= '0';
    b <= '1';
    wait for 7 ns;
    a <= '1';
    g <= to_unsigned( 3, 8 );
    wait for 10 ns;
    a <= '0';
    b <= '0';
    g <= to_unsigned( 5, 8 );
    wait;
  end process;

  process (a, b, e, f, g, q ) begin
    if a = '1' then
      q <= e + f;
      if b = '1' then
        r <= q + g;
        t <= e + g;
      else
        r <= q - g;
        t <= e - g;
      end if;
    else
      q <= e * f;
      r <= q * g;
      t <= e * g;
    end if;
  end process;

  process (q, r) begin
    s <= q + r;
  end process;

  process begin
    wait until rising_edge( clk );
    e <= f;
    f <= g;
  end process;

end architecture;
```

Q5 (12 Marks) DFD Analysis

(*estimated time: 10 minutes*)

Analyze the dataflow diagram by answer the questions below:



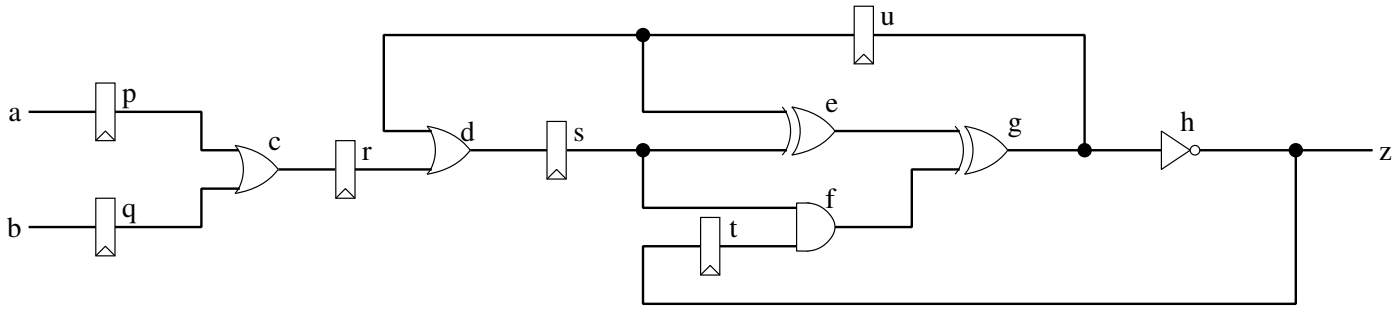
Throughput:
Latency:
Number of registers:
Minimum latency:

Q6 (10 Marks) Retiming

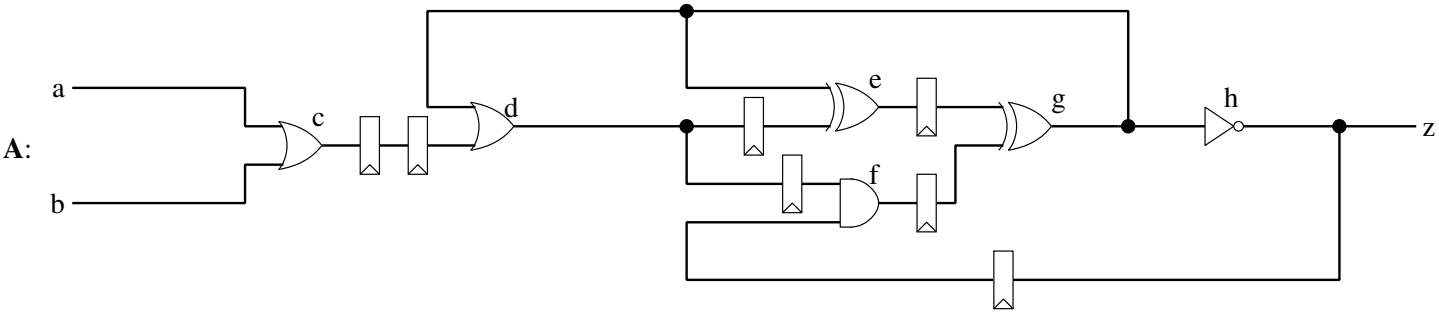
(*estimated time: 20 minutes*)

Which **one** of the circuits (A–D) is a possible retiming of the original circuit.

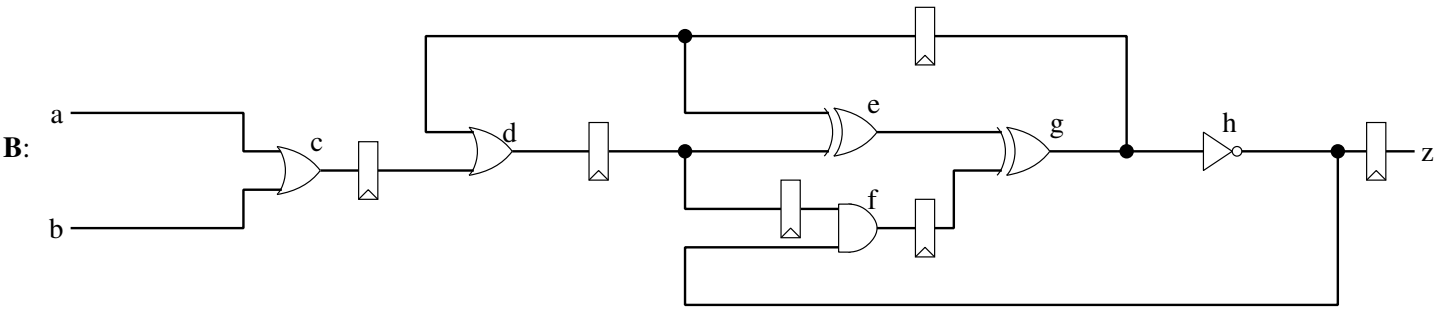
Original circuit:



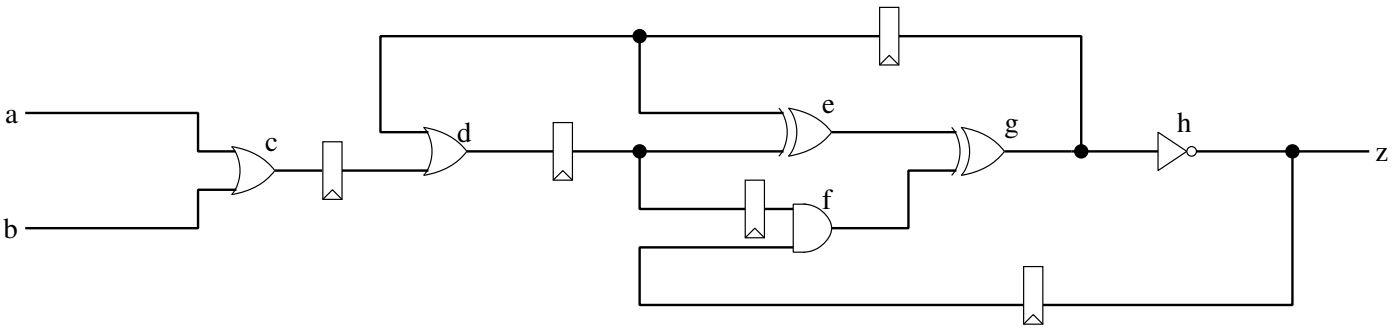
A:



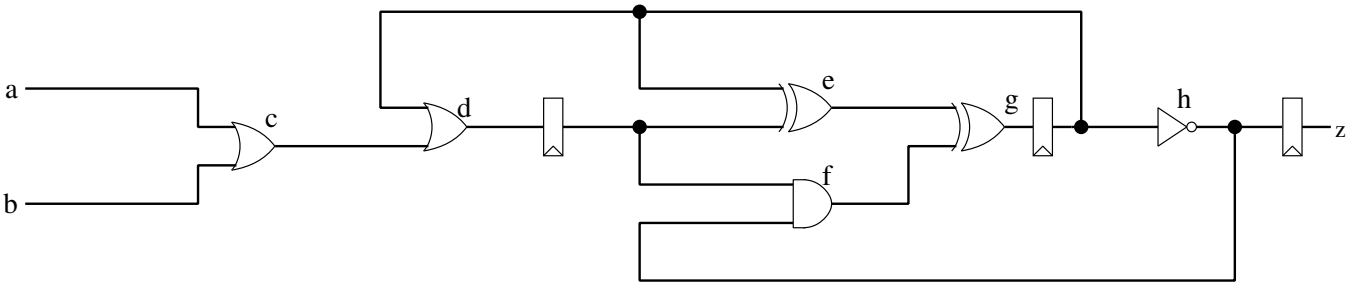
B:



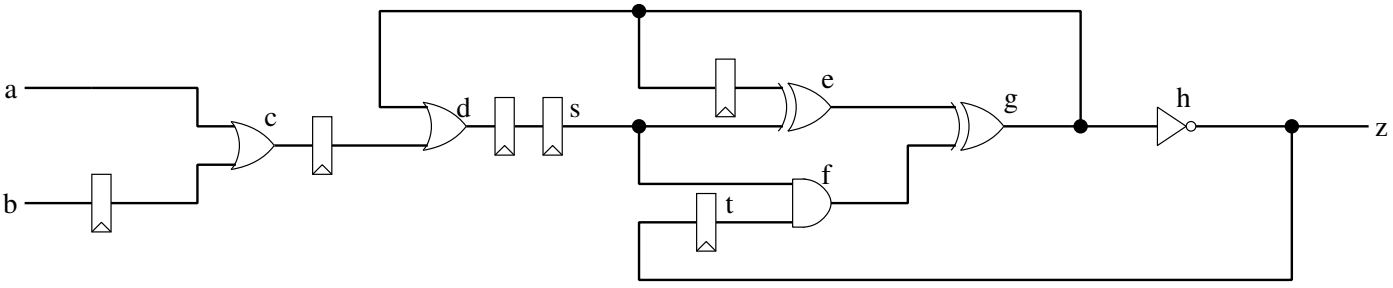
C:



D:



E:



Q7 (12 Marks) Real-Time Performance

(*estimated time: 15 minutes*)

The ECE-327 course notes state that for real time systems (systems like anti-lock brakes that must respond within a certain amount of time), latency is often more important than throughput.

Briefly explain the probable justification for this statement.

Answer:

Latency measures the time from when the inputs are available until the output is produced. Real time systems need to react within a certain amount of time, which matches the definition of latency.

In contrast, throughput measures the rate at which data enters or exits the system. So, a system with a high throughput could have a very long latency, which means that the system would be slow to respond to an input.

Marking:

- **+3 marks** *definition of latency*
- **+3 marks** *definition of throughput*
- **+3 marks** *real-time needs quick response to input*
- **+3 marks** *real time requirements matches definition of latency*

Q8 (12 Marks) Performance Analysis

(*estimated time: 15 minutes*)

After more than a decade of success developing professional-grade high-performance Waterluvian filters, your company without a clever name has developed a low-cost consumer-grade Waterluvian filter. The first version of the consumer-grade Waterluvian filter (Cv1) has 25% lower performance and 5% higher area than your professional model (Pro). You are now working on version 2 of the consumer filter (Cv2). If Cv2 has the same area as Cv1, how much will you have to increase the performance from Cv1 to Cv2 for the optimality of Pro to be 10% more than the optimality of Cv2?

NOTES:

1. Optimality is measured as performance/area.
2. To earn part marks, explain your method for solving the problem and show the key equations that you use.

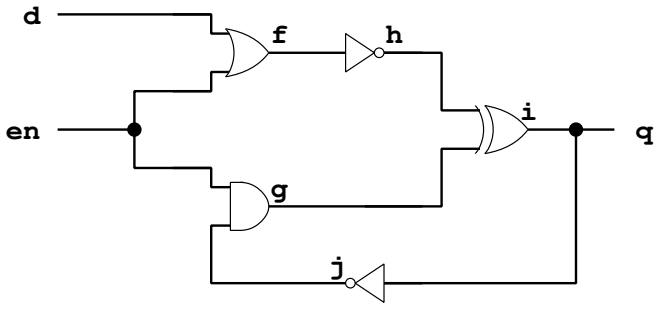
Q9 (12 Marks) Latch Analysis

(*estimated time: 15 minutes*)

Does the circuit below behave like a latch?

If yes, answer whether the latch is active high or active low; and calculate the clock-to-Q, setup, and hold times.

If no, choose locations to add inverters to make the circuit act as a latch. (For example, ”add 2 inverters between i and q”). The goal is to add the minimum possible number of inverters.



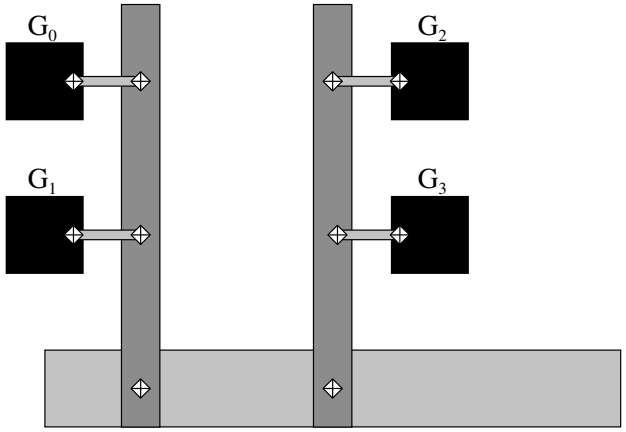
Q10 (10 Marks) Elmore Delay

(*estimated time: 20 minutes*)

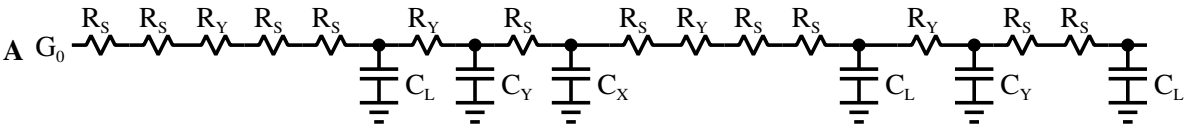
Which one of the RC-networks (A-E) is the best model for the layout below?

Symbol	Description	Capacitance	Resistance
	Interconnect level 3	C_X	0
	Interconnect level 2	C_Y	proportional to distance
	Interconnect level 1	0	0
	Gate	C_L	0
	Switchbox	0	R_S

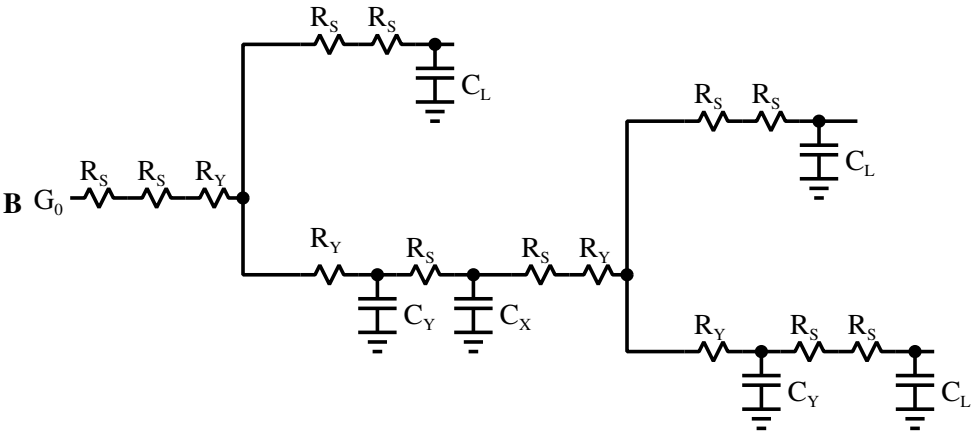
The resistances and capacitances for the physical layout are:



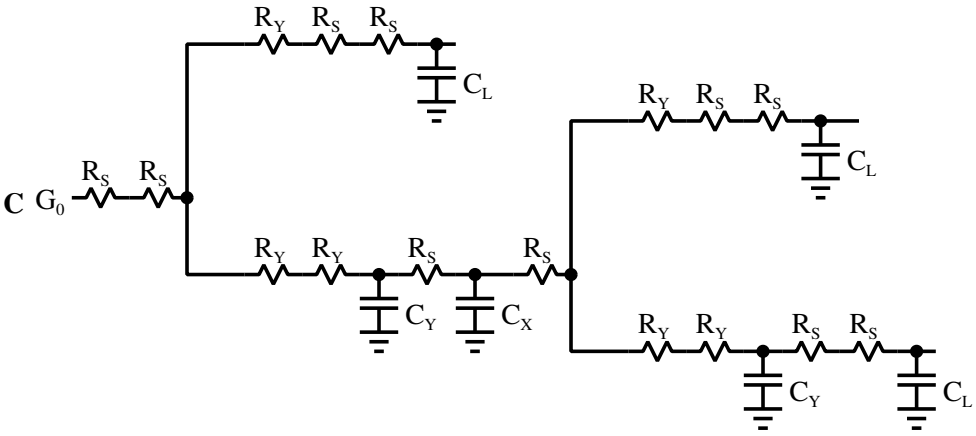
A



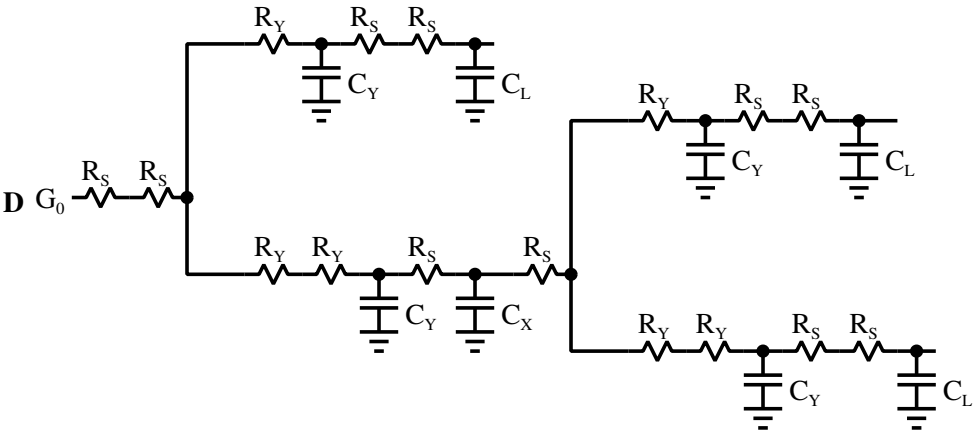
B


R_S R_S C_L
R_S R_S C_L
R_S R_S R_Y
G_0
R_Y R_S R_S R_Y
C_Y C_X
R_Y R_S R_S
C_Y C_L

C


R_Y R_S R_S C_L
R_Y R_S R_S C_L
R_S R_S
G_0
R_Y R_Y R_S R_S
C_Y C_X
R_Y R_Y R_S R_S
C_Y C_L

D


R_Y R_S R_S C_Y C_L
R_Y R_S R_S C_Y C_L
R_S R_S
G_0
R_Y R_Y R_S R_S
C_Y C_X
R_Y R_Y R_S R_S
C_Y C_L

E