1 Course Description

- An advanced course on the design of digital integrated circuits.

2 Course Objectives

- To teach the design of advanced digital circuit in modern CMOS processes.
- Focus on digital design areas where full custom circuits are required to meet stringent performance criteria. These areas include: high performance ALUs, sequencing elements (flip-flops), SRAM arrays, and high-speed interconnects.
- In addition to traditional power/performance tradeoffs, the effects of process variability will be considered as an equally important design consideration.
- A series of design projects will give students experience implementing, analyzing, and optimizing a variety of circuits using Cadence Virtuoso.

3 Date and Time

- Lecture Location: EIT 3151
- Lecture Time: Mondays 7:00pm - 10:00pm

4 Evaluation

- Your evaluation in this course is based on 3 major components:

<table>
<thead>
<tr>
<th># of Deliverables</th>
<th>Item</th>
<th>Grade</th>
<th>Weight</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Final Exam</td>
<td></td>
<td>50%</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Project/Lab/Assignments</td>
<td></td>
<td>40%</td>
<td>5 × 8% each</td>
</tr>
<tr>
<td>1</td>
<td>Paper Review/Presentation</td>
<td></td>
<td>10%</td>
<td>10% (5% review, 5% presentation)</td>
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</table>
5 Tentative Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Lecture</th>
<th>Lab</th>
<th>Lab Due Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Sept 8</td>
<td>Intro/MOSFETS</td>
<td>LS1: MOSFETs</td>
<td>Sept 22 @ 7pm</td>
</tr>
<tr>
<td>2</td>
<td>Sept 15</td>
<td>No Lecture</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Sept 22</td>
<td>Combination Logic</td>
<td>LS2: Inverter, NAND</td>
<td>Oct 6 @ 7pm</td>
</tr>
<tr>
<td>4</td>
<td>Sept 29</td>
<td>Variability</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Oct 6</td>
<td>Sequential Logic</td>
<td>LS3: DFF</td>
<td>Oct 20 @ 7pm</td>
</tr>
<tr>
<td>6</td>
<td>Oct 13</td>
<td>No Lecture - Thanksgiving</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Oct 20</td>
<td>Custom Adders</td>
<td>LS4: Adder</td>
<td>Nov 3 @ 7pm</td>
</tr>
<tr>
<td>8</td>
<td>Oct 27</td>
<td>Custom Multipliers/ALUs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Nov 3</td>
<td>SRAM Architecture</td>
<td>LS5: SRAM Bitcell</td>
<td>Nov 17 @ 7pm</td>
</tr>
<tr>
<td>10</td>
<td>Nov 10</td>
<td>SRAM Variability</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Nov 17</td>
<td>Clocking</td>
<td>LS6: Paper Review</td>
<td>Dec 1 @ 7pm</td>
</tr>
<tr>
<td>12</td>
<td>Nov 24</td>
<td>TBA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Dec 1</td>
<td>Course Review</td>
<td>Presentations</td>
<td></td>
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</tbody>
</table>

6 Resource Texts


7 Instructor

<table>
<thead>
<tr>
<th>Instructor</th>
<th>Adam Neale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Email</td>
<td><a href="mailto:ajneale@uwaterloo.ca">ajneale@uwaterloo.ca</a></td>
</tr>
<tr>
<td>Office</td>
<td>EIT 4017</td>
</tr>
<tr>
<td>Phone</td>
<td>519 888 4567 x31212</td>
</tr>
</tbody>
</table>

8 Distribution of Information

- Information will be distributed to the class via:
  - Announcements made in class.
  - Announcements made on LEARN.
  - Additional learning material will be available on LEARN, and posted as necessary.
  - It is your responsibility to check for announcements regularly.
  - If you miss a lecture, it is your responsibility to catch up on the material by either contacting the course instructor, or another student in the class.

9 Labs

- All labs must be completed individually:
You may not copy files directly from another student.

You may not submit work in groups.

Collaboration with other students on labs/assignments should be limited to: general discussion and assistance with tool debug.

- There will be 5 labs throughout the term:
  - Labs are to be done outside the classroom on your own time.
  - Labs descriptions will be released on the day of lectures during weeks: 1, 3, 5, 7, and 9.
  - Labs will be due 2 weeks following their release at 7pm on Monday evenings prior to lectures. Labs should be submitted electronically via LEARN.
  - You are allowed to submit multiple times on LEARN; however, only the most recent submission will be graded.
  - All due dates are fixed. Late lab submissions will be penalized at a rate of 20% of the maximum grade per day. Late penalties may be waived by the course instructor under exceptional circumstances.

10 Paper Review and Presentation

- To keep up to date with the latest advances in the field requires the ability to read and understand information from technical papers.

- 5% of your final grade will be dedicated to a report of a recent paper from a circuits conference or journal (likely ISSCC 2014 or a JSSC 2014, but this will be finalize later in the term).

- The final lecture will be devoted toward presentations of each of these reports (also 5% of final grade).

- Reports and presentations must be completed individually, report length and presentation durations will depend on student enrollment in the course.

11 Illness

- A student who misses the final examination must provide:
  - A Verification of Illness form, or
  - Other documentation as appropriate
  - Please, try not to miss the final exam

12 Academic Offense

- Academic offenses include but are not limited to:
  - Infringing unreasonably on the work of other students
  - Cheating
  - Plagiarism
  - Misrepresentation

- All students should be familiar with the University’s Policy 71 regarding Student Discipline
  - https://uwaterloo.ca/secretariat-general-counsel/policies-procedures-guidelines/policy-71
13 Plagiarism

• If one student copies from another student, both students are responsible regardless of the first student's knowledge of the offense.

• The penalty for plagiarism on a lab/assignment is a mark of zero on lab/assignment in question with the potential for further consequences.

• All instances of plagiarism will be reported to the Associate Dean of Graduate Studies.

• The Associate Dean may increase the penalty at their discretion. This may include:
  – Retaking the course
  – The requirement for a course on ethics
  – A suspension
  – Expulsion