Digital Integrated Circuits Syllabus
Fall 2014 ECE637

1 Course Description

- An advanced course on the design of digital integrated circuits.

2 Course Objectives

- To teach the design of advanced digital circuit in modern CMOS processes.
- Focus on digital design areas where full custom circuits are required to meet stringent performance criteria. These areas include: high performance ALUs, sequencing elements (flip-flops), SRAM arrays, and high-speed interconnects.
- In addition to traditional power/performance tradeoffs, the effects of process variability will be considered as an equally important design consideration.
- A series of design projects will give students experience implementing, analyzing, and optimizing a variety of circuits using Cadence Virtuoso.

3 Date and Time

- Lecture Location: EIT 3151
- Lecture Time: Mondays 7:00pm - 10:00pm

4 Evaluation

- Your evaluation in this course is based on 3 major components:

# of Deliverables	Item	Grade Weight	Note
1	Final Exam	50%	
5	Project/Lab/Assignments	40%	$5 \times 8\%$ each
1	Paper Review/Presentation	10%	10% (5% review, 5% presentation)

5 Tentative Schedule

Week	Date	Lecture	Lab	Lab Due Date
1	Sept 8	Intro/MOSFETS	LS1: MOSFETs	Sept 22 @ 7pm
2	Sept 15	No Lecture		
3	Sept 22	Combination Logic	LS2: Inverter, NAND	Oct 6 @ 7pm
4	Sept 29	Variability		
5	Oct 6	Sequential Logic	LS3: DFF	Oct 20 @ 7pm
6	Oct 13	No Lecture - Thanksgiving		
7	Oct 20	Custom Adders	LS4: Adder	Nov 3 @ 7pm
8	Oct 27	Custom Multipliers/ALUs		
9	Nov 3	SRAM Architecture	LS5: SRAM Bitcell	Nov 17 @ 7pm
10	Nov 10	SRAM Variability		
11	Nov 17	Clocking	LS6: Paper Review	Dec 1 @ 7pm
12	Nov 24	TBA		
13	Dec 1	Course Review	Presentations	

6 Resource Texts

- J. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuits: A Design Perspective," 2nd Edition, Prentice Hall, 2003.
- Neil Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective, 3rd or 4th Edition.

7 Instructor

Instructor	Adam Neale
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Phone	519 888 4567 x31212

8 Distribution of Information

- Information will be distributed to the class via:
  - Announcements made in class.
  - Announcements made on LEARN.
  - Additional learning material will be available on LEARN, and posted as necessary.
  - It is your responsibility to check for announcements regularly.
  - If you miss a lecture, it is your responsibility to catch up on the material by either contacting the course instructor, or another student in the class.

9 Labs

- All labs must be completed individually:

  - You may not copy files directly from another student.
  - You may not submit work in groups.
  - Collaboration with other students on labs/assignments should be limited to: general discussion and assistance with tool debug.

- There will be 5 labs throughout the term:
  - Labs are to be done outside the classroom on your own time.
  - Labs descriptions will be released on the day of lectures during weeks: 1, 3, 5, 7, and 9.
  - Labs will be due 2 weeks following their release at 7pm on Monday evenings prior to lectures. Labs should be submitted electronically via LEARN.
  - You are allowed to submit multiple times on LEARN; however, only the most recent submission will be graded.
  - All due dates are fixed. Late lab submissions will be penalized at a rate of 20% of the maximum grade per day. Late penalties may be waived by the course instructor under exceptional circumstances.

10 Paper Review and Presenation

- To keep up to date with the latest advances in the field requires the ability to read and understand information from technical papers.
- 5% of your final grade will be dedicated to a report of a recent paper from a circuits conference or journal (likely ISSCC 2014 or a JSSC 2014, but this will be finalize later in the term).
- The final lecture will be devoted toward presentations of each of these reports (also 5% of final grade).
- Reports and presentations must be completed individually, report length and presentation durations will depend on student enrollment in the course.

11 Illness

- A student who misses the final examination must provide:
  - A Verification of Illness form, or
  - Other documentation as appropriate
  - Please, try not to miss the final exam

12 Academic Offense

- Academic offenses include but are not limited to:
  - Infringing unreasonably on the work of other students
  - Cheating
  - Plagiarism
  - Misrepresentation
- All students should be familiar with the Universitys Policy 71 regarding Student Discipline
  - https://uwaterloo.ca/secretariat-general-counsel/policies-procedures-guidelines/policy-71

13 Plagiarism

- If one student copies from another student, both students are responsible regardless of the first students knowledge of the offense.
- The penalty for plagiarism on a lab/assignment is a mark of zero on lab/assignment in question with the potential for further consequences.
- All instances of plagiarism will be reported to the Associate Dean of Graduate Studies.
- The Associate Dean may increase the penalty at their discretion. This may include:
  - Retaking the course
  - The requirement for a course on ethics
  - A suspension
  - Expulsion