Defect Detection with Transient Current Testing and its Potential for Deep Sub-micron CMOS ICs

Manoj Sachdev*, Peter Janssen, and Victor Zieren

Philips Research Laboratories, WAY41, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands (*Currently at Univ. of Waterloo, Canada)

Abstract

Transient current testing (I_{DDT}) has been often cited as an alternative and/or supplement to I_{DDQ} testing. In this article we investigate the potential of transient current testing in faulty chip detection with silicon devices. The effectiveness of the I_{DDT} test method is compared with I_{DDQ} as well as with SA-based voltage testing. Photon emission microscopy is used to localize defects in several faulty devices. Furthermore, the potential of I_{DDT} testing for leaky deep sub-micron devices is investigated.

1 Introduction

Quiescent current testing (I_{DDQ}) is an important ingredient of the test suite for digital VLSI. The contributions of I_{DDQ} testing in quality improvement, test cost reduction, burn-in elimination have been well recognized [1]. However, the effectiveness of conventional I_{DDQ} testing in deep sub-micron is expected to be eroded owing to the increased sub-threshold current in MOS transistors [2-5]. Many solutions have been proposed to contain the increased sub-threshold leakage and are documented elsewhere [3,5,6]. These solutions include utilization of reverse biasing techniques to reduce the sub-threshold leakage in the test mode [3,5], utilization of Silicon On Insulator (SOI) technology for a sharper sub-threshold swing [7,8], or utilization of multi-threshold transistors to contain the sub-threshold leakage [9]. Moreover, containment of sub-threshold leakage is an important parameter for low power and device reliability consideration. Therefore, many low power circuit-level techniques have been devised to significantly reduce the sub-threshold leakage current.

Typically these solutions require non-trivial changes in the standard cell library or in the process. In many applications such as high performance VLSI, these solutions may pose several restrictions. CMOS processes for such devices are aggressively scaled (V_T and gate oxide) and optimized for switching speed. As a result, these devices are not I_{DDQ} testable. Therefore, ensuring gate oxide quality and reliability is becoming an increasingly difficult as well as an expensive task.

In this article, we investigate the potential of transient current testing (I_{DDT}) as an alternative/supplement to I_{DDQ} testing. The motivation of this research comes from the following reasons: (i) *To compare the effectiveness of I_{DDT} with respect to I_{DDQ} and voltage testing.* For a production test method, the reproducibility of the test method is of prime importance. (ii) *To investigate the feasibility of I_{DDT} based test techniques in a deep sub-micron environment.* Current-based test techniques are much more sensitive compared to voltage-based counter parts. Owing to several factors, in deep sub-micron voltage-based test strategies are unlikely to guarantee quality expectations. (iii) *To investigate the speed-up factor.* For I_{DDT} measurements, one does not have to wait till the current has reached the quiescent level. Hence, it is possible to enhance speed of the measurements. In other words, it is possible to perform I_{DDT} measurements at a significantly higher rate compared to I_{DDQ} measurements.

2 Previous Work

Some of the initial work on I_{DDT} was done by Frenzel and Marinos [10]. They simulated a small TTL circuit (few logic gates) assigning different sinusoidal waveforms on the inputs. They described complete power supply current as a signature of the Device Under Test (DUT). The signature of the DUT was compared with that of a golden device. In this manner a pass/fail criterion was established. Su and Makki [11] applied dynamic current monitoring techniques on SRAMs. To improve the defect detection capabilities of the dynamic current, they incorporated an extensive DFT strategy. The DFT scheme included separate V_{DD} and V_{SS} supplies for transient measurements, distributed switches to switch between the normal V_{DD} (V_{SS}), and a test V_{DD} (V_{SS}) only for dynamic current measurements. Furthermore, two dynamic current monitors and a set of controls are needed on the DUT. In their subsequent paper [12], the authors implemented the concept in silicon. The results reported showed that I_{DDT} is a better test method compared to I_{DDQ} and logic testing for open defects. However, the DFT implementation required is non-trivial and has implications for performance and area overhead.

Plusquellic et al. [13] proposed the concept of Transient

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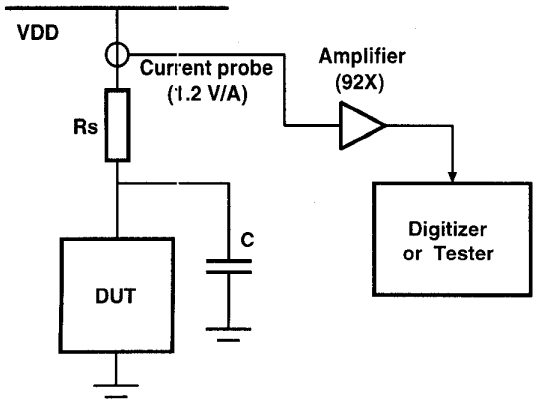


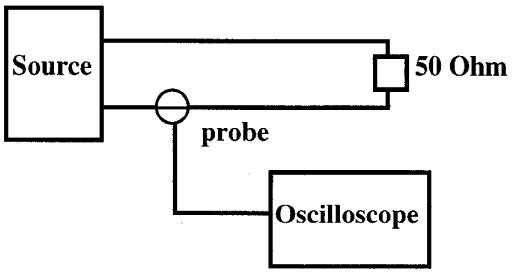
Fig. 1: The current-probe setup for I_{DDT} measurements.

Signal Analysis (TSA) with distributed measurement points. They argued that device physical characteristics such as substrate coupling and power supply or parasitic coupling contribute to the transient response of the DUT. Global V_T and gate oxide variations will cause measurable changes at all test points in the DUT. However, a local defect will affect transient response locally. The defect detection is accomplished in TSA by analysing the transient at all test points simultaneously so that defect-only information can be extracted in spite of global variations. They measured I_{DDT} across a resistor in the V_{DD} -line and transient voltages on the primary outputs. In their subsequent paper [14], they analysed the defective devices using correlation and regression analysis on frequency domain data.

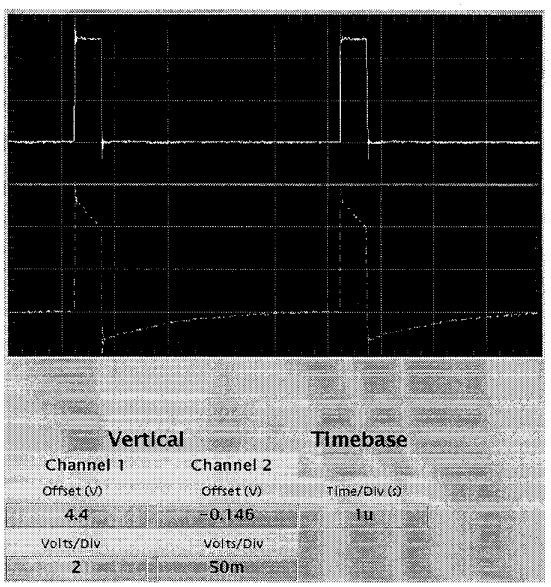
The V_{DDT} test method described by E.Cole [15] shows promising IC fault detection results. However, these V_{DDT} results are not compared to any other test method and are only performed on a few devices. The method described, strongly depends on the performance of a power supply (Keithley) which cannot be optimized for V_{DDT} testing. To prove the fault detection capability of this method, an oscilloscope was needed to show the difference in one particular test cycle between a good and a bad device. Because the transient current waveforms may differ in every cycle, probably, a comparison to a golden device is also required. However, this aspect is not explicitly mentioned in the paper. Furthermore, the maximum speed of their method is limited by ringing of the power supply level.

3 Experiment Description

The studies mentioned above, although highlighting the potential benefits of I_{DDT} testing, fail to provide conclusive evidence of the method's robustness and its application for production testing. Typically, very few devices were tested/analysed and the defect coverage of I_{DDT} was not compared with that of I_{DDQ} or SA based voltage tests. Moreover, extensive DFT implementations required to improve the defect resolution raise doubts about the practicality of these schemes.



(a)



(b)

Fig. 2: The characterization method (a) of the current probe, and graph (b) with stimuli (top) and response of the probe (bottom) (Hor.: 1 µs /div.).

Conceptually, our approach is also based on the golden signature of the DUT. However, unlike Frenzel and Marinos [10] we apply normal test stimuli on the DUT inputs. Furthermore, we do not describe complete power supply current as a signature (which is computationally expensive and not a practical solution for production testing). Moreover, in our approach only one sample of I_{DDT} is taken per

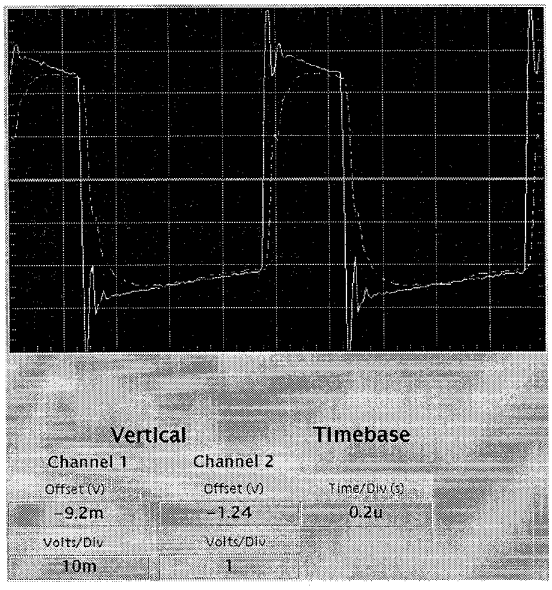


Fig. 3: Input (solid line) and output (broken line) of the amplifier (Hor.: 0.2 µs /div.).

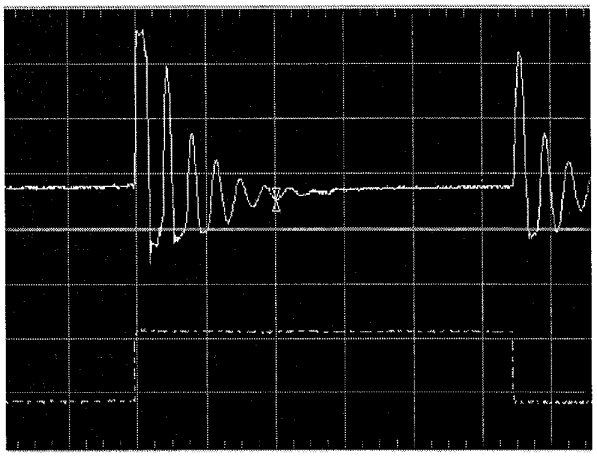
I_{DDT} test vector at a pre-determined instance. These vectors are pre-selected for their defect/fault coverage. The vector selection criterion is similar to that of I_{DDQ}. Finally, these samples are compared with those of a golden device for a pass/fail decision.

3.1 The Setup

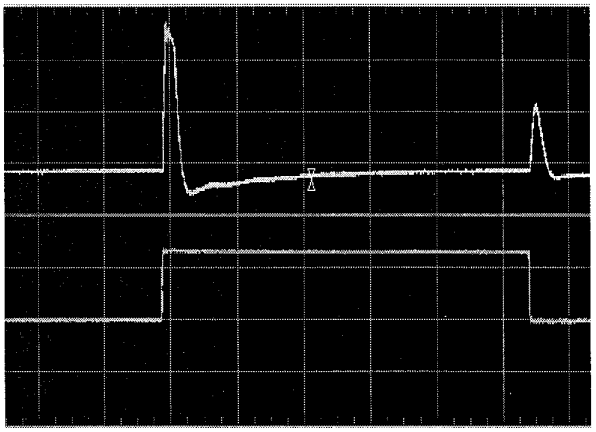
The experimental setup for I_{DDT} measurements is illustrated in Fig. 1. The setup includes the DUT, a decoupling capacitor (C), a series resistor (R_s), a current probe (EG&G COP-1), an amplifier and a tester (HP82000) or a digitizer (HP E1429). The digitizer has 10 effective bits. The selected range of the digitizer is +/- 1 V. Therefore, its resolution is 2 mV. The current probe is an inductively coupled device which is placed around the V_{DD} line. The current probe is only sensitive to the transient behavior and is insensitive to the DC level.

The behavior of the current probe has been characterised as illustrated in Fig. 2. The schematic in the figure illustrates the characterisation setup. A pulse of 5 V and frequency of 200 kHz is applied across a 50 Ω resistor. The input of the probe is coupled to one of the leads of the resistor. The graph in the figure (measured with a LeCroy 9400 oscilloscope) illustrates the input pulse (top) and the response through the probe (bottom).

This inductively coupled system ensures a transfer of the



(a)



(b)

Fig. 4: Clock signal (lower trace) and transient signal (upper trace) measured with (a) R_s = 0 Ω and C = 0 F, (b) R_s = 6 Ω and C= 0 F (Hor.: 1 µs /div.).

transient (step response) of the supply current (I_{DD}), whereas the system also acts as a high pass filter. The behavior of the probe is visible from its response which is depicted by the bottom signal (broken line) in the graph of Fig. 2. There, the output of the probe shows an undershoot. The trans-impedance of this probe was measured to be 1.2 V/A. The output of the probe is amplified for an improved resolution.

In general, the performance of the system is limited by the current probe. Hence, the specifications of the amplifier seem relaxed. However, the amplifier slew rate should be high enough to maintain linearity and the bandwidth small enough to block ringing. An amplifier configuration was

bread-boarded. Fig. 3 illustrates the response of the probe (solid line) and the output of the amplifier (broken line). The gain of the amplifier is 92. Hence, the overall trans-impedance of the probe and amplifier is 110 V/A. The output of the amplifier was sent to the tester comparator (HP82000) or a digitizer (HP E1429) depending upon the requirements.

3.2 The Device Under Test

No particular attempt was made to select a particular vehicle type. The selection of the vehicle was influenced by the availability of design in the state of the art technology as well as its testability with SA and I_{DDQ} testing. The DUT is a multi-channel audio decoder IC designed in 0.5 µm n-well triple metal CMOS technology. It has an area of 218 mm^2 and worst-case operating speed is 27 MHz. The device contains Cell Based Array logic, two DSP cores with an equivalence of about 142 k gates, and six SRAMs .

3.2.1 Logic and I_{DDQ} Tests for the DUT

Logic in the DUT is tested with full scan methodology. More than 500 k test vectors were generated with the proprietary Philips ATPG tool, AMSAL, for logic testing. The test vectors have a SA fault coverage of greater than 95%. All embedded RAMs are tested with on-board BIST. The V_{DD} supplies for RAMs and peripherals are isolated from that of the logic.

Logic in the DUT is also tested with I_{DDQ}. The I_{DDQ} test vectors were automatically generated by the AMSAL ATPG tool. A total of 9 I_{DDQ} test vectors was identified. However, 2631 scan shift operations were also generated to put the DUT in proper logic conditions for these I_{DDQ} test vectors. The I_{DDQ} was measured by the tester's DPS (Digital Power Supply) after the logic test and pass/fail information was logged in for subsequent comparative analysis. Owing to BIST and the embedded nature of RAMs, it was very difficult to perform I_{DDQ} and I_{DDT} testing on RAMs. Therefore, in this experimental study the analysis was performed only over the logic part of the chip.

3.2.2 I_{DDT} Response Determination for the DUT

Figures 4(a) and 4(b) illustrate the clock and I_{DDT} signals to the DUT in different circumstances. Fig. 4(a) shows the measured response when R_s is 0 Ω and C is 0 F. Assuming all flip-flops in a DUT are positive-edge triggered, at the instance of a positive clock transition, a large transient current flows through the V_{DD} pin. On the negative going transition, a relatively small transient current flows due to clocking activity related changes within flip-flops. In our case an appreciable amount of transient current flows on the negative transition of the clock, because the DUT contains a large number of negative-edge triggered flip-flops.

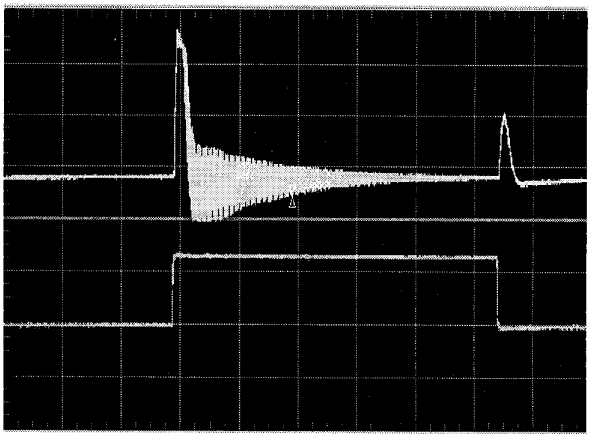


Fig. 5: The clock signal (bottom) and superimposed I_{DDT} responses (top) of a failed IC (Hor.: 1 µs /div.).

The V_{DD} line has a largely reactive (inductive and capacitive) load which results in an under-damped system. Due to this nature, there are oscillations or ringing on the V_{DD} line which are clearly visible in Fig. 4(a). These oscillations would seem to make I_{DDT} measurement and fault detection with I_{DDT} a very difficult task. However, an under-damped V_{DD} line can be made over-damped with changes in its impedance, i.e. by appropriate selection of R_s. Since this behavior is DUT and test-vector dependent, some trial and error experiments are needed to find out a smooth transient current waveform. Alternatively, one could also decide to model the RCL circuit, in order to determine the optimum (critically) damped response. For production testing the empirical way is probably preferred, as modelling would require a precise knowledge of the lumped model parameter values of the DUT and the load board.

The decoupling capacitance (C) is in parallel with the DUT capacitance and only slightly influences the damping behavior of the transient current. Furthermore, there are tester related constraints on the maximum value of the decoupling capacitance that can be driven by the tester parametric measurement unit (PMU). For the DUT of this experiment a decoupling capacitance of 100 nF is used for voltage and I_{DDQ} testing. However, removing the capacitance further improved the transient current behavior as well as the defect resolution of I_{DDT}. This is owing to the fact that in the modified situation, all the transient current is supplied to the V_{DD} pin. Therefore, defect behavior is not masked by the current supplied by C during the transient. For the DUT of this experiment, we found an optimum R_s of 6 Ω. Fig. 4(b) depicts the transient current response for this optimum R_s value and C = 0 F.

It is equally important to find out which transient current segments are sensitive to defects. In other words, where

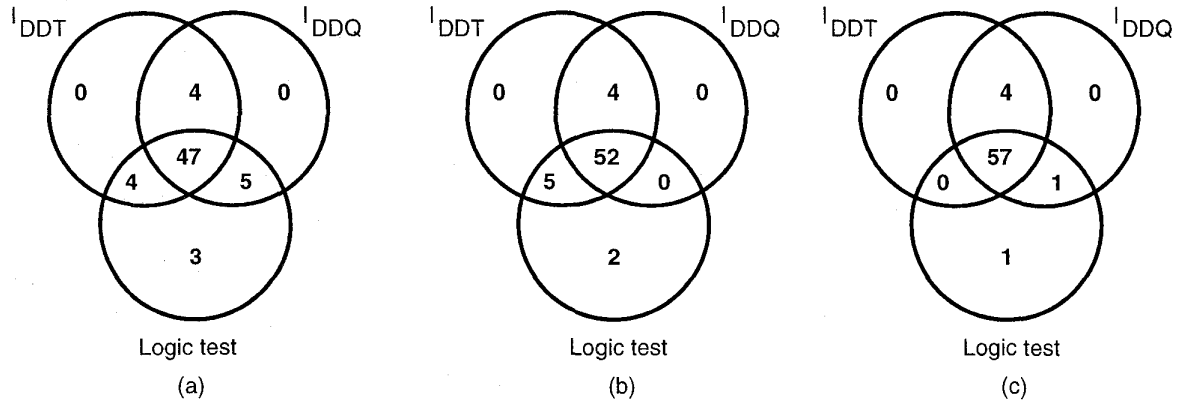


Fig. 6: Comparison of logic, I_{DDQ} and I_{DDT} testing on failed devices, (a) with global I_{DDT} pass margin, (b) with individual I_{DDT} pass margin for each I_{DDT} test vector, and (c) with individual I_{DDT} pass margin but with larger number of I_{DDQ} test vectors, measured with an I_{DDQ} monitor.

the difference between a defective and the defect-free signature will be most visible. Fig. 5 shows the clock signal and the I_{DDT} responses of a failed device. The I_{DDT} responses of several I_{DDT} test vectors are superimposed over each other. These responses should be individually compared with that of a good device illustrated in Fig. 4(b), (also superimposed). It is apparent that the variation amongst the I_{DDT} responses due to a fault is largest just after the peak. The difference becomes smaller as the transient settles down. In other words, the signal tends towards its DC level. Furthermore, after the peak, golden device responses consistently demonstrate a region where the transient signal is decaying (and even may become negative). This region is visible in Fig. 4(b) and such a response is achieved if the trailing edge of the current pulse is differentiated. This region, where the golden device signature is stable, provides a good reference for fault detection. When the signals are sampled at the right moment, i.e. when the golden device has its minimum, the difference between the DUT response and that of the golden device provides the key for fault detection. It appears that this detection method in one cycle provides information of not only the peak and the quiescent current level of that cycle, but also of the quiescent level of the previous cycle.

4 Experimental Results

A total of 238 devices was tested in this study. In the first part of this study, these devices were tested with SA fault based test patterns as well as with I_{DDQ} test vectors. A subset of good devices, i.e., those devices that passed logic as well as I_{DDQ} tests, was utilized to determine the golden device I_{DDT} response. The response of the DUT was digitized at a fixed moment (see Section 3.2.2) with respect to the positive clock edge. This is to ensure a robust fault detection with the I_{DDT} test method. In this study, we experimented with two different methods for setting the pass/fail I_{DDT} thresholds. In the first method, a single, global pass margin was determined for all I_{DDT} test vectors by which lower and upper threshold limits were defined for the DUT. In the second method, the pass/fail criterion was refined. The lower and upper limits were identified for each I_{DDT} test vector.

A total of 2640 I_{DDT} samples was taken in this experiment for exploring the potential of this test method. The large number of samples was feasible by virtue of the relatively high I_{DDT} sample speed.

4.1 Result of the Experiment with a Global I_{DDT} Margin

For global I_{DDT} margin setting, golden device responses of I_{DDT} vectors were sampled and measured. Within the set of golden devices a maximum and a minimum were determined of the output of all vectors. A margin of 10 mV (which is equivalent to 90 µA transient current in the V_{DD} line) was set to enable an unambiguous pass/fail decision. In other words, a DUT is considered faulty if its global response is at least 10 mV larger than the global maximum (or smaller than the global minimum) of the golden device response. The value of 10 mV was set to account for the small number of golden devices used as such, as a statistically more meaningful number probably would yield more spread and, thus, a larger margin. In general, the limit setting for I_{DDT} , similar to I_{DDQ} testing, depends on required test quality. Setting up global limits allows us

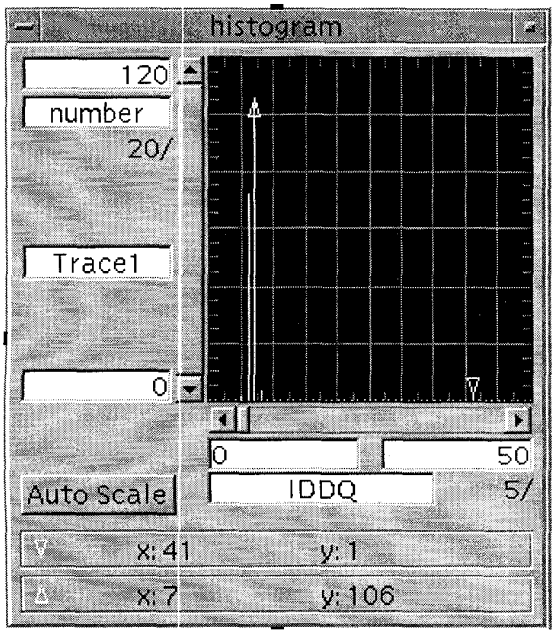


Fig.7(a): $I_{DDQ,max}$ distribution of all tested devices. (Hor.: 5 μA/div, 1 μA bins).

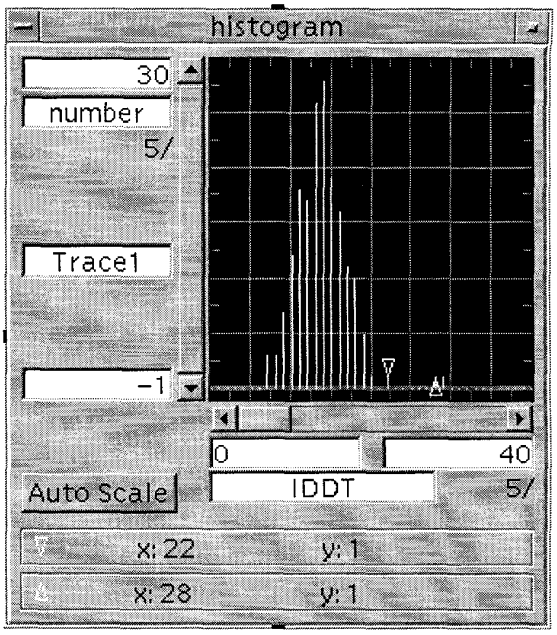


Fig. 7(b): $|\Delta I_{DDT}|_{max}$ distribution of all tested devices. (Hor.: 5 mV/div, 1 mV bins).

to use the comparator of a purely digital tester for the pass/fail decision without time-consuming data processing.

Fig. 6(a) illustrates the results of this experiment. The fault detection capability of the I_{DDT} test is compared with that of I_{DDQ} and logic SA test methods by means of the Venn diagram. It is apparent that most of the faulty devices (47) were failed by all three test methods. There are 3 failures that were detected only by the logic test. There are 4 failures that could not be detected by logic test, but were detected by I_{DDQ} and I_{DDT} test. Furthermore, 4 failures were detected by the I_{DDT} and the logic test but were not detected by the I_{DDQ} test. Similarly, 5 failures were detected by the I_{DDQ} and the logic test but were not detected by the I_{DDT} test. From this experiment we broadly concluded that in spite of the global I_{DDT} pass margin, the method was able to give comparable fault detection coverage with respect to logic test and I_{DDQ} test.

4.2 Result of the Experiment with Individual I_{DDT} Margins

The positive results of previous experiment encouraged us to strive for further improvement in this I_{DDT} measurement technique. Arguably, transient response may be affected significantly owing to the nodal activity within the DUT which is test-vector dependent. Therefore, there may be large, test-vector dependent variations in transient responses and a single set of pass/fail limits for all I_{DDT} test vectors may not be effective in catching faulty devices. Hence, lower and upper pass/fail limits were set for each I_{DDT} test vector. Vector-to-vector variations within one die, therefore, do not cause a detection problem.

Similar to the previous method, a margin was incorporated in setting the upper/lower limits. The absolute value of the difference between the I_{DDT}-output of an average golden device and that of the DUT ($|\Delta I_{DDT}|$) was set at a maximum of 25 mV (which is approximately equivalent to 226 μA transient current in the V_{DD} line) for each vector. Setting individual limits for each I_{DDT} test vector does not allow usage of the tester comparator. Therefore, the output of the I_{DDT}-monitor was sent to a digitizer.

Fig. 6(b) illustrates the result of the second method, i.e., with an individual pass/fail margin for each I_{DDT} test vector. The fault coverage of the logic and the I_{DDQ} test remains the same. However, the coverage of I_{DDT} increased significantly. In this experiment, the I_{DDT} detected all the I_{DDQ} failures, including 5 I_{DDQ} failures that were not detected by I_{DDT} in the previous experiment. In addition, I_{DDT} test also detected one more logic failure that was not detected by I_{DDT} in the previous experiment.

Fig.7 shows the histograms of the (a) I_{DDQ} and (b) I_{DDT} tests of Fig. 6(b). In Fig. 7(a) the maxima of 9 I_{DDQ} cycles were used, as measured by the DPS of the tester. There are four bins (of 1 μA) with 182 passing devices out of a total of 238. The maximum I_{DDQ}-value of a passing device is 8

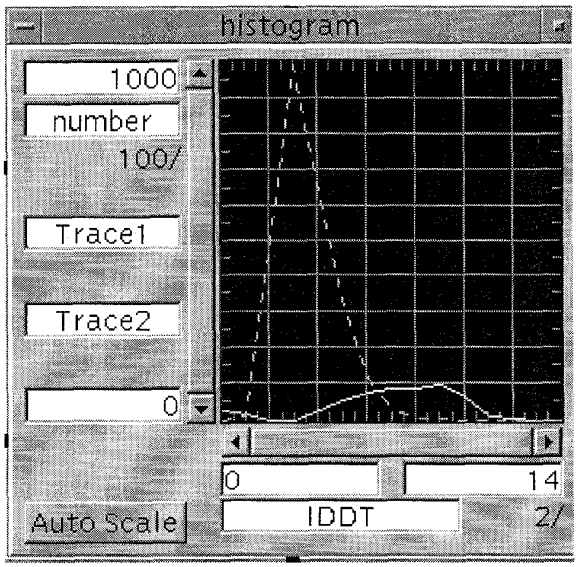


Fig. 8: I_{DDT} distribution of a golden device (broken line) and a failing device (solid line). (Hor.: 14 bins between -600 and -300 mV).

μA (where it should be noted that the DPS accuracy is about 5 μA). The second marker is pointing at the first failure (at 41 μA), such that a margin of 33 μA exists. Fig. 7(b) shows the histogram of maximum $|\Delta I_{DDT}|$-values of 238 devices. The first marker indicates the highest value for the 177 passing devices at 22 mV. The second marker is placed at the lowest value for the failing devices (28 mV). This explains why the 25 mV threshold was chosen. The 6 mV gap between good and faulty is rather small and improvement of the signal-to-noise ratio is needed, mainly by replacing the bread board monitor design by a monitor with a larger trans-impedance placed on the load board.

4.3 Fault coverage with a Large Number of I_{DDQ} Test Vectors

In order to benchmark I_{DDT} with respect to conventional I_{DDQ} testing, we repeated the I_{DDQ} test using all I_{DDT} test vectors. Application of an improved version of the QuiC-Mon monitor [16] allowed us to measure 2640 I_{DDQ} test vectors in an acceptable time. The result of this experiment is illustrated in Fig. 6(c). All 5 failures that were I_{DDT} detectable and were not detected by the I_{DDQ} test (Fig. 6(b)) are now also detected by I_{DDQ} test. Furthermore, one failure that was only detected by logic test is now also detected by I_{DDQ} test. Therefore, the extended I_{DDQ} test detected 6 additional failures.

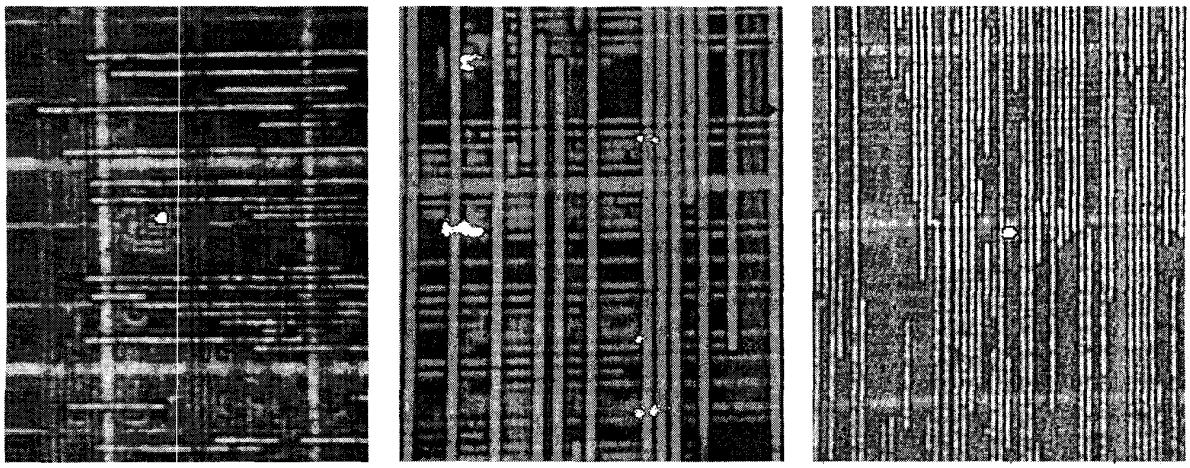
Several conclusions can be drawn from this experiment. First of all, extra I_{DDQ} test vectors give rise to a higher fault coverage. The initial 9 I_{DDQ} test vectors were generated with node toggle constraints. It appears that there are some bridges that are not excited by this small number of test vectors. Secondly, as expected, the cumulative fault coverage grows slowly with increasing number of I_{DDQ} test vectors. Thirdly, given the same number of test vectors, the coverage of I_{DDQ} and I_{DDT} is comparable, but I_{DDQ} detects one extra failure. A closer observation showed that this extra failure could only be detected at a critical sampling moment and not in a true quiescent state. This behavior has also been confirmed by photon emission microscopy (see Section 5). Probably, there is a floating gate that, due to a slow ramp on that node, gives rise to a high, but delayed, current peak.

4.4 I_{DDT} Distributions

Fig. 8 illustrates I_{DDT} distributions of a failed device (solid curve) and that of the golden device (broken curve). The I_{DDT} distributions of both devices for all I_{DDT} test vectors (2640) are plotted in this figure. The X-axis represents the values of the I_{DDT} responses between -600 and -300 mV. The Y-axis depicts how often the DUT response falls in a given bin. The graph representing the golden device has a smaller spread in its response compared to that of the faulty device. For a significant number of I_{DDT} vectors, the response of the faulty device has a larger transient current than the golden device.

5 Defect Diagnostics

In order to find possible relations between fault detection methods and the defects forming the root cause of the fault, photon-emission microscopy (PEM) was applied on samples from the various classes as depicted in the Venn diagram of Fig. 6(c). The devices were plastic encapsulated in QFP160-type packages and about 10 samples were selected and etched open. Only three devices showed an unaltered behaviour after this treatment. Fortunately, all were from a different group. The DUT was placed in a PEM setup and driven by the tester. Then the DUT was halted just after one I_{DDQ} cycle showing significant DC-current. Photon emission could be detected from all three samples, as is illustrated in Fig. 9. The emission spots are brightly white. In Fig. 9(a) a sample is shown to emit on one spot in the CBA logic (no memory was powered up here) which failed all three tests. Fig. 9(b) shows a detail of a second device which appeared to have 10 emission spots, of which 5 are visible in the micrograph. This device passed the SA fault test, but failed on I_{DDQ} and I_{DDT}. Finally, Fig. 9(c) depicts the third and most interesting device which failed on SA test but, initially, could not be detected by I_{DDQ}. Also, no photon emission was detected in



(a) (b) (c)

Fig. 9: Photon emission microscope images of 3 devices (a) failing SA, I_{DDQ} and I_{DDT} tests, (b) failing I_{DDQ} and I_{DDT} and (c) failing SA and I_{DDQ} test (only at a critical sampling moment). The width of the photomicrographs corresponds to: (a) 98 μm, (b) 74 μm and (c) 118 μm.

the situation where the device was halted! Only in a dynamic, i.e. a cyclic run test we found the emission spot visible in the centre of the picture. This corresponds to our finding that the device does not show a raised I_{DD} in the true quiescent state. However, a critical timing of the sampling moment for the I_{DDQ}-monitor appeared to be necessary: 17 μA was measured about 10 μs after the positive clock edge (frequency was about 70 kHz). I_{DDT} was not capable of detecting this malfunctioning device, probably because the resolution is not yet high enough. All emission spots were found on different locations and we tried to find the root-cause defects. Optical microscopy analysis could not result into a defect localization. After removing the protective oxi-nitride layer SEM observations unfortunately did not reveal any defective opens or shortcircuits in the neighbourhood of the emission spots.

6 Deep Sub-micron CMOS Potential of I_{DDT}

The sub-threshold leakage is expected to increase substantially for deep sub-micron devices. As a consequence, ICs may have significantly higher background current or I_{DDQ}. Arguably, as long as background leakage can be filtered from the defective transient current, I_{DDT} can be an effective test method for such leaky devices. Since inductively coupled current probes are insensitive to the DC levels, the proposed technique should be effective in a leaky environment.

An experiment was set up to verify the validity of the technique in higher background current. In the setup (see Fig. 1) a variable resistor ($R_{leakage}$) was introduced parallel to a known good DUT (golden device). Hence, a known background leakage was introduced in the I_{DDT} measurement. The I_{DDT} response was measured at several values of the background leakage and was compared with the I_{DDT} response without the background leakage. Fig. 10 shows I_{DDT} responses without any background leakage and with a 3 mA leakage. As it is apparent from the figure, the I_{DDT} signature does not vary with changes in the background leakage. In other words, the background leakage does not influence fault detection capability of the technique.

As the spread in transistor parameters such as L_{eff} and V_T in deep sub-micron process generations will increase [17], inter-vector and inter-die I_{DDQ} spread will be larger as well. This is also the conclusion of I_{DDQ} measurements on state-of-the-art silicon. The DUT of this experiment contains 3 DSPs with an area of 2.2 mm^2 each and is processed in a 0.25 μm technology with a nominal supply voltage of 2.5 V. Each DSP has its own supply pin. The average I_{DDQ} background current of good devices is about 30 μA and the vector-to-vector spread is 5 μA. Their maximum I_{DDQ} value is 45 μA (@T_{amb}). The I_{DDQ} leakage exhibited a very high temperature sensitivity. A total of 123 I_{DDQ} (and I_{DDT}) measurements was taken. In addition, 22828 scan vectors were needed to put the DUT in the required logic states for these measurements. For these chips an external decoupling capacitor (C) of 10 nF was added to slow down the transient waveform, which makes the timing of I_{DDT} testing less critical. The measurements were performed on a small set of 12 DSPs owing to the

unavailability of a larger number of samples. They were used for comparison between I_{DDQ}, I_{DDT} and SA voltage testing. For most DSPs the fault-coverage of all 3 methods was the same. However, there are two remarkable exceptions. One device which failed the I_{DDT} and SA voltage test could only be rejected by I_{DDQ} testing when sampling fast enough after the active clock edge. In our previous experiment (see Section 4) we have seen a similar behavior. However, in this latter experiment, I_{DDT} is capable to detect this faulty IC. Furthermore, one device was only failing the I_{DDT} test. The SA voltage test was initially performed at a low frequency of 100 kHz with zero errors Increasing the test frequency to 10 MHz resulted in a lot of fail vectors. Studying the I_{DDQ} results of this device, we found abnormally low I_{DDQ} currents (max. 7 μA) compared to other good parts (average 30 μA). This confirms the statement of Intel [6] that there is a relation between the max. speed (F_{max}) and the I_{DDQ} current, but shows also the potential of I_{DDT} testing in detecting devices which do not run at their nominal (= specified) speed. For future technologies we expect larger I_{DDT} variations over devices and cycles, which might result in a more difficult comparison with a golden device.

7 Discussion: Issues in I_{DDT} Testing

Some of the issues in I_{DDT} testing are similar to that of I_{DDQ} testing. For example, floating nodes may have a very unpredictable behavior for both methods. Therefore, it is important that all nodes should have hard logic values (and have not been set in a wrong state). Furthermore, dynamic circuits may potentially invalidate an I_{DDT} test. However, further research is required to establish the effectiveness of I_{DDT} test for dynamic circuits. Similarly, initialization plays an important role in robust I_{DDT} testing. A DUT without proper initialization may have undefined nodal states that may invalidate the test.

Reproducibility of the test is an important criterion for production testing. In general, these issues can be sub-divided into (i) DUT related issues, and (ii) I_{DDT} instrumentation related issues. The former category includes the method's ability to work for different DUT types and under statistical variations within the processing window. It might imply the use of wafer statistics to determine the pass/fail criterion per wafer (moving limits). This aspect is a subject of future research. The latter category includes the sensitivity of the pass/fail criterion on the selection of R_s and C, sampling moment, behavior of the probe and amplifier. The selected values of R_s and C should be able to damp I_{DDT} ringing of the DUT. Our experience suggests that a sampling moment uncertainty of a couple of nano-seconds does not influence the fault detection capability. This is because the pass/fail information is available

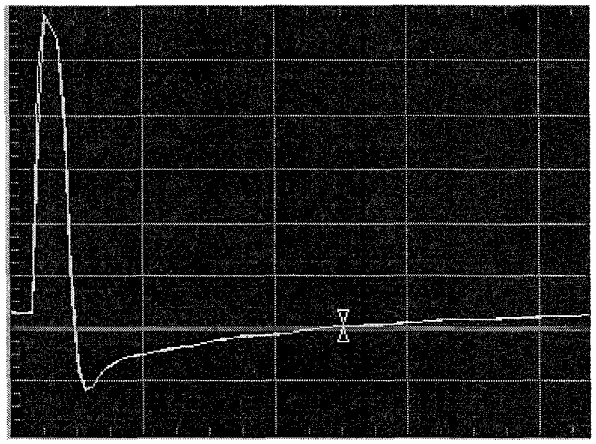


Fig. 10: Almost undistinguishable I_{DDT} - responses with 3 mA background leakage and without any background leakage (Hor.: 1 μs /div.).

on a much wider time scale, due to the inclusion of R_s and C. This implies that even very fast circuits can be measured under more relaxed timing conditions. For example, in Fig. 10 the horizontal axis represents 1000 ns/div.

With technology scaling, operational frequency and complexity of ICs is increasing significantly. Therefore, measurement speed of a test method is an important aspect. Although conceptually, I_{DDT} and I_{DDQ} measurements are different, it is relevant to benchmark I_{DDT} measurement speed with that of I_{DDQ}. Within Philips Semiconductors, often I_{DDQ} measurements are carried out with the QuiCmon I_{DDQ} monitor [16]. The average settling time for a transient before an I_{DDQ} measurement can be carried out is 10 μs. This time translates to an I_{DDQ} test speed of about 100 kHz.

Potentially, I_{DDT} can be carried out at a much higher rate compared to the I_{DDQ} testing. In this experimental study the components are not particularly optimized for measurement speed. Yet, we could achieve the measurement frequency of 1.5 MHz. This implies that **the I_{DDT} test is approximately 15 times faster than the I_{DDQ} test**. However, high frequency current probes up to 200 MHz are readily available from commercial vendors [18]. Similarly, a better, faster amplifier may be implemented for higher measurement speed. Therefore, a higher I_{DDT} measurement speed seems feasible in the future at the expense of a more critical timing. Nevertheless, improving the measurement speed remains one of the future topics for research and is beyond the objectives of this article.

8 Conclusion

I_{DDQ} measurement is an important aspect of VLSI testing. Its contribution in ensuring device quality and reliability is well-known. With scaling of technology, the effectiveness of I_{DDQ} testing is expected to be eroded due to increased sub-threshold leakage. Many design and technology solutions have been proposed to enhance I_{DDQ} testing in deep sub-micron. Most of these solutions require non-trivial design and/or process changes which may not be acceptable for many application areas such as high performance ICs.

In this article the potential of transient current testing is evaluated as an alternative to I_{DDQ} testing and its potential for deep sub-micron VLSI testing is explored. The results of conducted experiments, **conclusively** prove the potential of I_{DDT} testing in catching device failures in the presence of raised background current levels. For the devices used in this study the performance of the I_{DDT} test method is found to be comparable with that of I_{DDQ} and logic testing. Furthermore, the I_{DDT} test can be carried out at a significantly higher speed (15x) than the I_{DDQ} test. The expected increase in die-to-die spread of deep sub-micron transistor parameters, such as L_{eff} , will have its impact on the applicability of current-based testing. For I_{DDT} this will have to be investigated more thoroughly, combined with items such as simulation, vector optimization, adaptive pass margin, applicability to memories, and design of a more flexible I_{DDT} monitor.

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