A Parametric Stability Fault Model for Embedded SRAMs

Andrei Pavlov[1], Manoj Sachdev[1]

[1]University of Waterloo, 200 University Ave. W., Waterloo, Ontario, Canada, N2L 3G1
apavlov@vlsi.uwaterloo.ca,
msachdev@vlsi.uwaterloo.ca

José Pineda de Gyvez[2]

[2]Philips Research Labs, Prof. Holstlaan 4, 5656AA Eindhoven, The Netherlands
jose.pineda.de.gyvez@philips.com

Motivation

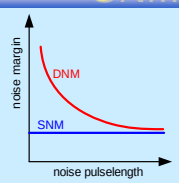
- System on Chips (SoCs) are memory intensive
- Scaled technologies →Larger process spread →Increasing shift towards parametric faults
- Noise in SoCs → data integrity at risk → need for stability characterization and specification
- Embedded memories are ***yield limiters*** of SoCs

Introduction

SoC are becoming memory intensive. However, the increasing process spreads of modern scaled-down technologies result in a growing number of parametric faults in embedded SRAMs [1]. Moreover, large switching and substrate noise imposes even more stringent requirements on the SRAM robustness.

Process variations, the presence of non-catastrophic defects and voltage ripples can cause parametric stability faults in SRAMs. Since the dynamic noise margins are always larger than static, we applied the Static Noise Margin (SNM) defined by [2,3] to develop our fault model. Low SNM indicates poor cell stability. Such cells are termed "weak". A weak cell can inadvertently flip due to noise which can be tolerated by a good cell.

SNM and DNM

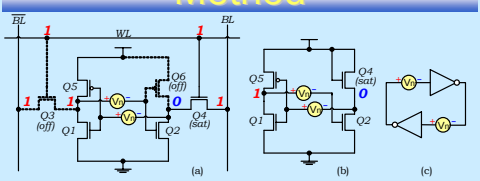


Static noise sources:
- operation conditions variations
- process offsets and mismatches

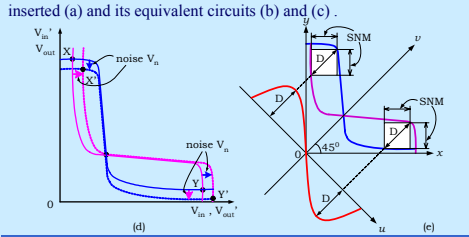
Dynamic noise sources:
- α-particles
- cross-talk
- ripples in the power and signal buses

DNM= *f* (noise energy, capacitive load, circuit speed)

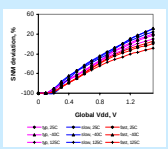
Method



Read accessed SRAM cell with static noise voltage sources Vn inserted (a) and its equivalent circuits (b) and (c) .

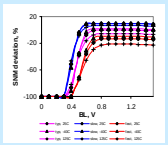


SNM vs. operational voltages



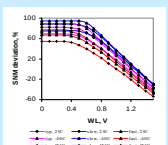
SNM vs. power supply voltage

- V_{DD}=V_{WL}= V_{BL} were all varied at once from 0V to 1.5V
- SNM shows practically linear dependence on the supply voltage



SNM vs. the bitline voltage

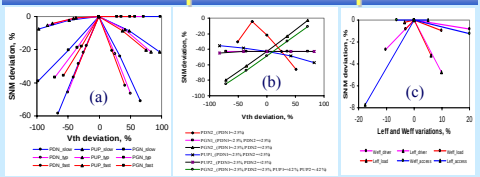
- V_{DD}=V_{WL}=V_{BLB} =1.2V, V_{BL} was varied from 0V to 1.5V
- SNM starts to collapse once the access nMOS turns ON



SNM vs. the wordline voltage

- V_{DD}=V_{BL}=V_{BLB} =1.2V, V_{WL} was varied from 0V to 1.5V
- SNM starts to collapse linearly once the access nMOS turns ON

SNM vs. process spread



SNM vs. process spread

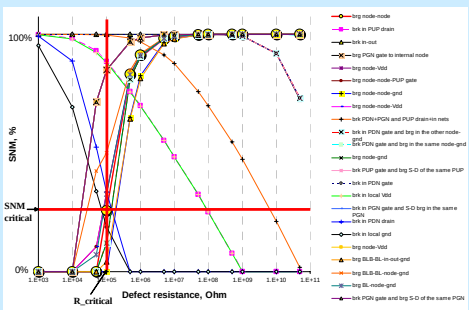
"0" point corresponds to the typical values

a) V_{TH} of only one transistor was changed at a time

b) SNM vs. V_{TH} combinations demonstrates steeper dependencies. For many combinations of V_{TH} deviations SNM reduces to zero.

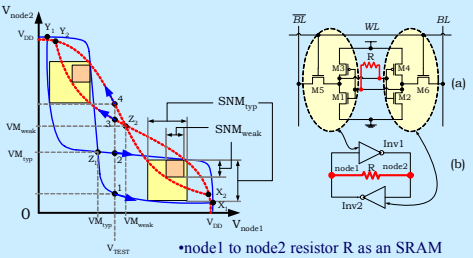
c) Varying L_{eff} or W_{eff} of one cell transistor has relatively minor effect on the SNM.

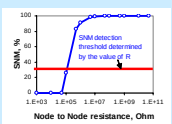
SNM vs. defect resistance



Non-catastrophic resistive defects were injected into the SRAM cell layout and the SNM vs. the defect resistance was measured. All other operating conditions were kept typical. Resistive opens and resistive bridges have distinctively different effect on the SNM.

Fault model





- node1 to node2 resistor R as an SRAM stability fault model
- R is a simple and reliable cumulative representation of the reasons causing SNM reduction
- By varying the value of R we can modify the SNM of the target SRAM cell. Such a weakened cell can be used to verify and compare the techniques aimed at weak cell detection.

Conclusions

An SNM-based SRAM parametric stability fault model is proposed. The proposed fault model allows simulating SRAM cells with marginal stability. Moreover, the fault model makes it feasible to compare and fine-tune DFT techniques aimed at the detection of SRAM with marginal stability.

References

[1] J. Segura et al., Int. Test Conf. (ITC), pp. 90-99, 2002.
[2] J. Lohstroh, IEEE JSSC, Vol. SC-14, No.3, pp. 591-598, 1979.
[3] C. Hill, Mullard Tech. Com., No.89, pp. 239-245, 1967.
[4] E. Seevinck et al., IEEE JSSC, No.5, pp. 748-754, 1987.
[5] Carafe IFA tool: http://sctest.cse.ucsc.edu/carafe/
[6] J. Houser, IEEE Trans. on Educ., No.4, pp. 363-368, 1993.
[7] A. Meixner et al., ITC, pp. 1043-1052, 1997.
[8] C. Kuo et al., US patent 5,034,923, 1991.