AN SRAM WEAK CELL FAULT MODEL AND A DFT TECHNIQUE WITH A PROGRAMMABLE DETECTION THRESHOLD

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Abstract

SRAM cell stability has become an important design and test issue owing to significant process spreads, non-ideal operational conditions, and subtle manufacturing defects in scaled-down geometries. In this article, we carry out an extensive SRAM SNM sensitivity analysis and propose an SRAM cell stability fault model for weak cell detection. This fault model is used to design and verify a proposed digitally programmable design-for-test (DFT) technique targeting the weak cell detection in embedded SRAMs (eSRAM).

1 Introduction and Motivation

Systems on a Chip (SOC) are becoming memory intensive. Embedded memories can occupy up to 70% of the total SOC area [1]. Owing to the higher robustness compared to DRAMs, embedded SRAMs (eSRAM) are often used in SOC applications. However, because of the high density it is thus not surprising that eSRAMs are the yield limiters in SOCs [2]. The increased process spreads of modern scaled-down technologies and non-catastrophic defect related sensitivity to environmental parameters cause stability faults in SRAMs [3, 4]. We refer to the cells causing such faults as to *weak cells*.

Weak cell failures are random because the cells are not entirely damaged and the state flipping may be triggered only under certain operating conditions. For instance, if an SOC with an embedded SRAM is used in a battery-operated device, with battery discharge, weak cells may cause a failure of such an SOC while other blocks might still have been operating.

The cell weakness is typically a result of resistive defects, excessive process shifts, transistor mismatch, IR drops, etc. The state flipping of a weak cell may occur due to any electrical disturbance such as power supply noise, read/write cell disturbs, etc. during the normal operation of the SRAM. These adverse conditions, especially combined, can cause a weak cell to flip its state easily and corrupt its contents.

In this paper, we make use of a new metric to quantify the level of weakness of such cells. This metric is based on the cell's Static Noise Margin (SNM) [5]. We define *weak cells* as the cells with insufficient static noise margin. Such cells can inadvertently flip their state, as a reduced SNM indicates poor cell stability. Observe that a stuck-at cell corresponds to a special case of weakness when the SNM is zero.

SNM provides an excellent figure of merit for SRAM cell stability design and analysis. Several SNM definitions can be found in the literature and are discussed in detail in [5]. In this work, we used the SNM definition initially proposed by Hill [6] and further developed by Seevinck, List and Lohstroh [7]. Furthermore, the metric goes hand in hand with the newly proposed parametric stability fault model for weak SRAM cells. We believe that the development of a weak cell fault model for SRAMs is crucial for investigation and comparison of the effectiveness of various test algorithms and techniques as well as for stability characterization of SRAM designs.

Reading a 6T SRAM cell with bit lines precharged and equalized at V_{DD} may not detect several types of defects, e.g. a missing P-channel in pull-up transistors, poor or absent vias to the pull-up transistors (an SRAM cell in this case will act as a "good" 4T DRAM cell). Detection of such cells in SRAM arrays may require a Data Retention Test (DRT). However, for large memory instances, DRT can take significant time leading to a more expensive test. Moreover, for stricter PPM levels, some cells may require excessively long DRT delay times, reduced supply voltage and high temperature. For this reason, several weak cell detection techniques have been proposed [8, 9, 10]. These techniques are effective and are widely used in the industry. They offer significant test time and cost reductions over the DRT, and, besides the data retention faults, they are also capable of detecting weak cells.

Detection of structural defects in SRAM cells allows to screen out devices with potential long-term reliability problems. Some techniques are developed to target specific types of fabrication defects, e.g., highly resistive bit-line contacts [11].

However, these techniques lack easy programmability to provide a detection mechanism for several levels of cell weakness. In this article, we propose a digitally programmable DFT technique capable of detecting cells with varying degree of weakness. The proposed fault model mimics SNM degradation due to structural defects and/or process spread and/or variation of the operating conditions.

This paper is organized as follows: Section 2 presents an extensive sensitivity analysis of a 6T SRAM's SNM. Section 3 describes the proposed *weak cell fault model*. Section 4 explains the concept of programmable weak cell detection threshold. Section 5 introduces the *proposed DFT* for detection of weak SRAM cells. In Section 6 we draw the conclusions.

2 SNM sensitivity analysis

A 6T SRAM cell and its corresponding voltage transfer characteristic (VTC) for a non-ideal cell is depicted in Figure 1. In an ideal SRAM cell, VTC of both halves

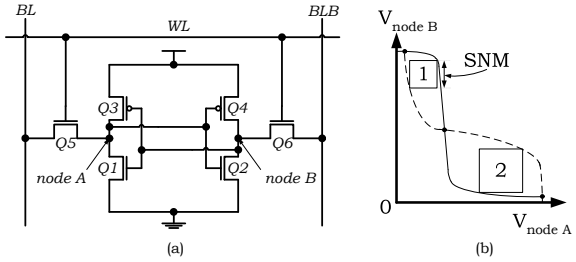


Figure 1 A Six-transistor SRAM cell (a) and its SNM definition (b)

of such a cell would be perfectly symmetrical and the squares 1 and 2 between the VTC curves (Figure 1(b)) would be equal. However, in reality, process spreads and non-catastrophic resistive defects can change the shape of VTC curves. We define the SNM as the side of the smaller of the two squares that can be fit in the eyes of the VTC curves, as shown in Figure 1(b). In our SRAM SNM sensitivity analysis, all measurements were taken in a *read-accessed* cell. That gives the worst case SNM [7] as $Q5$ is effectively shunting $Q3$, and $Q6$ is shunting $Q4$, which degrades the stored low-level state and reduces the SNM.

We investigated the SNM dependencies on the process spread (V_{TH}, L_{eff}, and W_{eff}), presence of non-catastrophic defects (resistive bridges and breaks), and variation of operating voltages (V_{DD}), (V_{BL}) and (V_{WL}) for a 6T SRAM cell in 0.13 μm CMOS technology with V_{DD}=1.2 V using special SRAM transistor models allowing more relaxed design rules. The presented data are normalized with respect to the typical case (typical process corner, room temperature, typical voltages). In the subsequent sections we used the following transistor notation (Figure 1(a)): $Q1$ and $Q2$ – driver transistors, $Q3$ and $Q4$ – load transistors, and $Q5$ and $Q6$ – access transistors. The signal notation: BL – bit line, BLB – bit line bar, WL – word line, node A and node B – the internal nodes of an SRAM cell.

2.1 SRAM SNM and process variations

Process variations in modern CMOS nano-technologies pose an ever-growing threat to SRAM cell robustness. Threshold voltage (V_{TH}) spreads over ten percents of the typical are not unusual anymore [3, 12]. Such variations can dramatically reduce the SNM and thus – the stability of SRAM cell, which is also demonstrated by our simulation results.

SNM dependence on V_{TH} variations for slow, typical and fast process corners is shown in Figure 2.

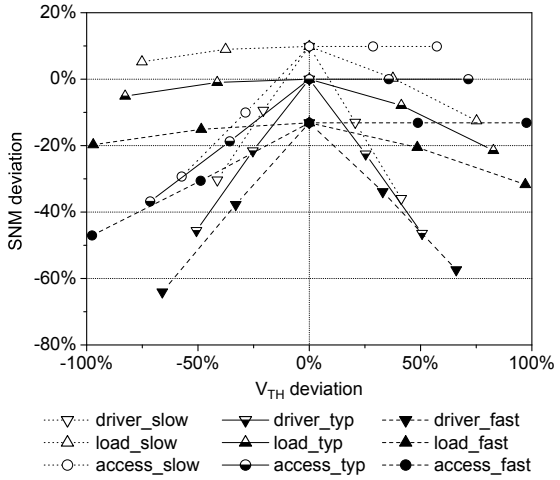


Figure 2 SRAM cell SNM vs. threshold voltage deviation of one of the transistors

We swept V_{TH} of only one transistor at a time while keeping the V_{TH} of the other transistors typical. By sweeping V_{TH} of one of the transistors, we introduced a mismatch between two halves of the SRAM cell. This essentially changes the shape of the transfer characteristics (see Figure 1(b)) and thus can adversely affect the SNM. The "0" point on the x-axis corresponds to the typical value of V_{TH} of a corresponding transistor in the corresponding process corner.

V_{TH} variation of the driver transistor has the largest impact on the VTC shape and thus SNM due to its larger W/L ratio compared to other transistors in SRAM cell. Decrease in V_{TH} of the access transistor also has a strong negative impact on the SNM. Since the measurements were taken in a read-accessed SRAM cell, the access transistors are effectively connected in parallel with the load transistors. Thus, reducing the V_{TH} of the access transistor compromises the low level stored in the cell, which in turn reduces the SNM. On the other hand, the V_{TH} variation of the PMOS load transistor has the least impact on the SNM due to its weaker drive and typically smaller W/L ratio.

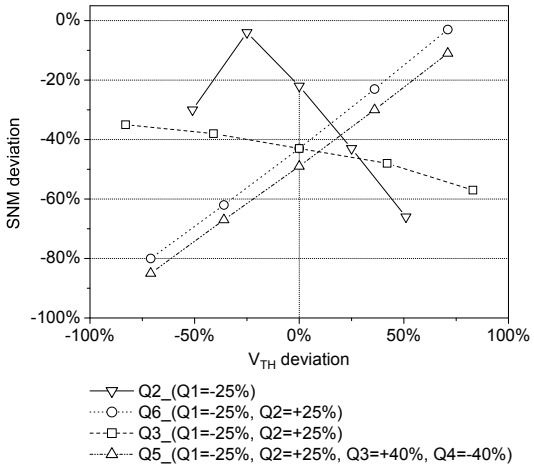


Figure 3 SRAM cell SNM vs. threshold voltage deviation of more than one transistor

Note that SNM deviation is zero if V_{TH} deviation of all transistors is zero (symmetrical cell), except only for the case of increasing V_{TH} of the access transistor, which does not affect the SNM as its shunting action on the load transistor decreases.

If more than one V_{TH} is affected at a time, the SNM degradation will be stronger. Figure 3 presents several cases of the SNM vs. V_{TH} dependencies when V_{TH} of more than one transistor in the SRAM cell is not at its typical value (typical process corner). For instance, $Q2\_(Q1{=}{-}25\%)$ in Figure 3 represents the dependence of the SNM on V_{TH} of $Q3$ provided that V_{TH} of $Q1$ is below its typical value by 25%. This dependence has its maximum at the point where V_{TH_Q1}=V_{TH_Q2}=-25% (i.e., where the cell is symmetrical). SNM vs. V_{TH} of $Q5\_(Q1{=}{-}25\%$, $Q2{=}{+}25\%$, $Q3{=}{+}40\%$, and $Q4{=}{-}40\%)$ represents one of the worst cases of the SNM degradation due to the asymmetry of V_{TH} of the cell's transistors.

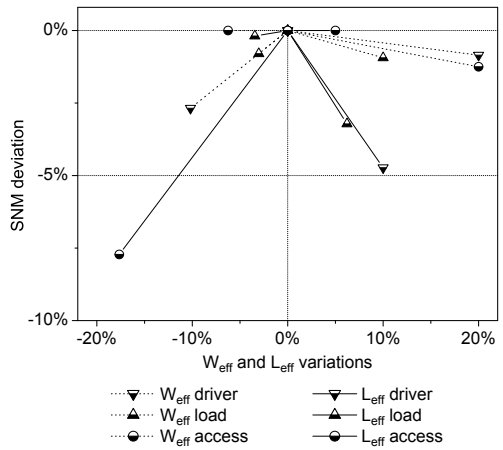


Figure 4 SRAM cell SNM vs. L_{eff} and W_{eff}

SRAM cell SNM dependence on L_{eff} or W_{eff} variations of a single transistor under typical conditions is shown in Figure 4. The SNM decrease is insignificant when the transistor's effective length and width variation remains within 20% of the typical values. Regardless of the direction of the transistor geometry variation, the SNM is maximal at the typical (symmetrical) transistor sizes. This is due to the fact that the variation of the transistor geometry in only one of the halves of the SRAM cell causes mismatch, which leads to the reduction of the SNM. Analysis of Figure 4 shows that for a weaker driver transistor (smaller W/L ratio) SNM decreases, whereas a weaker access transistor improves the SNM. Deviations in W/L of the load transistor just slightly degrade the SNM.

From Figure 2, Figure 3 and Figure 4 it is apparent that the SNM of SRAM cell is maximal if the effective driving strength of both halves $(Q1-Q3-Q5$ and $Q2-Q4-Q6)$ of the cell is symmetrical with respect to their threshold voltages and W/L ratios.

2.2 SRAM SNM and non-catastrophic defects

Most catastrophic defects in SRAM cells cause drastic reduction of the SNM causing functional faults and thus and are easily detected. However, SRAM cells with non-catastrophic defects can escape standard tests due to a non-zero SNM, while degrading the cell stability and posing potential long-term reliability issues. In order to investigate SRAM SNM degradation based on non-catastrophic defects, we utilized Carafe inductive fault analysis (IFA) tool to introduce *resistive* defects in the layout [13]. Carafe works by widening and shrinking the layout geometries and finds possible intersections of conductors in different process planes to determine how a spot defect of a certain size can affect the layout. Based on the layout sensitivity analysis, Carafe generates a list of faults.

We modelled the obtained faults as parallel and series resistors for bridges and breaks respectively and simulated the faulty netlists with a SPICE-like circuit simulator. Defects were injected into the layout consisting of an array of 2×2 SRAM cells to generate the list of the most likely faults. Since an SRAM cell has a symmetrical structure, certain defects can appear in either half of the cell. The probability for such defects had been doubled. We simulated only one defect type at a time, while all other conditions were kept typical. The defect resistance values were swept from $1\ k\Omega$ to $50\ G\Omega$ for both the breaks and the bridges.

For the most likely breaks (resistive open) and bridges (resistive short), the SNM deviation as a function of their resistance is for typical conditions is presented in Figure 5 and Figure 6 respectively.

As is evident from Figure 5 and Figure 6, increasing the resistance of bridges and breaks has an opposite effect on SRAM cell's SNM. When resistance is increasing, most resistive opens (breaks) linearly degrade the SNM and

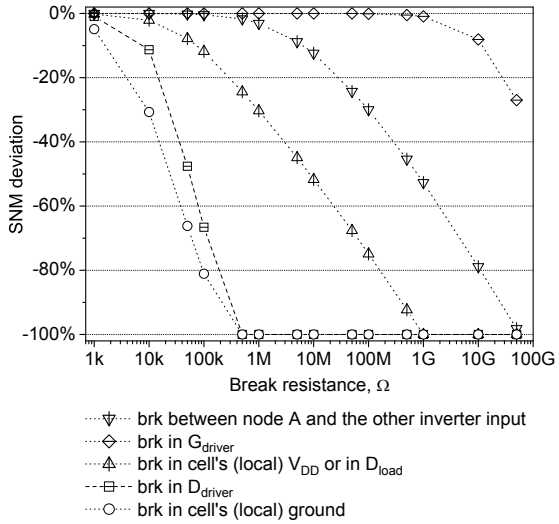


Figure 5 SRAM cell SNM vs. break (resistive open) resistance

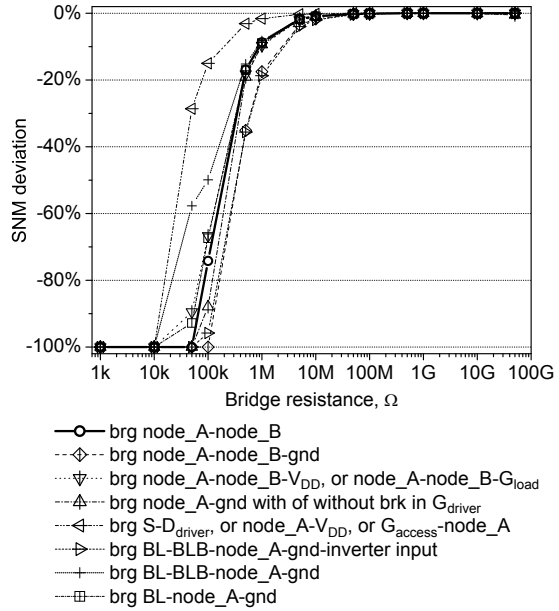


Figure 6 SRAM cell SNM vs. bridge (resistive short) resistance

above certain resistance values, they cause the SNM to become a zero. Resistive open defects are likely to appear in place of poor or absent contacts, vias or silicide [9, 10]. Note that different breaks have different impact on the SNM. Break in the local ground contact of SRAM cell has the strongest negative impact on the SNM. Break in drain of a driver transistor (D_{driver}) also causes a severe reduction of the SNM. Break in cell's (local) V_{DD} or in the drain of a single load transistor (D_{load}), which can cause Data Retention Faults (DTFs), has a medium impact on the SNM. Whereas resistive breaks in transistor gates do not cause a noticeable SNM degradation unless the break resistance is exceeding $1\ G\Omega$.

Figure 6 shows that unlike the case of resistive breaks, the reduction of resistance of most bridges causes a very similar degree of the SNM degradation. Bridges with resistance below $10 - 100\ k\Omega$ reduce the SNM to be near zero and cause catastrophic functional failures, which are easily detected by the regular march tests. The SNM increases almost linearly for most of the bridges having resistances between $100\ k\Omega$ and $1\ M\Omega$. Bridge defects with resistance of more than $10\ M\Omega$ show no impact on the SNM. Due to the cross-coupled layout of and SRAM cell, the most likely resistive bridge is the bridge between the internal nodes of the cell. In Figure 6, the SNM dependence on this bridge (brg node_A-node_B) resistance is shown in a bold solid line.

2.3 SRAM SNM and operating voltages variation

Variation of the operating voltages such as supply (V_{DD}), bit line (V_{BL}) or word line (V_{WL}) voltages strongly impacts SRAM cell's SNM. The worst case SNM is typically observed for the fast process corner and high temperature; the best case SNM – for the slow process corner and low temperature. The results for all other temperature/process corner combinations fall in between the best and the worst cases. We swept V_{DD}, V_{BL} and V_{WL} one at a time from 0 to $1.5V$ and measured the corresponding SNM.

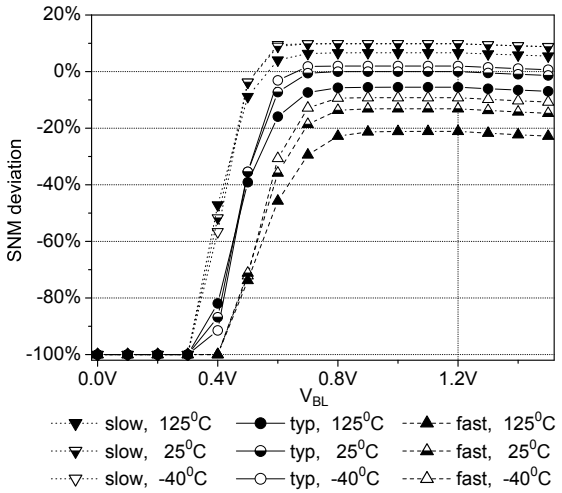


Figure 7 SRAM cell SNM vs. bit line voltage

Figure 7 depicts the SNM dependence on V_{BL} while the V_{DD}, V_{WL}, and V_{BLB} are at the typical $1.2\ V$. The situation when one of the bit lines is driven from V_{DD} to the ground corresponds to a "write" operation. Overwriting the data stored in an SRAM cell becomes possible when the SNM is made zero. It can be seen from Figure 7 that the SNM becomes zero at $V_{BL} < 0.3\ V$ for the typical process corner. Note that the SNM does not decrease immediately once V_{BL} starts decreasing. The reduction of V_{BL} begins to reduce the SNM once $|V_{BL} - V_{WL}| > V_{TH_{access}}$ and the access transistor enters the linear mode. Since in the slow process corner transistors have higher V_{TH}, with the reduction of V_{BL}

the cell SNM stays constant for a longer period than its counterparts from the typical and the fast process corners.

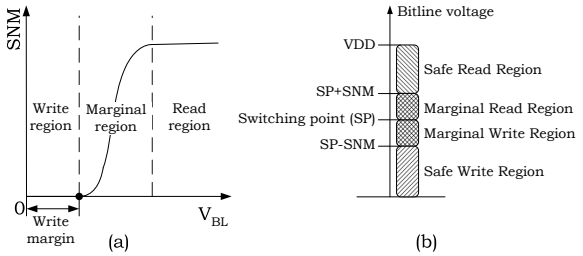


Figure 8 Read and write safe and marginal regions of an SRAM cell

Figure 8 (a) shows the read and write regions of an SRAM cell as a function of the bit line voltage. A write operation is possible in the region where the bit line voltage is at or below the point where the SNM is zero. This region is called the *write margin*.

The write margin is an important design parameter as it also defines the cell stability to various disturbances. A balance between the cell stability (SNM), cell area and access speed (read current) must be found, which may not allow to maximize the cell stability.

Four regions can be identified for the bit line voltage between the ground and the precharge value: Safe Read Region, Marginal Read Region, Marginal Write Region and Safe Write Region (Figure 8 (b)) [15]. The Safe Read Region is defined from the switching point (SP) plus SNM to the V_{DD}, whereas the Safe Write Region is defined from the SP minus SNM to the ground. The regions between the SP and the Safe Read Region and between the SP and the Safe Write Region are described as Marginal Read or Write regions respectively.

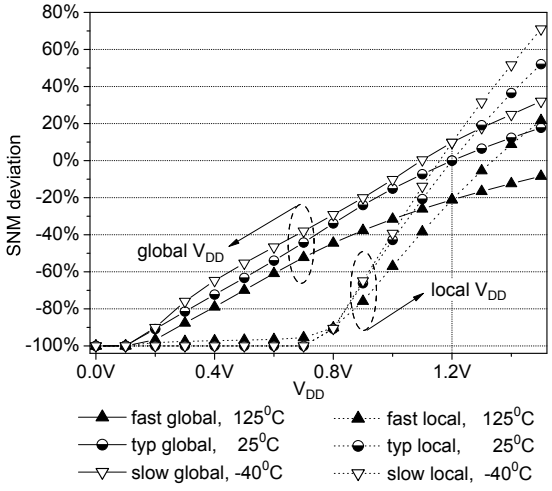


Figure 9 SRAM cell SNM vs. V_{DD}

Figure 9 shows SNM as a function of the global and local V_{DD}. By global V_{DD} variation, we mean the situation when V_{WL}, V_{BL}, V_{BLB}, and SRAM cell supply voltages vary all at the same time, which is similar to battery discharge in a mobile device. By local V_{DD}, we imply only the variation of SRAM cell supply voltage, while V_{WL}, V_{BL} and V_{BLB} are all at the typical values. Local V_{DD} variation mimics a faulty via in the supply voltage grid of SRAM cell. SNM shows strong dependence on both the local and the global V_{DD} variations. However, the SNM dependence on the local variation is stronger since in this case the word line and the global bit lines are at full V_{DD}, which causes the access transistor to shunt the pull-up transistors stronger and degrade the low state of the cell. If we continue to rise the local V_{DD}, we can observe a significant increase of the SNM because the drive of the access transistors of the read-accessed cell is becoming weaker while the power supply of the cross-coupled inverters rises.

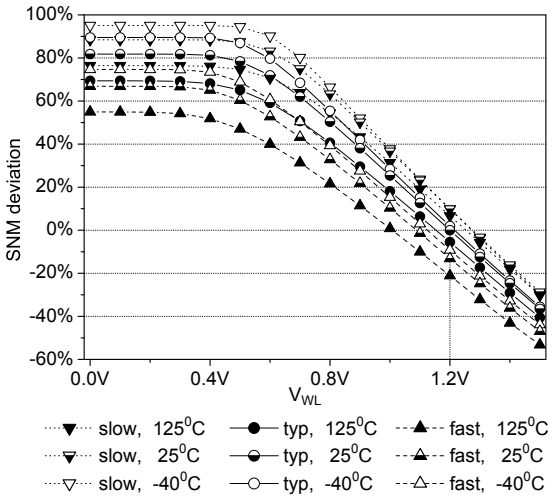


Figure 10 SRAM cell SNM vs. word line voltage

Figure 10 shows the dependence of the SNM on the word line voltage. All other operating voltages are at typical values. The SNM does not decrease if the V_{WL} is below the V_{TH} of the access transistor. Once V_{WL}>V_{TH} of the access transistor, the SNM starts to deteriorate as the access transistor starts to shunt the load transistor and pull higher the node storing a logic zero. Note that if the word line exceeds V_{DD}, the SNM continues to deteriorate as the shunting action of the access transistor strengthens.

If all voltages are kept at their typical values and the temperature is varied from $-40°$C to $125°$C, the SNM demonstrates rather weak temperature dependence from 5% for the slow process corner to 12% for the fast process corner. as it is apparent from Figure 11. The SNM tends to decrease at the elevated temperatures. However, compared to other parameters, contributing to the SNM degradation, the temperature factor alone often negligible.

In previous paragraphs, we described the impact of a sin-

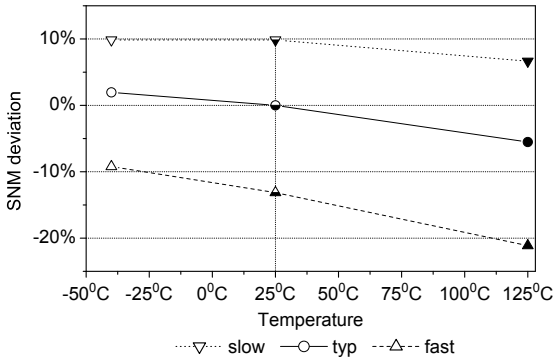


Figure 11 SRAM cell SNM vs. temperature

gle process parameter variation on the SNM. However, in real life, several process parameters may change simultaneously. In case more than one process parameter (especially V_{TH}) departs from its typical value, the impact on the SNM is dramatic, often reducing the SNM to a very low value. Such SRAM cells are prone to stability faults, which may escape the standard tests. Stability faults can manifest potential long-term reliability problems.

3 Proposed Weak Cell fault model

A fault model is a systematic and precise representation of physical faults in a form suitable for simulation and test generation [14]. A fault must mimic behavior of a physical defect with a certain degree of accuracy. Since the SNM is a measure of an SRAM cell stability, its degraded value results in a cell stability fault that is parametric in nature. This fault can manifest itself under certain conditions by compromising the stored data integrity. We believe that development of a parametric stability fault model for SRAMs is crucial for investigation and comparison of the effectiveness of various test algorithms and DFT techniques as well as for stability characterization of SRAM designs. Therefore, we developed such a model. The proposed fault model mimics the SNM degradation due to transistor mismatches, non-catastrophic defects and variation of the operating conditions.

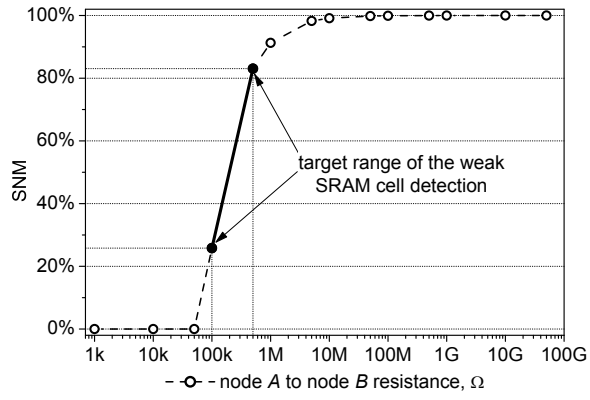


Figure 12 A weak cell detection threshold

Let us consider the dependence of the SNM on the resistance between node A and node B as illustrated in Figure 12, and also in a thicker solid line in Figure 6. For very large resistance values of $(> 10\ M\Omega)$, the cell SNM is not affected. For the resistance range between $50\ k\Omega$ and $1\ M\Omega$, the SNM is reducing linearly. The SNM becomes zero and causes catastrophic failure for the resistor values below $50\ k\Omega$. Depending on the SRAM cell, one can choose a particular resistance value in order to realize a weak cell with a pre-determined SNM. For instance, to obtain a cell with a half of the typical SNM, a resistor of $200\ k\Omega$ has to be used. A bold line in Figure 12 represents a possible target range for the weak SRAM cell detection.

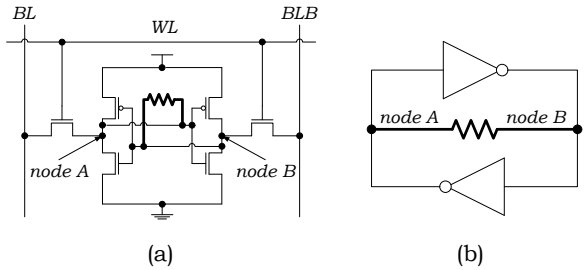


Figure 13 The proposed fault model (a) and its equivalent circuit (b)

The resistor between node A and node B represents the proposed *weak cell fault model*, which is illustrated in Figure 13 (a). SRAM cell has the worst-case SNM in the read-access mode when both the bit lines are precharged and the word line is activated [7]. Each half of a read-accessed SRAM cell can be represented as an equivalent inverter, as shown in Figure 13 (b). As we can see from Figure 13, a node-to-node resistive defect represents a negative feedback for the equivalent inverters comprising SRAM cell. The corresponding reduction of the inverter gains and hence, the amount of the negative feedback in the cross-coupled inverters, is symmetrical and can be used to control the SNM. In a simulation environment, a cell with a resistor of a specified value between node A and node B can imitate a weak cell with a specified SNM value. The degree of the "weakness" is controlled by the value of the resistor. Provided equal other conditions, the "weakened" cell has equal SNMs for both the high-to-low and the low-to-high internal node voltage transitions. Thus, it represents a simple, symmetric and realistic weak cell fault model for simulation of parametric stability faults in SRAMs.

Intentionally inserting weak cells with the desired target SNMs into an SRAM array allows us to verify and fine-tune test techniques for parametric stability fault (weak cell) detection in the simulation environment. Having a simulation setup with a set of weakened cells with varying degree of weakness (SNM) allowed us to evaluate various cell stability DFT techniques and algorithms.

Moreover, such a setup can also be instrumental on the stability characterization and debugging stages of SRAM development.

4 Programmable detection threshold concept

To illustrate the concept of programmable detection, consider the transfer characteristics of a good SRAM cell (solid lines) and a weak SRAM cell (dashed lines) presented in Figure 14. Axes in Figure 14 represent node A and B voltages, which in turn, are proportional to the bit line voltages. VM_{good} and VM_{weak} represent the metastability points of a good and a weak cell respectively. If node A or node B of an SRAM cell is driven to the level of VM, then a small voltage increment will flip the cell towards the direction of this increment. Points X_1, Y_1 (X_2, Y_2) on the transfer characteristic represent the stable states and Z_1 (Z_2) - the metastable states of the good (weak) cell, respectively. As it is apparent from the figure, the weak cell has a significantly smaller SNM (SNM_{weak}<SNM_{good}).

If a test voltage V_{TEST} is applied to node A (x-axis), the weak cell can be flipped while the good cell will retain its data. By varying the V_{TEST} value, one can test for a given degree of cell weakness. Hence, if we can manipulate the value of V_{TEST}, we can realize a programmable detection threshold and detect weak cells with a targeted degree of weakness. The significance of our ability to program how weak should be a cell to be detected, in other words, the significance of the detection target programmability, stems from various considerations. For example, (i) not all cells have the same transfer characteristics, (ii) the meta-stable points also may change due to technology spread and in the presence of defects, and (iii) customer requirements may vary depending on the target application. A DFT with a programmable detection threshold can substitute time consuming and thus costly Data Retention Test (DRT).

Let us assume that node A of an SRAM cell has state "1" and that the bit lines are pre-charged to a known value (e.g. V_{DD}). Now assume that by certain manipulation, the V_{node_A} is reduced from a stable state X_1 (or X_2 for a weak cell) to a certain test voltage V_{TEST}. Voltage level V_{TEST} intersects the good cell's transfer characteristics at points "1" and "2" and it intersects the weak cell's transfer characteristics at points "3" and "4", as shown in Figure 14. The value of V_{TEST} will set the programmable weak cell detection threshold. As it is apparent from Figure 14, the weak cell will flip its state if $(V_{DD} - V_{TEST}) < (V_{DD} - VM_{weak})$. The good cell will retain its state. Node A of the good cell will retain its state "1" upon removal of the test stimulus V_{TEST}, while node A of the weak cell will flip to state "0". The arrows in Figure 14 show the direction of the transfer characteristic dynamics in this case. This is exactly the principle that is utilized in the proposed method of detection of the weak cells. All the cells, which flip at the node voltage above V_{TEST} are deemed "weak". The rest of the cells is assumed to have acceptable stability.

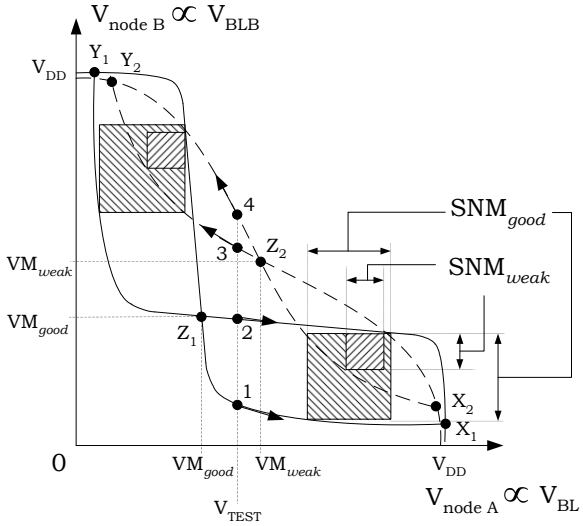
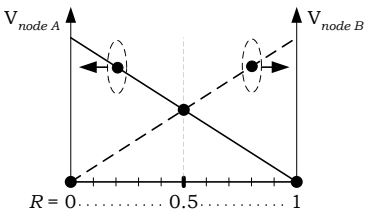


Figure 14 VTC of a typical and a weakened SRAM cell

5 Proposed DFT

The concept of programmable threshold is implemented using a set of n SRAM cells in a given column. Existing cells in the column or external cells can be utilized for this purpose. Let R be the ratio of cells having state "0" to the total number of cells in a set n (Figure 15).



$$R = \frac{number\ of\ cells\ with\ state\ \text{"0"}\ in\ a\ set\ of\ n\ cells}{set\ of\ n\ cells}$$

Figure 15 Definition of the programmable ratio R

We assume that the rest of the cells in a set n have state "1". Initially, BL and BLB are precharged to V_{DD}. By manipulating the value of R, and simultaneously accessing n cells, we can manipulate the bit line voltage. As can be seen from Figure 15, Figure 18, Figure 19, by varying the value of R, we can control which bit line will have a higher potential.

Now, if we write a ratio R, simultaneously enable n word lines, and short the bit lines together, we can reduce V_{node_A} or V_{node_B} to a given V_{TEST} value. Large V_{TEST} will not flip any of the cells as it will be similar to a read operation. Smaller V_{TEST} (around VM_{weak})

will flip the weak cells. And finally, when V_{TEST} approaches VM_{good}, it can overwrite even the good cells. Therefore, by varying the ratio R, we can program a detection threshold for detection of SRAM cells with varying degrees of weakness.

The flow diagram shown in Figure 16 depicts the sequence of steps necessary for digitally programmable weak cell detection. It is assumed that we can program the trip point of a weak cell by selecting an appropriate 0/1 ratio (R) of cells. An inverse of the current 0/1 ratio is necessary to detect the weak cells that may flip in the opposite direction.

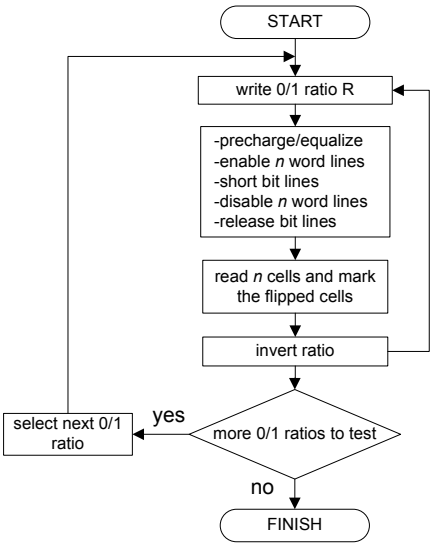


Figure 16 Flow diagram of the programmable weak cell detection

Figure 17 shows the hardware required for one of the implementations of the proposed technique. Ellipses surround additional and/or modified circuitry. Figure 17 represents one of the SRAM cells in a column, two cross-coupled PMOS transistors $(Q1, Q2)$ to pull up the bit lines, three other PMOS transistors $(Q4 - Q6)$ to precharge the bit lines to V_{DD}, one NMOS $(Q3)$ transistor to short the bit lines together. It also includes special logic to issue the Weak Detect (WD) signal, and a modified word line decoder for simultaneous enabling of n word lines.

The weak-cell detection phase starts by programming the trip point that is necessary to detect cells with the SNM below the target value. This is done by writing a predetermined number of cells with either a "1" or a "0" state. After the normal bit line precharging finishes, n word lines are simultaneously enabled connecting in parallel n cells of the same column. Under this configuration, access transistors of each side of an SRAM column share a common gate and a common bit line nodes. The other terminal of each of the access transistors is connected either to the ground or to V_{DD} through the corresponding driver

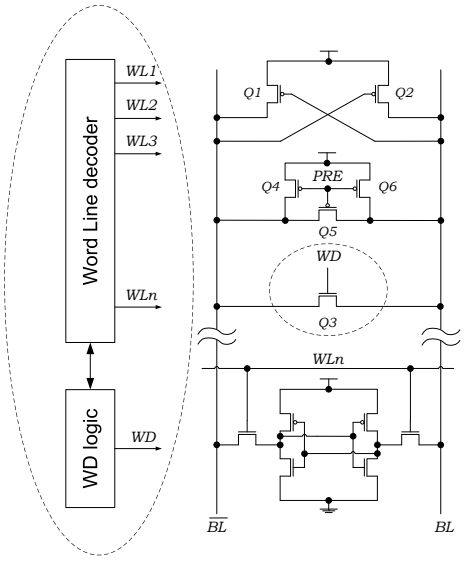


Figure 17 Programmable detection threshold hardware implementation-1

or load transistors of an SRAM cell. The access transistors work as resistors dividing the power supply voltage on each bit line between V_{DD} and the ground depending upon the equivalent dc path resistance. For instance, bit line potentials will be around $V_{DD}/2$ when 50% of cells are in state "0" and 50% of cells are in state "1" because the path resistance to the ground and V_{DD} is the same, i.e. $R = 0.5$ (Figure 15).

When the word lines are enabled, the capacitance of each bit line discharges according to the time constant created by the corresponding equivalent path. If the bit lines discharge below the metastable point VM_{good}, even the good cells will flip pulling one of the bit lines even further to the ground and restoring the other one to V_{DD}. To prevent the cells from reaching metastable point VM_{good}, the bit lines are shorted together through an NMOS pass transistor by applying a WD (weak detection) pulse. This causes the voltages at the bit lines to remain at around $V_{DD}/2$ while the cell dynamics finds a new equilibrium. In other words, the bit lines are not pulled to complementary logical values. However, a bit line voltage around $V_{DD}/2$ is already sufficient to flip the weaker cells (see Figure 14) with insufficient SNM. For a ratio $R \neq 0.5$, the corresponding path resistances to V_{DD} and the ground will be different and thus the bit line voltage is pulled earlier above or below $V_{DD}/2$.

To prove the effectiveness of this method we designed a setup with eight six-transistor SRAM cells in CMOS $0.13\ \mu m$ technology with $V_{DD} = 1.2\ V$. The degree of weakness of one of the cells was manipulated by varying the resistance value of the resistor between node A and node B of this cell as per the proposed weak cell fault model. To verify the data retention fault detection capabilities, we also simulated the proposed DFT implementation with inserted resistive breaks in the load transistors.

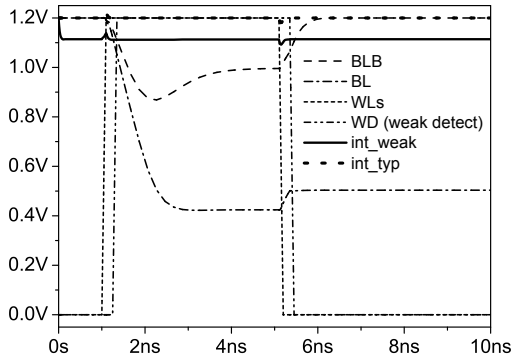


Figure 18 Voltage dynamics of node B and other signals for a weak cell (int_weak) and a reference cell (int_typ) for a 0/1 ratio of 3/5

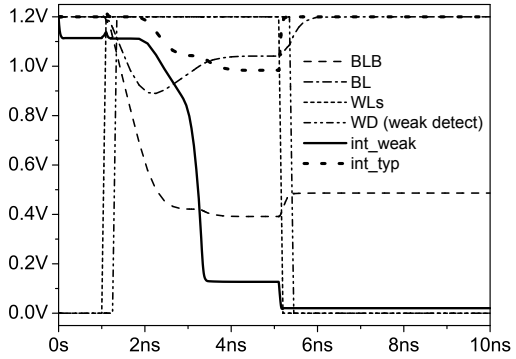


Figure 19 Voltage dynamic of node B and other signals for weak cell (int_weak) and a reference cell (int_typ) for a 0/1 ratio of 5/3

Figure 18 and Figure 19 illustrate the voltage dynamic of node B and other signals for the weak cell (int_weak) and a reference typical cell (int_typ) for a 0/1 ratios of 3/5 and 5/3 respectively.

The weak cell was forced into a weak state by connecting nodes A and B with a resistor of 200 $k\Omega$. Evaluation of this cell with the inserted resistor of 200 $k\Omega$ gives an SNM of around 50% of the typical SNM.

A logical "1" state was stored in node B of the weak cell as well as in node B of a reference typical cell. To have a more realistic situation the bit line precharge was simulated as well. After precharging both bit lines to V_{DD} and equalizing them, we enabled n word lines and shortly after that enabled the weak detect (WD) pulse to enter the weak detection mode. The cells state can be inspected at around 6 ns point.

When the ratio of 0/1 states is 4/4, the bit line-bar voltage drops to around $0.6\ V$ $(V_{DD}/2)$ but the weak cell's state does not flip. If the ratio of 0/1 states is 3/5, V_{BLB} rises up to about $1\ V$ (see Figure 18). This voltage strengthens the weak cell and helps it to remain in its logical "1" state (bold solid line int_weak in Figure 18). With a 5/3 ratio of 0/1 states (Figure 19) V_{BLB} drops down to about $400\ mV$ forcing the weak cell to flip states (bold solid line int_weak in Figure 19).

Figure 20 demonstrates the detection capability of the proposed method. The resistance value of the node A to node B resistor for imitating a weak cell was swept from $100\ k\Omega$ to $500\ k\Omega$ and we used 0/1 ratio of 5/3.

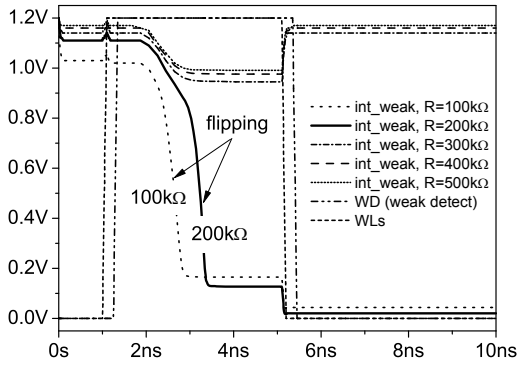


Figure 20 Detection capability of the proposed DFT (implementation-1) for a 0/1 ratio of 5/3

Signal int_weak in Figure 20 represents node B of the weak cell. We can see that after applying the test sequence, the weak cell flips for resistance between node A and node B of $100\ k\Omega$ and $200\ k\Omega$. It this case, the SNM of the weak cell is too small to resist the overwriting disturbance and the cell is overwritten in the Marginal Write Region (Figure 8 (b)). Note that the cell does not flip for resistor values of $300\ k\Omega$, $400\ k\Omega$, and $500\ k\Omega$ because in this case the SNM is large enough to resist the flipping. Although it is still possible to force such a cell to flip by choosing a different 0/1 ratio of n cells, i.e., by digitally programming the detection threshold.

Similar waveforms were obtained for detection of resistive opens in one or both load transistors, which confirms, that the proposed DFT can be effectively used to detect both the stability and data retention faults in SRAM cells.

Another possible hardware implementation of the proposed technique is shown in Figure 21. It consists of cross-coupled pull-up PMOS transistors $(Q1, Q2)$, pull up and pull down transistors $(Q3, Q4)$ tied to the bit lines, a CMOS switch $(Q5, Q6)$ to short the bit lines together, special logic to enable n word lines simultaneously and to test-precharge the bit lines.

The sequence of steps to carry out this implementation is similar to the one for the first implementation. However, in contrast with the previous implementation, the BL is precharged to the ground, and the BLB – to V_{DD} rather than both bit lines are precharged to V_{DD}. Applying the bit line capacitances precharged in such a fashion works in a similar way to a write operation. After precharging the bit lines by enabling $PRE/\overline{PRE}$, we enable n word lines and apply $WD/\overline{WD}$ pulse, the bit line

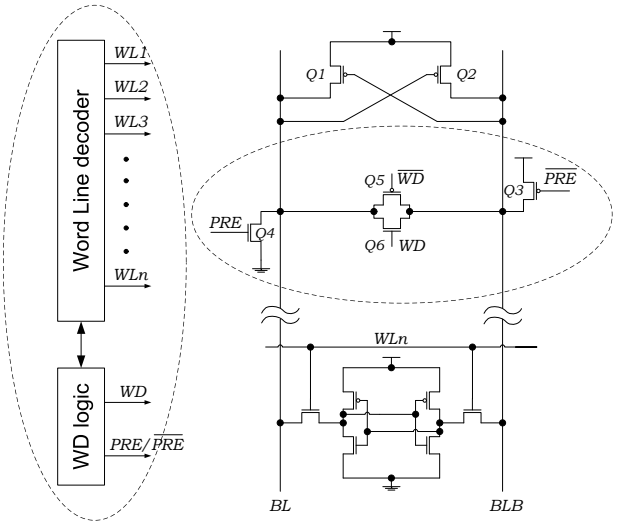


Figure 21 Programmable detection threshold hardware implementation-2

potentials redistribute, causing weak cells to flip states. $PRE/\overline{PRE}$ and WL should be mutually exclusive but in practice a small overlap can exist between them. If this overlap is sufficiently long, even the good cells will flip, since a long overlap will effectively turn precharge transistors into write drivers.

6 Conclusions

Stability of embedded SRAM cells is a crucial design, manufacturing and test issue. As a result of extensive SNM sensitivity analysis, we proposed a *parametric stability fault model* for *weak* SRAM cells. The proposed weak cell fault model mimics a symmetrical SNM degradation that can be caused by process spread, and/or non-catastrophic structural defects, and/or variation of the operating voltages.

Proposed fault model allows modelling the impact of the above detrimental conditions on SRAM cells and enables stability characterization of SRAM designs and DFT techniques aimed at the detection of memory cells with compromised stability (i.e., with a low SNM).

A DFT technique capable of detecting stability faults is proposed. A distinctive feature of the proposed DFT technique is digital programmability of the weak cell detection threshold, which facilitates testing cells with various degree of stability degradation as well as with data retention faults. Application of the proposed DFT also provides information whether a found non-catastrophic defect is symmetric or not. Moreover, thanks to the programmability of the detection threshold, it facilitates estimation of stability level (SNM) of weak SRAM cells.

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