Analysis and Design of LVTSCR-based EOS/ESD Protection Circuits for Burn-in Environment

O. Semenov, H. Sarbishaei and M. Sachdev
Dept. of Electrical and Computer Engineering, University of Waterloo, Waterloo, Canada N2L 3G1
osemenov@vlsi.uwaterloo.ca

ABSTRACT

As technology feature size is reduced, ESD becomes one of the dominant failure modes due to the lower gate oxide breakdown voltage. Also, the holding voltage of LVTSCR devices is reduced with operating temperature increase. As a result, during stress testing (burn-in), the risk of latch-up in LVTSCR is extremely high. In this paper, a new latch-up free LVTSCR-based protection circuit is proposed. It can be reliably used in sub-0.18 um CMOS technologies and burn-in environment. The proposed ESD circuit has higher holding voltage by 1.5X than the conventional LVTSCR structure at burn-in temperature. Under 3kV HBM ESD stress, the developed LVTSCR-based protection circuit has the voltage peak less than the conventional LVTSCR structure and GG-MOSFET by 2X and 1.25X, respectively.

Keywords *- Electrostatic discharge (ESD),* electrical overstress (EOS), *LVTSCR, burn-in, latch-up.*

1. Introduction

Electrostatic Overstress and Discharge is considered as a major reliability threat in the semiconductor industry for decades. It was reported that ESD and EOS are responsible for up to 70% of failures in IC technology [1]. Therefore, each I/O must be designed with a protection circuitry that creates a discharge path for ESD current. As a CMOS technology scales down, the design of ESD protection circuits becomes more challenging. This is due to thinner gate oxide and shallower junction depth in advanced technologies that makes them more vulnerable to ESD damages. In addition, special accelerated test methods such as burn-in are often employed as reliability screens to weed out infant mortalities. Weak gate oxides are one of the major components of such failures. These failures are accelerated due to elevated temperature (~125ºC), elevated voltage (V_{DD} + 30%) and long stress time (30-168 hours). Under stress operating conditions, ESD robustness of protection devises becomes worse.

Silicon Controlled Rectifiers (SCRs) in low voltage triggered configurations (LVTSCR) are the popular protection elements that are used for on-chip ESD protection. The excellent high current behavior of LVTSCRs provide an area gain factor of 4X to 5X over the silicide-blocked grounded-gate N-MOSFET (GG-NMOSFET). Generally, ESD protection device should have the first breakdown voltage less than the breakdown voltage of the gate oxide while its holding voltage should be greater than V_{DD} in order to avoid the latch-up possibilities. However, the relatively high triggering voltage (~10-12 V) and low holding voltage (~1.5-2.5 V) restrict the application of conventional LVTSCR ESD devices for sub-0.18 micron CMOS technologies [2]. The risk of latch-up in SCR structures and hence the post burn-in yield losses are significantly increased under stress operating conditions during burn-in [3]. Note, that the burn-in testing is typically performed at T=110-125ºC and V_{DD}=2.1-2.3V for 0.18 um CMOS technology.

In this paper, a new implementation of latch-up free LVTSCR-based ESD protection circuit for burn-in environment is proposed. The developed ESD protection device has the following features:

(1) The holding voltage (V_h) more than 3V at stress temperature (to avoid latch-up in LVTSCR under burn-in operating conditions),

(2) The triggering voltage (V_{tr}) less than 9V (to prevent the gate oxide breakdown due to ESD event in sub-0.18 um transistors)

(3) The ESD robustness is more than 3kV of human body model (HBM) ESD stress.

Our results show that the proposed LVTSCR-based ESD protection circuit has significantly lower V_{tr} and higher V_h than the conventional LVTSCR device. Also, it has less V_{tr} and peak temperature during ESD event than the conventional GG-MOSFET with equivalent device width. Hence, the developed ESD circuit is more robust at ESD event and burn-in conditions in comparison with the commonly used ESD protection devices.

The rest of the paper is organized as follows: In Section 2, we review the operating features of ESD protection circuits in burn-in environment. The conventional LVTSCR structure and the proposed ESD protection circuits, used in our research, are described in Section 3. The circuit and device simulation results at burn-in operating conditions and 3kV HBM ESD stress are presented in Section 4. In Section 5, the analytical modeling of temperature dependency of holding voltage in analyzed ESD circuits is presented. Finally, the conclusions are summarized in Section 6.

2. ESD Protection Devices under Burn-in Stress

During burn-in testing devices in the chip can be damaged, when incorrect test vectors, systems and procedures are used. Usually, burn-in systems include voltage protection circuits, bypass capacitors, burn-in

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ovens, driver boards and power suppliers. Over voltage or under voltage spikes on power suppliers or device inputs can result in ESD device and I/O buffer failures. In practice, 2.5V spikes were observed on input pins of Field Programmable Gate Arrays (FPGAs) due to the electrical overstress (EOS) in burn-in ovens during the stress testing. Note, that 2.5 V spike for a 1.5V chip is 167% overstress [4]. Hence, the conventional LVTSCR structures can not be used for EOS/ESD protection due to the high risk of latch-up.

Cascaded diodes are other semiconductor devices, which are widely used for ESD protection. The typical forward biased turn-on voltage of diode is 0.6-0.7V at room temperature. Hence, for reliable ESD protection in 0.18 um CMOS technology we need four diodes connected in series. At burn-in temperature (110-125ºC), the diode string leakage current is increased due to the Darlington effect and the diode turn-in voltage is reduced from 0.6V to 0.4V. As a result, a longer diode string will be needed to provide the same EOS/ESD protection at stress temperature and to prevent the false triggering under voltage spikes in burn-in oven. However, the increase in number of diodes and their series resistance may have effect on ESD reliability [5].

For GG-MOSFET protection devices, the burn-in is not such a severe concern because these devices are only experience higher leakage current under stress operating conditions.

3. ESD Protection Circuits under Investigation

To develop the LVTSCR-based protection circuit with latch-up immunity under burn-in operating conditions, low triggering voltage and high ESD robustness, the following ESD structures were studied in this work: (1) conventional LVTSCR, (2) LVTSCR with gate or/and substrate triggering to reduce the V_{tr} [6,7], (3) LVTSCR with high V_h option and (4) GG-MOS transistor, which was used for the comparison. All these circuits were designed using 0.18 um CMOS technology (T_{ox}=41Å).

Electrothermal simulation has been introduced to general-purpose commercially available device simulation in the early 90-ties by TMA [8]. Validity of physical models such as mobility, impact ionization rates, etc. has been confirmed by numerous industrial applications and is generally believed to extend to approximately 600-700K. Since then a number of other TCAD companies also developed similar electrothermal models, including Silvaco, ISE and SEQUOIA. In our research, we used 2-D "SEQUOIA ESD" simulation software, which was developed by Sequoia Design Systems for characterization of an ESD event [9]. This simulator has built-in device synthesis, mesh generation, device simulation, circuit-device mixed-mode simulation and lattice self-heating simulation modules. The physical structures of protection devices used for ESD simulations and quasi-DC I-V characteristics are given in Fig. 1. These device structures were calibrated using industrial data by Sequoia Design Systems. LVTSCR structure was implemented as a punch-through-induced protection element [10]. The quasi-DC simulations were performed under high current conditions including a self-heating effect. The input voltage was ramped linearly up to 2kV during ~100ns of stress time and was applied to a large resistor (1500 Ohm) in series with the ESD device to limit the current. I-V characteristics were extracted from these simulations. Fig. 1 shows that at room temperature, for LVTSCR and GG-MOSFET, V_{tr} is 12.5V and 9.5V respectively, while V_h is 2.2V and 3V respectively.

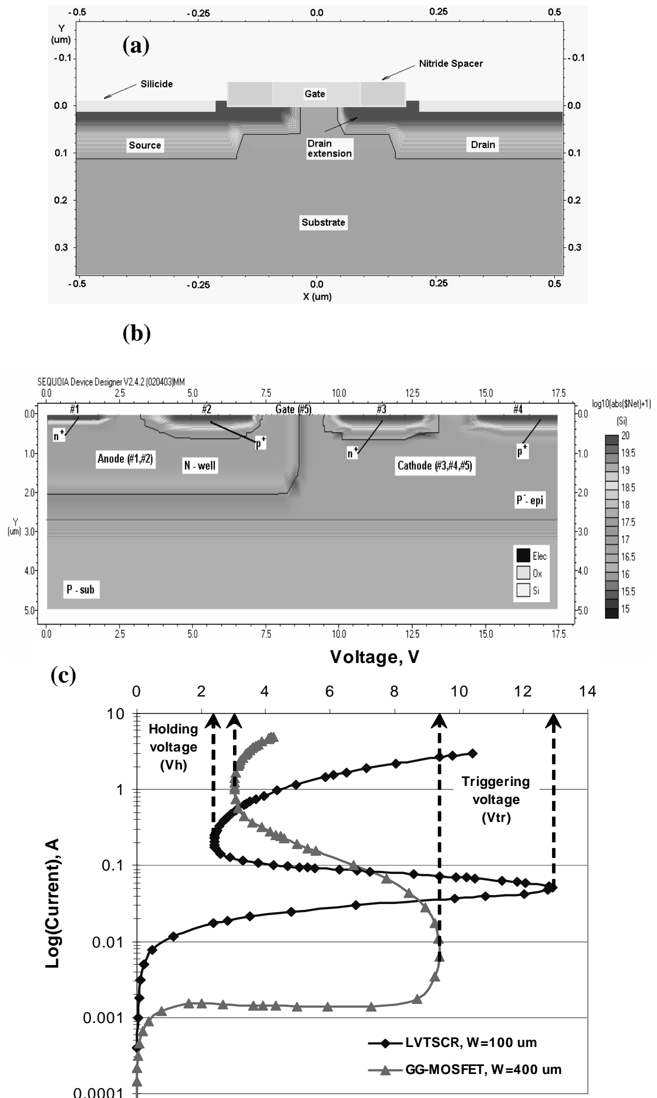

Fig. 1. (a) Cross-section of 0.18 um silicided GG-NMOSFET, (b) Cross-section of surface-induced LVTSCR, (c) Quasi-DC I-V characteristics of ESD devices.

The schematics of analyzed ESD protection circuits are shown in Fig. 2. The size of ESD protection devices was chosen to pass a 3kV HBM ESD stress. In our simulations, the waveform of 3kV HBM ESD stress had 4 ns (10%-90% of peak) rise time and 100 ns (90%-10% of peak) decay time (see Fig 3). The equivalent human body resistance was 1500 Ohms. Note, that the size of GG-MOSFET and the equivalent size of all active devices in LVTSCR-base ESD circuit are the same. Transistors used for substrate triggering and high V_h should be large to provide a significant current pumped into substrate of LVTSCR and ground. On the other hand, the transistor used for gate triggering can be significantly smaller. This transistor only provides the voltage biasing on the gate of LVTSCR during ESD event.

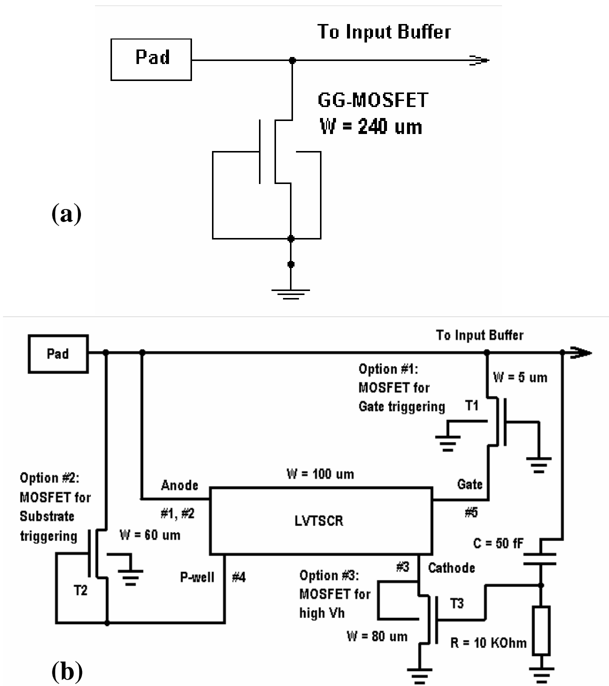

Fig. 2. (a) ESD GG-NMOSFET, (b) LVTSCR-based protection circuit with different options.

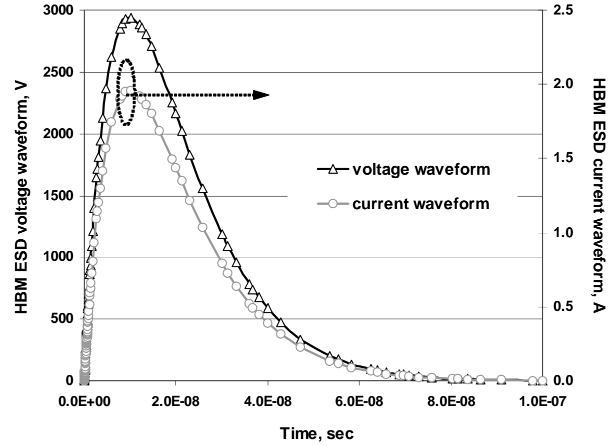

Fig. 3. 3kV HBM ESD stress waveforms used for simulations.

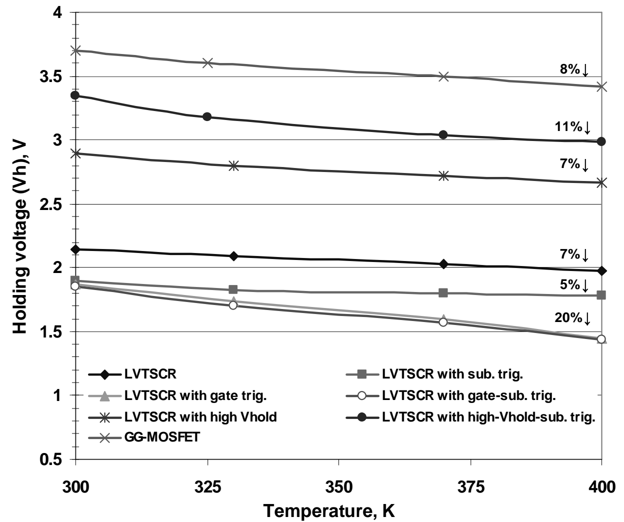

Fig. 4. The comparison of V_h dependency on ambient temperature for different techniques applied for LVTSCR (V_h of GG-MOSFET is shown for the comparison).

4. Simulation Results: V_h under Burn-in Operating Conditions and HBM ESD Stress

From Fig. 1 (c), we can conclude that the basic disadvantages of conventional LVTSCR protection devices are high V_{tr} and low V_h. Note, that the holding voltage of SCR-based devices decreases with elevating temperature [11]. Hence, it is important to develop the LVTSCR-based protection circuit with high V_h to avoid latch-up during burn-in. To estimate the impact of elevated temperature on LVTSCR protection device with different options (see Fig. 2 (b)), the holding voltage was extracted from the quasi-DC I-V characteristics obtained from simulations for different temperatures. The simulation results are depicted in Fig. 4. From these graphs, we can conclude that in the first order approximation, the V_h has a linear dependency on temperature in the range of 300K-400K. The same temperature trend of holding voltage was also observed in experimental results in SCR (1.2 um CMOS process) [12] and LVTSCR (0.5 um CMOS process) structures [11]. The notations in Fig. 4 show the reduction of holding voltage in percentage, when the ambient temperature increases from room temperature to burn-in temperature (400K). We can note that the LVTSCR with gate triggering has the holding voltage degradation by 4X stronger than the LVTSCR with substrate triggering. Hence for burn-in conditions, the substrate triggering technique is more preferable for using in LVTSCR-based

EOS/ESD protection circuits for triggering voltage reduction than the gate triggering technique. To increase the holding voltage at room and stress temperatures, we developed a special technique (see option #3 in Fig. 2 (b)), which include transistor T3 with RC gate coupling network. The combination of substrate triggering technique and high V_h option gives us the increase of holding voltage by 1.56X (from 2.15V to 3.35V) at room temperature and by 1.5X (from 2V to 3V) at burn-in temperature (400K). Note, that 3V of holding voltage at stress temperature is enough to prevent the latch-up of LVTCSR-based protection circuit due to 2.5V spikes on chip input pins in burn-in oven during the stress testing.

4.1 Design of LVTSCR-based Protection Circuit for 3kV HBM ESD Stress

As it was mentioned before, the main advantage of using LVTSCR is it's a high ESD protection level per unit area. After quasi-DC simulations, we also simulated human body 3kV ESD events at room temperature. The purpose of this analysis was to reduce the triggering voltage of LVTSCR from original 15V to acceptable level, which should be less than 9V. The GG-MOSFET (see Fig. 2(a)) was also simulated for the comparison. From the previous analysis, we found that the substrate triggering technique is optimal for burn-in conditions and we used this technique for V_{tr} reduction. The obtained simulation results are shown in Fig. 5. From these graphs, we can conclude that the developed technique for high V_h allows us to increase the holding voltage by 1.6X under transient operating conditions. The substrate triggering technique reduces the triggering voltage by 2X from 15V to 7.5V. To reduce the second voltage peak in LVTSCR with high V_h, the bulk electrodes of T2 and T3 transistors (see Fig. 2(b))

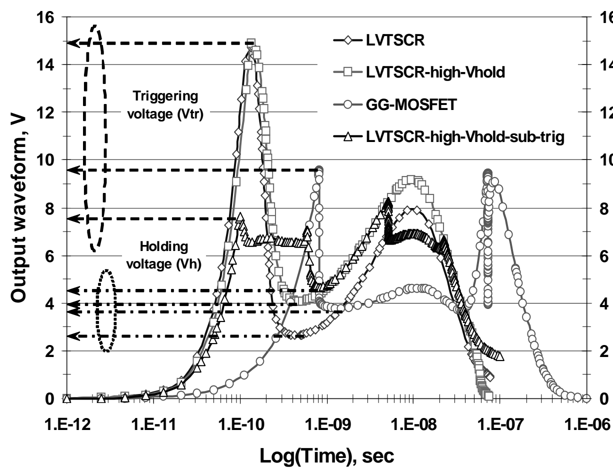

Fig. 5. Output waveform of LVTSCR-based protection circuits and GG-MOSFET under 3kV HBM ESD stress (T=300K).

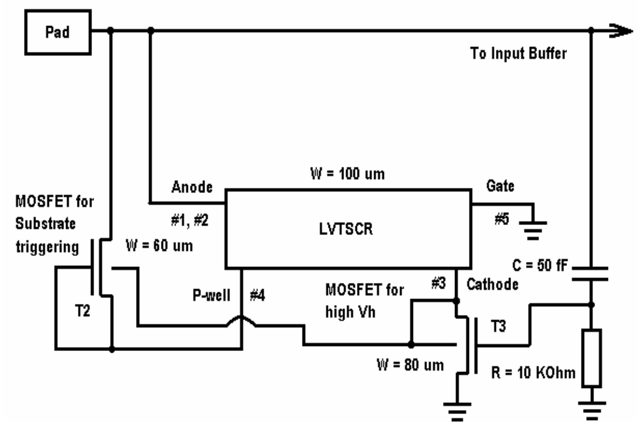

Fig. 6. LVTSCR-based EOS/ESD protection circuit developed for burn-in environment and sub-0.18 um CMOS technologies.

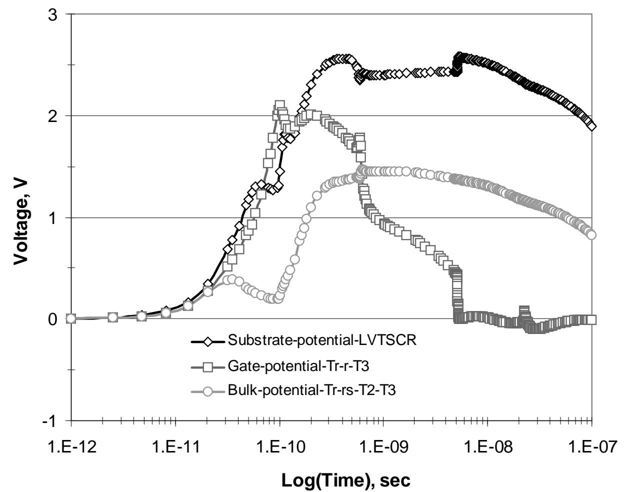

Fig. 7. Internal potentials in LVTSCR-based protection circuit under 3kV HBM ESD stress.

were connected together and were shorted with cathode terminal of LVTSCR. The final LVTSCR-based protection circuit, which was optimized for burn-in environment and sub-0.18 um CMOS technologies, is shown in Fig. 6. This circuit has less voltage peak by 20% (8V) and higher holding voltage by 25% (4.5V) in comparison with the conventional GG-MOSFET with the same device width at 3kV HBM ESD stress. The effectiveness of implemented techniques in LVTSCR-based protection circuit can be explained as follows: During the ESD stress, substrate and well potentials of LVTSCR and T2/T3 transistors significantly exceed the built-in *p-n* junction potential (~0.7 V) (see Fig. 7) and the parasitic BJT transistors are activated in these devices. As a result, the triggering voltage of proposed circuit becomes less than the triggering voltage of conventional LVTSCR and GG-MOSFET. The gate potential of T3

transistor exceeds his threshold voltage V_{th} (>0.5 V) as shown in Fig. 7. Hence, during the ESD event this transistor can pass significant current from the pad to ground. At normal and burn-in operating conditions T3 transistor provides the high holding voltage, which allows us to eliminate the lath-up in LVTSCR structure.

4.2 Evaluation of ESD Robustness of LVTSCR-based Protection Circuit

Generally, the destruction of an ESD device occurs at the threshold voltage, at which the maximum temperature in device structure reaches the melting point of silicon (1412°C) [13] (typically in the gate-to-drain overlap region) or the melting point of metallization (660°C for aluminum based metallization and 1034 °C for copper based metallization) [14]. To estimate the ESD robustness of proposed LVTSCR-based protection circuit, we performed thermal simulations and extracted peak temperature during the 3kV HBM ESD stress. For comparison, the same simulations were performed for the GG-MOSFET. The width of this device (240 um) was equalled to the total width of T2, T3 transistors and LVTSCR (see Fig. 6). The sizes of GG-MOSFET and LVTSCR-based protection device were chosen to prevent the internal heating more than 660°C at 3kV ESD stress. The thermal simulation results are shown in Fig. 8. From this figure, we can conclude that the self-heating effect in proposed LVTSCR-based protection circuit is less by 12% than the self-heating effect in GG-MOSFET. Hence, the ESD robustness of proposed ESC circuit is stronger than the ESD robustness of conventional GG-MOSFET. Note, that in the developed LVTSCR-based ESD protection circuit, the strongest heating has transistor T2.

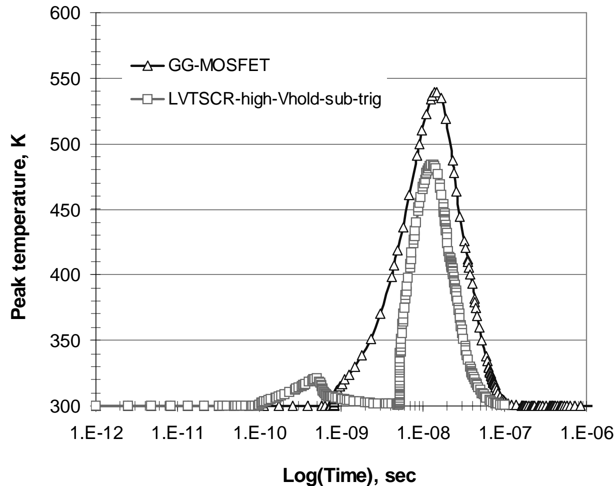

Fig. 8. Self-heating effect in ESD protection devices under 3kV HBM ESD stress.

5. Analytical Model for Temperature Dependence of Holding Current

In order to verify the validity of simulations results, an analytical model for holding current of LVTSCR is presented in this section. Fig. 9 (a) shows a simple model for LVTSCR which consists of parasitic bipolar and MOS transistors.

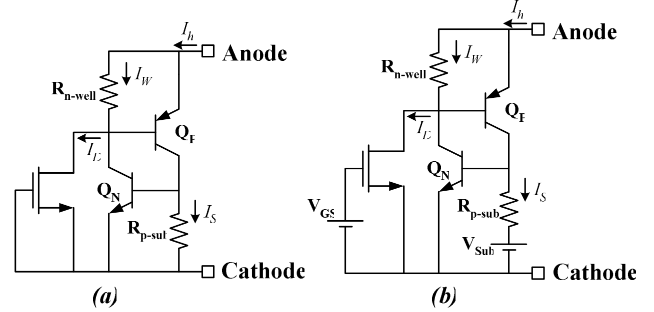

Fig. 9. (a) A model for LVTSCR (b) A model for gate-coupling and substrate-triggering effects.

Using collector current equations of bipolar transistors, the holding current of LVTSCR can be expressed as follows.

$$I_h = \frac{\beta_p(\beta_n+1)I_W + \beta_n(\beta_p+1)I_S}{\beta_n\beta_p - 1} - \frac{\beta_p+1}{\beta_n\beta_p-1} I_D\Big|_{V_{GS}=0} \quad (1)$$

It has been shown that the first term in Eq. 1 is the holding current of SCR [15]. Therefore,

$$I_{h(LVTSCR)} = I_{h(SCR)} - \frac{\beta_p+1}{\beta_n\beta_p-1} I_D\Big|_{V_{GS}=0} \quad (2)$$

In order to use this model under gate-coupling and substrate-triggering conditions, two bias voltages are added to the model, which represent gate and substrate bias of the LVTSCR. This model is shown in Fig. 9 (b). According to the new model, Eq. 1 can be modified to cover the effect of gate-coupling and substrate-triggering techniques. Holding current for gate-triggered LVTSCR (GTLVTSCR) and substrate-triggered LVTSCR (STLVTSCR) are given in equations 3 and 4 respectively.

$$I_{h(GTLVTSCR)} = I_{h(SCR)} - \frac{\beta_p+1}{\beta_n\beta_p-1} I_D\Big|_{V_{GS}} \quad (3)$$

$$I_{h(STLVTSCR)} = I_{h(SCR)} - \frac{\beta_p+1}{\beta_n\beta_p-1}\frac{V_{Sub}}{R_S} - \frac{\beta_p+1}{\beta_n\beta_p-1} I_D\Big|_{V_{GS}=0} \quad (4)$$

In order to model the temperature dependency of holding current, gain of bipolar transistors (β_n and β_p), well and substrate resistances (R_W and R_S), and MOSFET current (I_D) should be determined in terms of temperature. In other words, to predict variations of holding current under burn-in conditions, the temperature dependency of mobility (μ_p, μ_n), current gain of BJTs (β_p, β_n) and MOSFET threshold voltage (V_{th}) should be derived. It has been reported that V_{th} has a linear dependency on temperature. For 0.18μm technology, dV_{th}/dT is

0.6mV/°C [16]. In our research we used mobility models proposed by N. Arora et al. [17]. They developed electron and hole mobility models as a function of temperature and doping concentration.

For temperature dependence of β, a numerical expression (Eq. 5) has been proposed in [18].

$$\beta(T_2) = \beta(T_1)\left(1 + a(T_2 - T_1) + b(T_2 - T_1)^2\right) \quad (5)$$

where constants 'a' and 'b' can be determined from simulations. In order to find these values, the SCR structure has been divided into two parasitic bipolar transistors (Q_N and Q_P). Values of 'a' and 'b' were founded by extracting β from MEDICI simulations for two different temperatures.

To solve equations 2,3 and 4, a MATLAB simulator has been used. Fig. 10 shows the holding current of LVTSCR, GTLVTSCR and STLVTSCR for different temperatures. It can be seen that the holding current of STLVTSCR has the lowest dependency on temperature and the holding current of GTLVTSCR has the highest temperature dependency. This agrees with simulation results of Fig. 4, since ESD protection device has a resistive I-V characteristic after the snapback region and therefore holding voltage and holding current have the same temperature dependency trend.

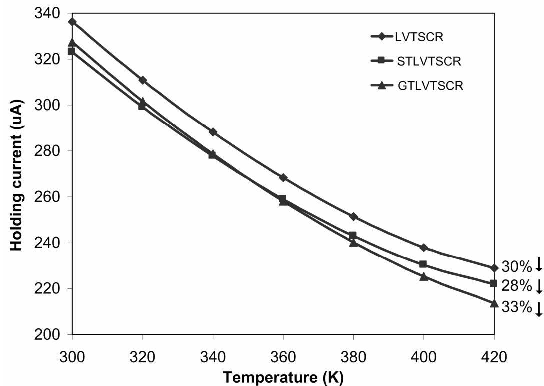

Fig. 10. Temperature dependency of holding current of LVTSCR with gate- and substrate-triggering.

6. Conclusion

This paper reports a new design of LVTSCR-based EOS/ESD protection circuit optimized for burn-in environment and sub-0.18 um CMOS technologies. The analytical model of holding voltage temperature dependency of LVTSCR-based structure has been developed. The proposed ESD circuit has higher holding voltage by 1.5X (3V) than the conventional LVTSCR structure (2V) at burn-in temperature. It allows us to eliminate the latch-up in LVTSCR due to voltage spikes (2.5V) on chip input pins during burn-in. Under 3kV HBM ESD stress, the developed LVTSCR-based protection circuit has the voltage peak (7.5V) less than the conventional LVTSCR structure (15V) by 2X and less than the GG-MOSFET (9.5V) by 1.25X. Hence, it can prevent the gate oxide breakdown due to ESD event in sub-0.18 um CMOS technologies. A new protection circuit has the self-heating effect less than the conventional GG-MOSFET by 12% at 3kV HBM ESD stress. Therefore, it has higher ESD robustness than the traditional ESD protection devices.

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