A New Flip-Flop-Based Transient Power Supply Clamp for ESD Protection

Hossein Sarbishaei, *Member, IEEE*, Oleg Semenov, *Member, IEEE*, and Manoj Sachdev, *Senior Member, IEEE*

***Abstract*—As CMOS technology is scaled, the design of a robust electrostatic-discharge (ESD) protection circuit that is transparent to the main circuit is becoming more challenging. For high-frequency applications where minimum parasitic capacitance is required, diodes along with clamps are a popular ESD protection method. The main challenge in the clamp design is to keep the clamp in "on" mode for the whole ESD event while minimizing area and avoiding false triggering. In this paper, a new clamp that uses a flip-flop to turn on the clamp for the complete ESD event is presented. The trigger circuit is able to keep the clamp on for over 2 μs, and this clamp passes a 3-kV HBM ESD stress. Simulation results show that this clamp is immune to false triggering and power supply noise. Furthermore, the stability problem in clamps is addressed, and the new clamp is shown to be immune to oscillation.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuit, flip-flop, transient ESD clamps.**

I. Introduction

ELECTROSTATIC discharge (ESD) is considered as a major reliability threat in the semiconductor industry for decades. It was reported that ESD and EOS are responsible for up to 70% of failures in IC technology [1]. Therefore, each I/O must be designed with a protection circuitry that creates a discharge path for ESD current. As CMOS technology scales down, the design of ESD protection circuits becomes more challenging. Thinner gate oxides and shallower junction depths in advanced technologies make CMOS circuits more vulnerable to ESD damage. Power supply ESD clamps are commonly used in many ICs as part of the whole chip ESD protection scheme. The main purpose of the clamp is to perform ESD protection between power supply pins. Furthermore, the clamp can be used as a part of the discharge path for other zapping modes as well [2]. In order to understand this method, consider Fig. 1 where a complete ESD protection for all zapping modes is shown. The main feature of this method is that the protection elements are not operating in snapback breakdown region. Therefore, this method is usually referred to as the nonsnapback protection. When a negative ESD pulse with respect to $V_{\rm SS}$ (NS mode) occurs, the discharge path is through the forward-biased diode D_2. On the other hand, on a positive ESD pulse with respect to $V_{\rm SS}$ (PS mode), the discharge path is through the forward-biased diode D_1 and the clamp. Similarly, discharge paths for positive and negative stresses with respect to $V_{\rm DD}$ (PD and ND modes) are through D_1 and D_2 clamps, respectively. It can be seen that in this configuration, clamp becomes a part of the discharge path for I/O pads as well [2].

Three types of nonsnapback clamp networks have been previously proposed: 1) the ESD clamps based on Zener diodes or string of forward-biased diodes [3], [4]; 2) the power supply reference ESD clamps [5]; and 3) the transient ESD clamps [6].

In this paper, we focus on the transient ESD clamps where the clamp consists of a wide NMOS transistor with a trigger circuitry (as shown in Fig. 1). The trigger circuit should turn on the NMOS transistor and keep it on during the whole ESD event (up to 1 μs for HBM model). On the other hand, the NMOS transistor should be kept off under normal operating conditions. Some of the key advantages of transient power clamps are the ability to provide ESD protection at low voltages, no added process steps, relaxed layout constraints, and easy SPICE simulations [6]. The major limitations of this method are the large RC network [6], the false triggering [6], and the possibility of oscillation [7]. In this paper, a new transient ESD clamp is proposed that overcomes these major limitations. The proposed clamp uses a flip-flop to latch the clamp into ON-state during the ESD event.

The rest of this paper is organized as follows. In Section II, previously proposed transient ESD clamps are reviewed, and their operating principles are discussed. A novel design of ESD clamp proposed in this paper is analyzed in Section III. Section IV presents the simulation results under ESD conditions, and Section V discusses the operation of the proposed clamp in normal conditions. The oscillation problem in transient clamps is addressed and analyzed in Section VI. Finally, the transmission-line-pulse (TLP) and HBM measurement results for the ESD clamp are presented in Section VII.

II. Operation of Transient ESD Clamps

Transient ESD clamps use an RC network to detect an ESD event and turn on a large device (usually a MOSFET) that shunts the ESD stress from the supply pin to the ground. One of the first transient clamps was proposed by Merrill *et al.* [8], which used an RC delay with three inverters to trigger the main discharging NMOS transistor. There are different versions of this clamp reported in literature as well [9]–[12]. Fig. 2 shows the schematic of one implementation of the clamp proposed by Merrill *et al.* This clamp uses a C–R coupling method instead of the RC delay.

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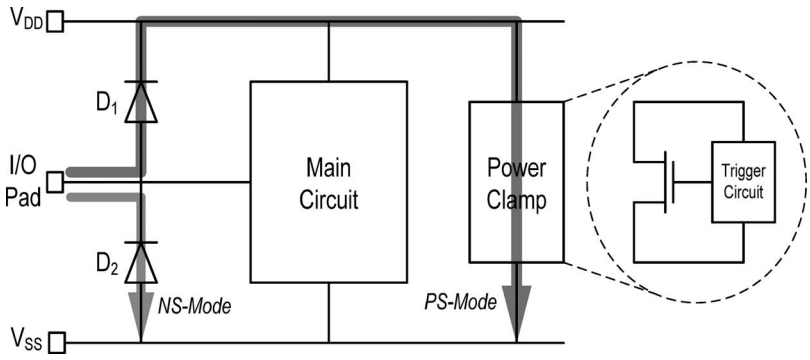

Fig. 1. Nonsnapback ESD protection method.

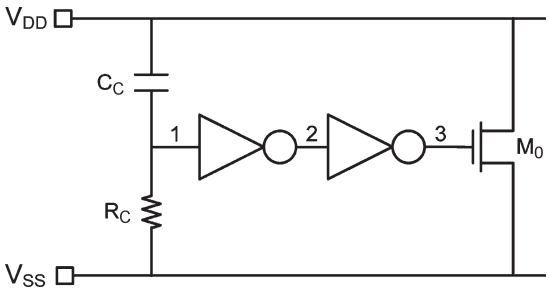

Fig. 2. Inverter-based transient ESD clamp.

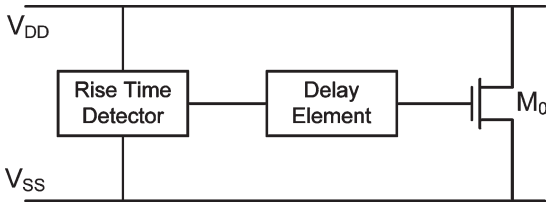

Fig. 3. Block diagram of the clamp with immunity to false triggering.

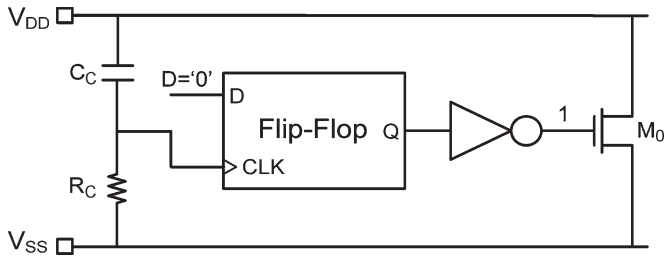

Fig. 4. Block diagram of the proposed clamp.

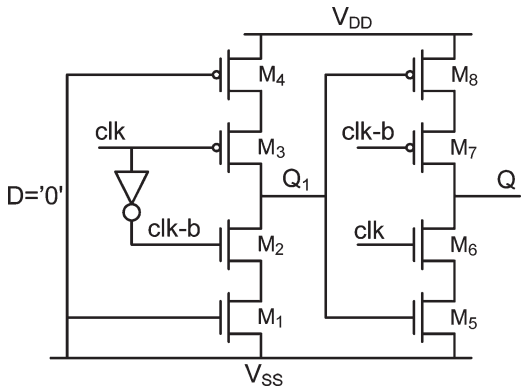

Fig. 5. D-type flip-flop with grounded input.

The triggering circuit of the clamp shown in Fig. 2 is based on the fact that the rise time of normal power up is on the order of milliseconds, whereas the rise time of the ESD event is between 100 ps and 60 ns [6]. Therefore, it is easy to distinguish the ESD event from the normal power-up condition using this clamp. Note that the RC time constant of the ESD clamp should be longer than the duration of the ESD event, which is from 500 ns to 1 μs for HBM ESD stress [6], and shorter than the rise time of normal power up, which is in millisecond range. Therefore, the typical value for the RC time constant is very large and around 1 μs. On the other hand, some applications, such as "hot-plug" operations or switching networks controlling the sleep power mode in low-power high-performance microprocessors, result in much faster power-up times on the order of a few microseconds [13] or even hundreds of nanoseconds [6]. Hence, this clamp might trigger under normal operating conditions as well. This phenomenon is usually referred to as false triggering.

To reduce the RC time constant and prevent false triggering, the triggering circuit is divided into two sections: a rise-time detector to detect the ESD event and a delay element to keep the clamp "on" for the complete ESD event. Fig. 3 shows the block diagram of such a transient clamp. The rise-time detector is usually implemented with a simple RC network. It has been shown that setting the time constant to 40 ns allows the detection of the ESD event and, at the same time, provides immunity to even very fast power-up events [6]. There are a wide range of transient clamps reported in literature with different designs for the delay element. The most common methods use either a feedback network [12]–[16] or a separate RC time constant [6] to design the delay element.

III. Novel ESD Clamp

As mentioned earlier, in order to design a clamp with immunity to false triggering, the triggering circuit is divided into two sections: the rise-time detector and the delay element. This delay element should be designed to keep the main transistor (M_0) in ON-state for the whole ESD event. In this paper, we used a rising-edge-triggered D-type flip-flop to create a delay element. Fig. 4 shows the block diagram of this clamp.

When an ESD event comes, a rising edge is detected at the clock input of the flip-flop. Therefore, the output of the flip-flop

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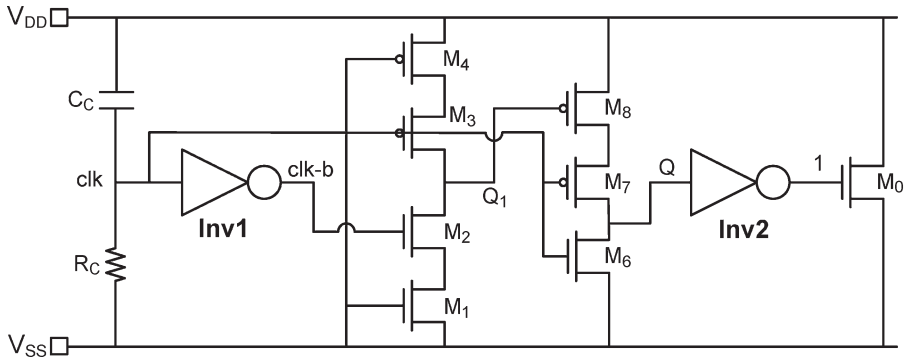

Fig. 6. Schematic of the new clamp.

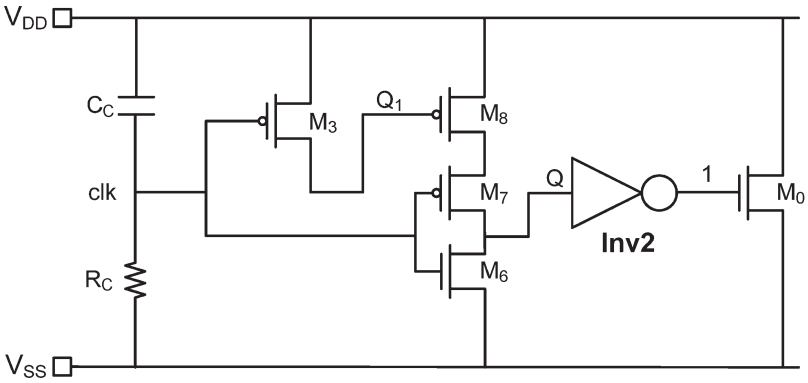

Fig. 7. Schematic of the modified FF-based clamp.

becomes "0," and M_0 turns on. The flip-flop holds its value, which means that M_0 continues to conduct during the whole ESD event. Fig. 5 shows the schematic of a D-type flip-flop with grounded input that is used in our research [17].

Although ESD performance of this circuit seems to be promising, this clamp has one major limitation. If the clamp triggers, there is no mechanism that can turn off the clamp. In other words, if a false triggering occurs during power up, the clamp cannot be turned off afterward, which creates a short circuit between $V_{\rm DD}$ and $V_{\rm SS}$. In order to solve this problem, the flip-flop design is modified based on our application. Consider the schematic of the D-type flip-flop shown in Fig. 5. The flip-flop evaluates its output on the rising edge of the clock. As the D input of the flip-flop is always low (or simply "0"), the voltage of node $\rm Q_1$ is high (or simply "1"). Hence, transistor M_5 is always "on" and can be removed without affecting the operation of the clamp. In order to create a turn-off mechanism for the clamp, the gate connection of M_7 is changed from "clk-b" to "clk." The schematic of the clamp with the modified flip-flop is shown in Fig. 6.

Now, let us try to understand the turn-off mechanism of the clamp. Under normal operating conditions, and when the supply voltage is constant at $V_{\rm DD}$, capacitor C_C is fully charged, and voltage of the node "clk" is zero. As a result, both nodes "clk-b" and "$\rm Q_1$" are charged to $V_{\rm DD}$. Therefore, transistors M_6 and M_8 are "off," and transistor M_7 is "on." In order to make sure that the clamp is "off," the voltage of node "Q" should be high. Hence, widths of M_7 and M_8 are designed to be higher than M_6 to be able to pull up the node "Q" completely. It should be noted that node "Q" is charged through the leakage currents of M_7 and M_8. For proper operation, we ensured that the leakage of M_8 is at least 20 times higher than M_6. Similar concept was used in the clamp with cascaded PMOS feedback as well, where difference in leakage of transistors was used to solve the false-triggering problem of the clamp [15].

During a power-up event, supply voltage ramps from 0 to $V_{\rm DD}$. The rise time of the power-up event is in microsecond to millisecond range. To ensure immunity to false triggering, the R_CC_C time constant of the clamp is set to 40 ns. As a result, during a power-up event, the clock input of the flip-flop does not see a rising edge. However, if, by any reason, the flip-flop triggers during power up, as mentioned earlier, the sizing of M_6, M_7, and M_8 is in such a way that after the voltages of nodes "$V_{\rm DD}$" and "clk" are settled, the voltage of node "Q" rises to $V_{\rm DD}$, and the clamp turns off. It can be seen that the difference in leakage current of M6 and M8 is the key factor in implementing the turn-off mechanism of the clamp. Complete discussion and simulation results on this matter are presented in Section V.

The schematic of the new clamp can be further simplified. Based on the operation of the clamp, and knowing that input of the flip-flop is always zero, one can see that the pull-down network of node "$\rm Q_1$" (transistors M_1 and M_2) is not activated and that transistor M_4 is always "on." Hence, the first inverter (Inv1) and transistors M_1, M_2, and M_4 can be simply eliminated without affecting the circuit operation under both ESD and normal power-up conditions. Fig. 7 shows the schematic of the simplified FF-based clamp.

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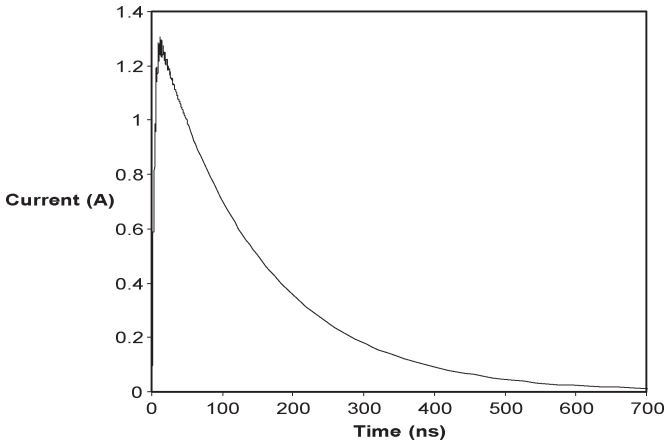

Fig. 8. Two-kilovolt HBM ESD current waveform.

In this paper, we fabricated the clamp shown in Fig. 6. As a result, in the rest of this paper, all the discussions, simulations, and measurement results are based on this clamp. However, our simulations show that the simplified clamp shown in Fig. 7 has the same performance as the original clamp under both the ESD and normal operating conditions.

IV. ESD Operation

In order to evaluate the effectiveness of this clamp under ESD conditions, its response to a 2-kV HBM stress is simulated in both circuit and device levels. The HBM test is the main ESD test method which is widely used in industry, and it is defined in the MIL-STD-883 standard (method 3015.7). In this standard, the HBM waveform has a rise time of less than 10 ns and a delay time of 120–180 ns. For a 2-kV ESD stress, the peak current is 1.33 A $\pm$ 10%. The transient current waveform used in our simulations is shown in Fig. 8.

A. Circuit-Level Simulations

One of the key features of the nonsnapback ESD protection scheme is the possibility to simulate the clamp using circuit-level simulation tools such as Cadence. This feature is based on the fact that the transistors of the clamp are not operating in their breakdown region. In order to simulate this clamp with Cadence, the ESD stress shown in Fig. 8 is applied to the $V_{\rm DD}$ line with grounded $V_{\rm SS}$. The circuit is simulated in a 0.18-μm CMOS technology with $t_{\rm ox} = 40$ Å. The transistor M_0 is designed with minimum length and 400 μm width. Fig. 9(a) and (b) shows the voltage of different nodes under this stress. It can be seen that as the ESD event occurs, a rising edge is detected at node "clk," and hence, the output of the flip-flop (node "Q") becomes "0," which turns on transistor M_0.

As the voltages of nodes "$V_{\rm DD}$," "Q_1," and "1" are the same during a 2-μs simulation time, the clamp is "on" for over 2 μs which is enough to discharge the ESD energy completely. The peak voltage of the supply line during the 2-kV stress is 5.8 V. Since the gate-oxide breakdown voltage of transistors in a 0.18-μs CMOS technology under 100-ns voltage pulse is around 8 V [18], this new clamp can effectively protect the core circuit against a 2-kV ESD stress.

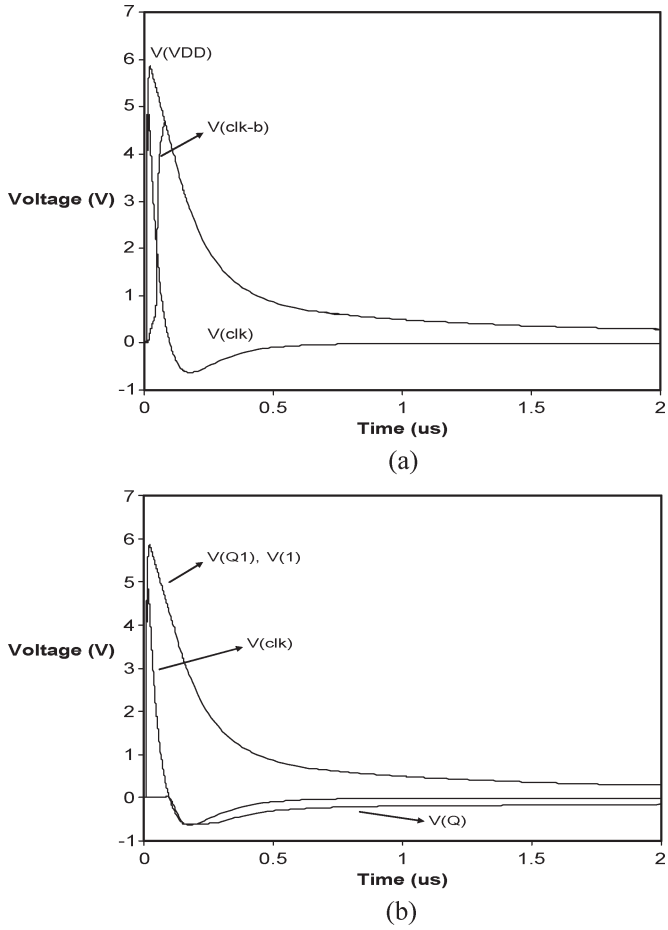

Fig. 9. ESD response to a 2-kV HBM stress. (a) Voltage of nodes $V_{\rm DD}$, clk, and clk-b. (b) Voltage of nodes Q, Q1, 1, and clk.

B. Device-Level Simulations

Although the nonsnapback ESD clamps can be simulated with circuit simulators, their high current behavior and self-heating effect require device-level simulations. In this paper, we used the 2-D "SEQUOIA ESD" device simulation software, which was developed by Sequoia Design Systems to characterize the ESD events [19]. This simulator has built-in device synthesis, mesh generation, device simulation, circuit-device mixed-mode simulation, and lattice self-heating simulation modules. Validity of physical models, such as mobility, generation–recombination, and impact-ionization rates, has been confirmed in numerous industrial applications and is accurate up to 700 K. In our simulations, the Lombardi low electric field and the Caughey–Thomas high electric field mobility models were used. The Chynoweth model and the Shockley–Read–Hall model were used for the modeling of the impact-ionization and the generation-recombination processes.

The transistor structures in the ESD clamp are designed by using process parameters of the 0.18-μm silicided CMOS technology. The physical structure of the ESD device used in our simulations is shown in Fig. 10. For thermal simulations, a thermal electrode is placed at the bottom of the substrate, and the temperature of this electrode is assumed to be the same as ambient temperature (300 K). All contacts are ideal ohmic

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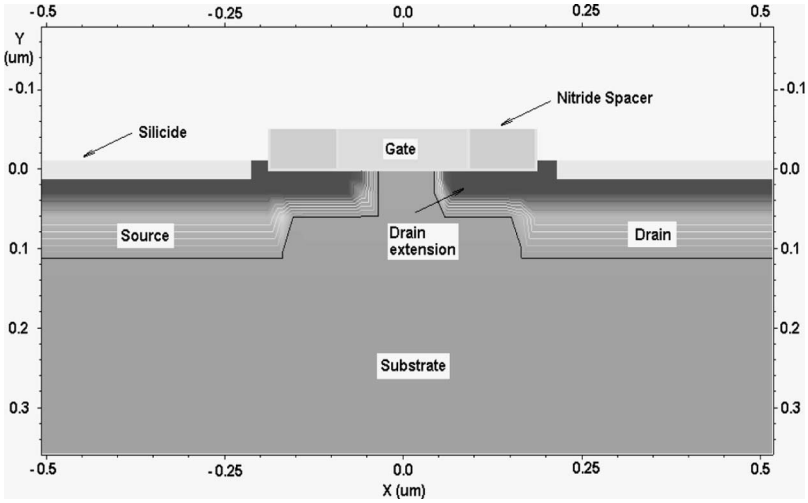

Fig. 10. Cross section of the 0.18-μm NMOS transistor.

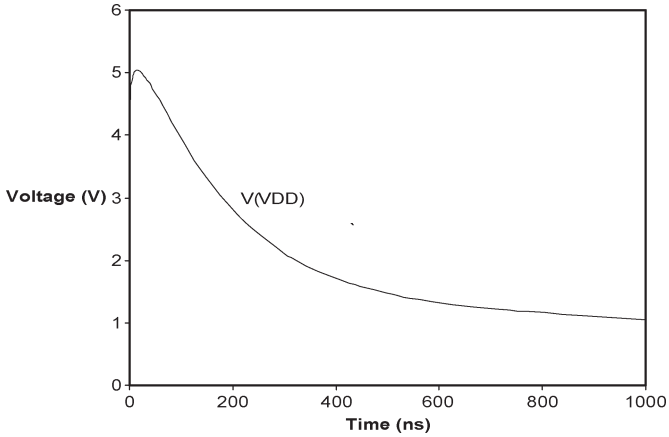

Fig. 11. Voltage of the $V_{\rm DD}$ line under a 2-kV HBM stress.

electrodes. In order to verify the reliability of the transistors, their maximum temperature should be less than the melting point of metallization (660 °C for aluminum-based metallization and 1034 °C for copper-based metallization) and the melting point of silicon (1412 °C) [20].

The 2-kV HBM stress is applied to the $V_{\rm DD}$ line of the proposed clamp in the device simulator, whereas the $V_{\rm SS}$ line is grounded. The failure of the clamp is tested by monitoring the maximum temperature of all transistors. The peak temperature during this stress is 400 K, which is in the gate–drain boundary of the main transistor M_0. As this temperature is less than the melting point of metallization and silicon, this clamp passes the 2-kV stress. Fig. 11 shows the voltage of the $V_{\rm DD}$ node under this stress.

Comparing the results from Cadence to those from Sequoia shows that the device simulator is predicting a lower peak voltage under ESD conditions. This difference is due to the impact-ionization effect, which is becoming significant in high current mode. In the circuit simulators, like Cadence, the impact of the parasitic bipolar action of M_0 is neglected. Therefore, the current flow through the protection device is underestimated [21].

V. Normal Conditions

In addition to ESD response, the new clamp should be tested under normal operating conditions as well. The first experiment is to ensure that the clamp is off when the supply voltage is connected to $V_{\rm DD}$. Cadence simulations show that with 1.8-V supply voltage, the clamp is off and has a very low leakage current of 8 nA. As false triggering is the main drawback of transient clamps, the new clamp is simulated under very fast power-up conditions with $t_r = 1$ μs. Furthermore, in order to make sure that M_0 turns off after false triggering, the rise time is further reduced to 50 ns. Finally, the immunity to power supply noise is investigated in this section as well.

A. Immunity to False Triggering

The immunity to false triggering is evaluated by applying a ramp from 0 to $V_{\rm DD}$ with different rise times. In regular applications, power up is a very slow event where the rise time is in millisecond range. However, in some applications such as hot-plug operations, the rise time can be as low as 1 μs that may cause false triggering. Hence, to test the worst case scenario, the new clamp is simulated for a 1-μs power-up event. In order to avoid false triggering, the gate voltage of M_0 (node "trig") should be less than its threshold voltage ($\sim$0.45 V). Fig. 12 shows the voltage of different nodes for a 1-μs power up.

It can be seen that the gate voltage of M_0 (node "1") rises to 0.12 V and goes back to zero immediately. Hence, even with a very fast power-up event, this clamp does not trigger, which ensures the immunity to false triggering. It should be noted that at time $t = 2$ μs, the voltage of node "Q" is around 1.5 V, which is high enough to pull down the output of the last inverter (Inv2). However, based on the discussions in Section III, this voltage should increase to 1.8 V. Increasing the simulation time shows that this voltage eventually rises to 1.8 V within 100 μs.

As mentioned earlier, the concept of using a flip-flop to latch the gate of M_0 to "1" under ESD conditions brings the concern of turning off the clamp after false triggering. Therefore, another set of experiment is necessary to verify the turn-off mechanism of the clamp. As a result, the rise time of

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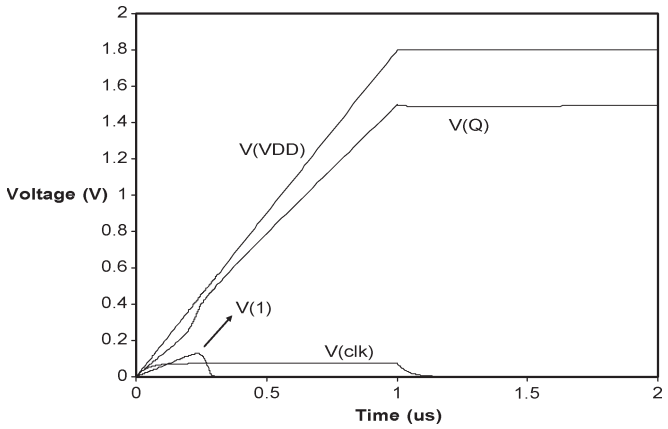

Fig. 12. Proposed clamp under 1-μs power-up condition.

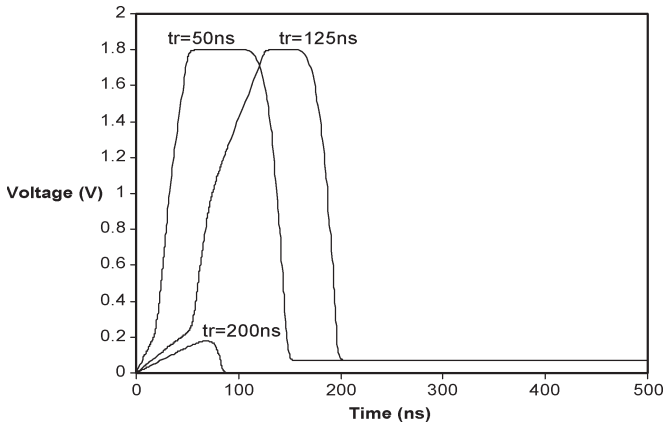

Fig. 13. Voltage of node 1 for $t_r = 50$, 125, and 200 ns.

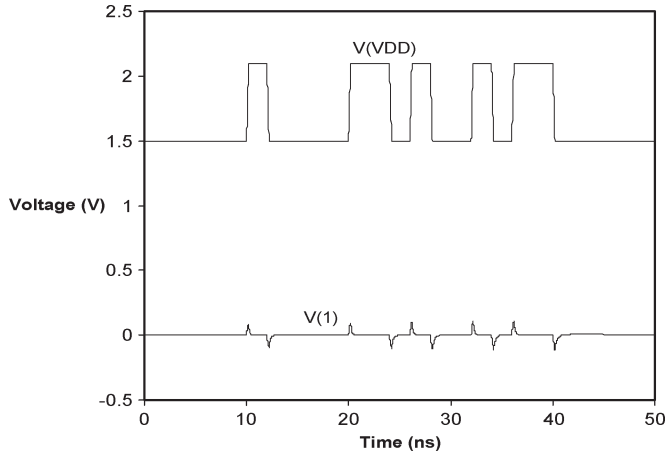

Fig. 14. Power supply noise immunity: Voltage of nodes 1 and $V_{\rm DD}$.

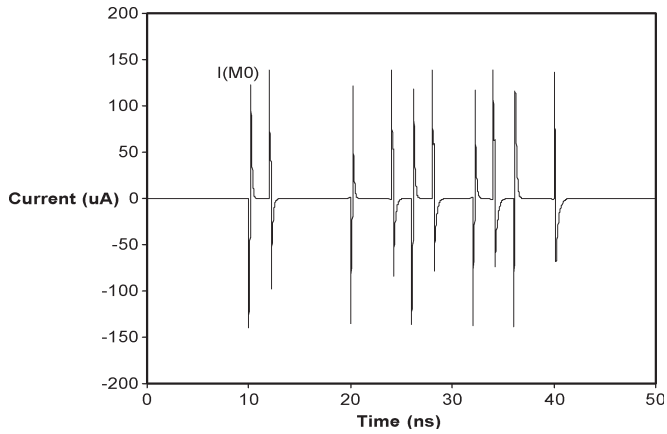

Fig. 15. Power supply noise immunity: Current of transistor M_0.

the power-up event is further reduced to 200, 125, and 50 ns. Fig. 13 shows the voltage of node "1" during these power-up events.

It can be seen that for the higher rise time of 200 ns, the clamp does not trigger. On the other hand, for smaller rise times of 125 and 50 ns, the clamp turns on at the power-up event but turns off after less than 50 ns. As explained in Section III, this is the time required to the charge capacitor C_C and the pull-up voltage of node "Q." This simulation ensures that the turn-off mechanism of the clamp under normal operating conditions is effective.

The concept of turn-off mechanism of the clamp brings up the concern that, similar to power up with rise times of 50 and 125 ns, the clamp may turn off under ESD conditions as well. Consider the ESD response shown in Fig. 9. It can be seen that at the ESD event, a rising edge occurs at the input of the flip-flop which discharges the voltage of node "Q" to ground and turns on the clamp. However, unlike the normal operating conditions, the voltage of node "Q" is not charging toward $V_{\rm DD}$ afterward. As discussed in Section III, node "Q" is charged through the leakage current of transistors M_7 and M_8. During an HBM stress, the source of ESD energy is the charge stored in a 100-pF capacitance. This energy is mainly transferred to ground through M_0, and hence, there is no enough energy to charge the node "Q." On the other hand, during a power-up event, a voltage source provides the energy that supplies enough current to turn off the clamp. In order to verify this explanation, we reduced the discharge current of the clamp by reducing the width of M_0. We found that if the width of M_0 is reduced to 20 μm (from the original value of 400 μm), the clamp turns off under ESD conditions as well. Another method to confirm this explanation is to increase the ESD energy and see if the clamp turns off during the ESD stress. Hence, we increased $C_{\rm HBM}$ and observed that increasing $C_{\rm HBM}$ to 2 nF (from the original value of 100 pF) turns off the clamp after the ESD stress. It can be seen that there is enough margin in our design to ensure that the turn-off mechanism does not degrade the ESD performance.

B. Immunity to Power Supply Noise

The power supply noise becomes an important factor in circuits with high switching rates. The impact of power supply noise on the clamp is simulated by adding a pseudorandom pulse to the supply voltage. In order to simulate the clamp under worst case conditions, the added noise has a rate of 500 Mb/s and the amplitude of 600 $\rm mV_{p-p}$ [13]. This bit sequence, along with the voltage of node 1, is shown in Fig. 14, whereas Fig. 15 shows the current of the main clamp transistor M_0.

It can be seen that the peak current of the clamp is approximately 150 μA which is very small considering the amplitude of the noise on the supply line. Hence, the new clamp is immune to power supply noise.

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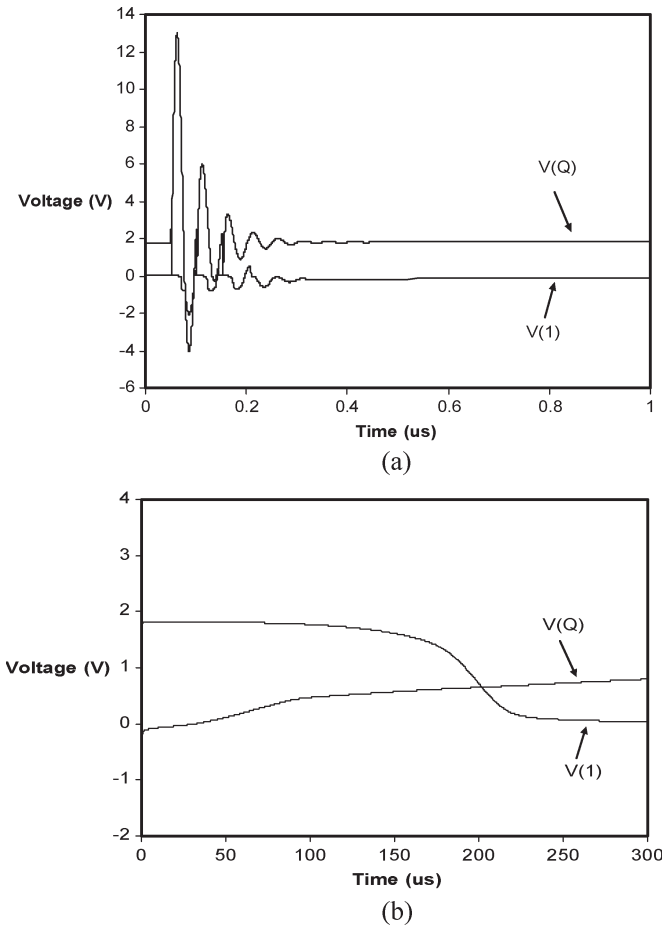

Fig. 16. Voltage of nodes "1" and "Q" during the system-level ESD test. (a) First 500 ns of the waveform. (b) Complete waveform showing that the clamp turns off after stress.

C. System-Level Simulation

System-level ESD test has become more important in recent years [22], [23]. It has been reported that ESD protection circuits, after passing chip-level test, may fail under system-level test. Specifically, failure of some transient clamps under system-level test has been reported in [24]. The failure is observed as a significant increase in leakage current of the clamp after the stress. In other words, after the system-level test, the clamp may not turn off and cause failure. Simulation of the system-level test is done by applying a damped sine voltage to $V_{\rm DD}$ as follows [22]:

$$V = V_0 + V_a e^{-(t-t_d)D_a} \sin(2\pi f(t-t_d)).$$

In order to simulate the clamp under system-level test, the parameters of the equation are set as: $V_0 = V_{\rm DD} = 1.8$ V, $V_a = 14.6$ V, $D_a = 2 \times 10$ s^{-1}, $t_d = 50$ ns, and $f = 20$ MHz. This voltage is applied to the $V_{\rm DD}$ line of the proposed clamp. Fig. 16 shows the voltage of nodes "Q" and "1" of the clamp. The first 1 μs of the waveform is shown in Fig. 16(a). It can be seen that after the stress, V(1) remains at 1.8 V, and the clamp keeps conducting. However, simulating the clamp for 300 μs, as shown in Fig. 16(b), shows that the clamp eventually turns off at $\sim$200 μs. Hence, the proposed clamp passes the system-level test as well.

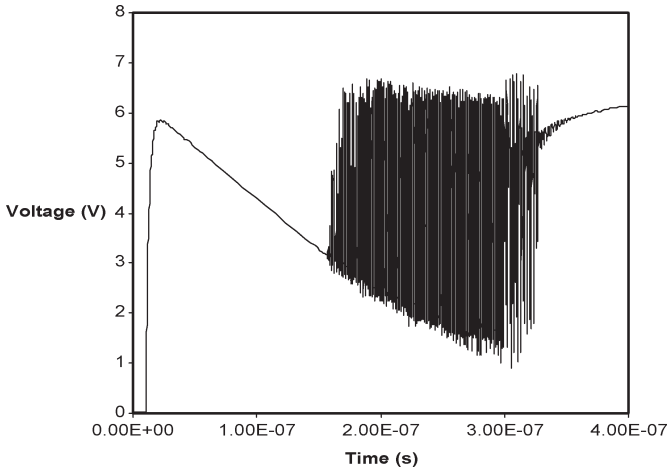

Fig. 17. Voltage of the $V_{\rm DD}$ node of the inverter-based clamp during the 2-kV ESD stress.

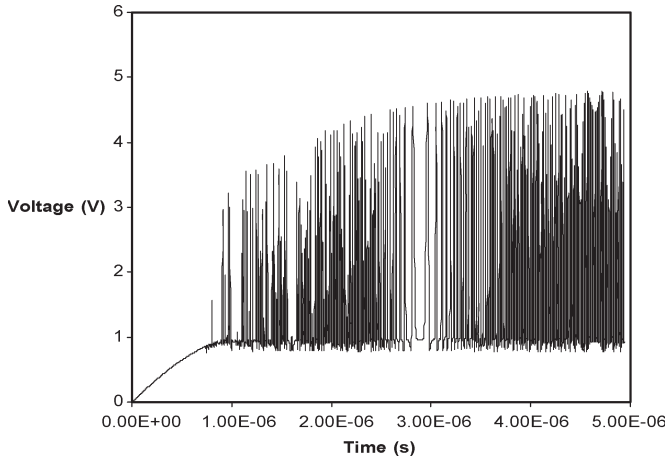

Fig. 18. Voltage of the $V_{\rm DD}$ node of the inverter-based clamp during the 3-μs power up.

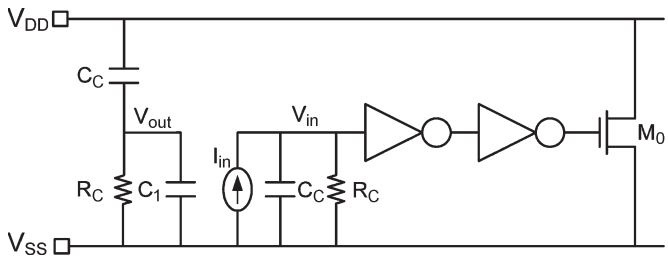

Fig. 19. Setup to simulate the open loop gain of the inverter-based clamp.

It should be noted that the 200-μs turn-off time can be reduced by modifying the design of transistor M_8. Leakage of this transistor determines the delay in turning off the clamp. Hence, upsizing this transistor or designing it with low threshold transistor helps reduce this delay.

VI. Immunity to Oscillation

As mentioned earlier, transient clamps usually suffer from large area and false triggering. Another issue that has been

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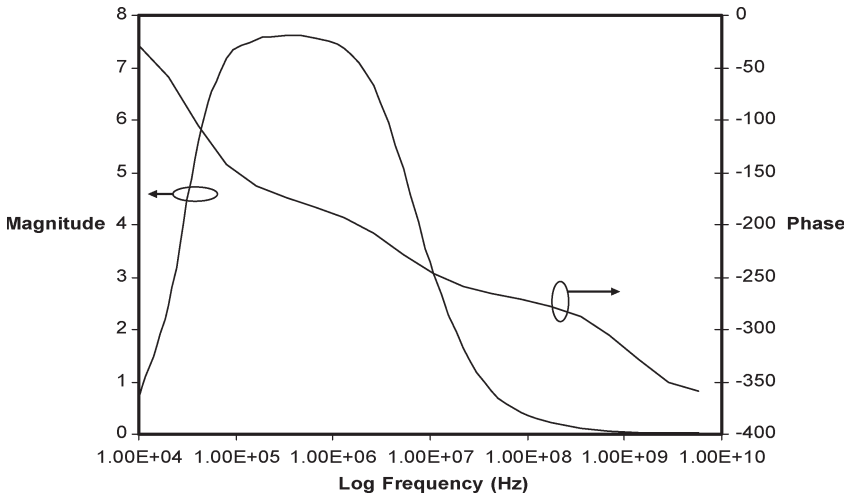

Fig. 20. Magnitude and phase of the open loop gain of the inverter-based clamp.

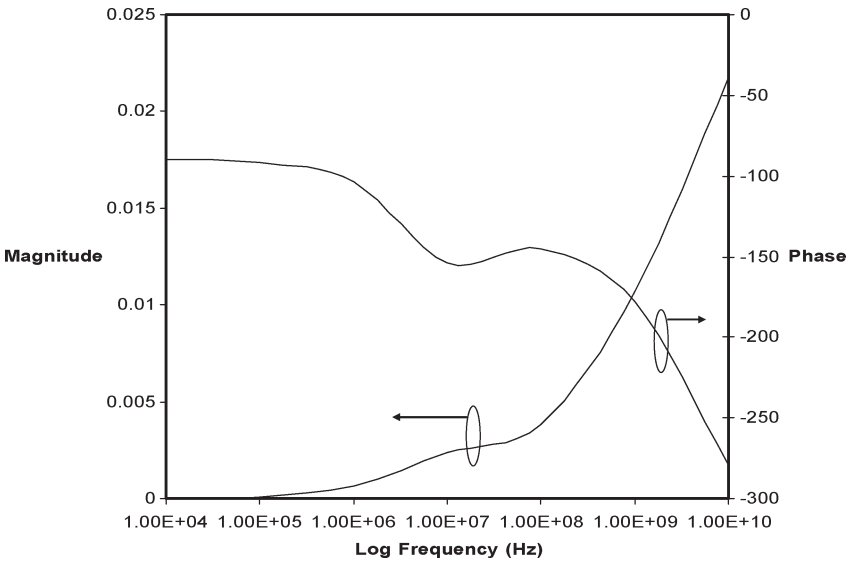

Fig. 21. Magnitude and phase of the loop gain of the proposed clamp.

addressed recently is the possibility of oscillation during power-up and/or ESD conditions [7]. This issue has been observed as a high-frequency oscillation on the power rails. In order to understand the nature of these oscillations, consider the inverter-based clamp shown in Fig. 2. Under the ESD conditions, the voltage of the $V_{\rm DD}$ line suddenly increases. Capacitor C_C transfers this transition to node "1" as well. Going through two inverters, gate voltage of the main transistor increases and turns on the clamp. As the ESD energy starts to decay, voltage of the "$V_{\rm DD}$" line starts to decrease. Voltage of the node "1" decreases with a slower rate due to the high RC constant. As the voltage of node "1" reaches the triggering voltage of the first inverter, the inverter chain turns off the main clamp transistor. As a result, the voltage of the "$V_{\rm DD}$" line increases, which increases the voltage of the node "1" as well. If the RC time constant is high enough, the voltage increase in node "1" turns on the inverter again. This process is observed as an oscillation on the $V_{\rm DD}$ line. The inverter-based clamp was designed by setting the width of M_0 to 400 μm. The ESD response to a 2-kV HBM stress was simulated in Cadence. Fig. 17 shows the voltage of the "$V_{\rm DD}$" node during this experiment where a high-frequency oscillation is observed. It should be noted that these oscillations can be ignored as long as their magnitude is not more than the oxide breakdown voltage and they have a limited duration.

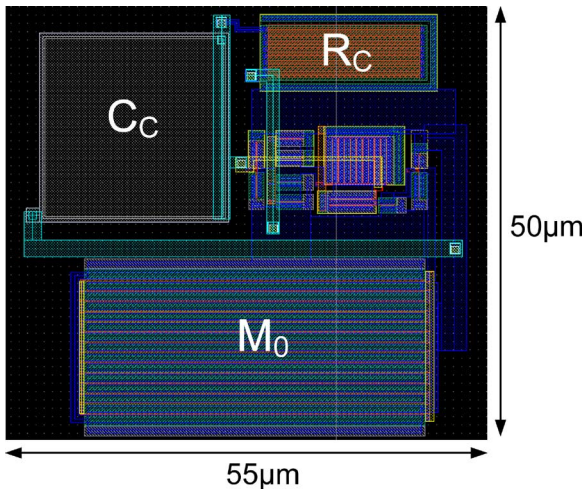

Fig. 22. Layout of the proposed clamp.

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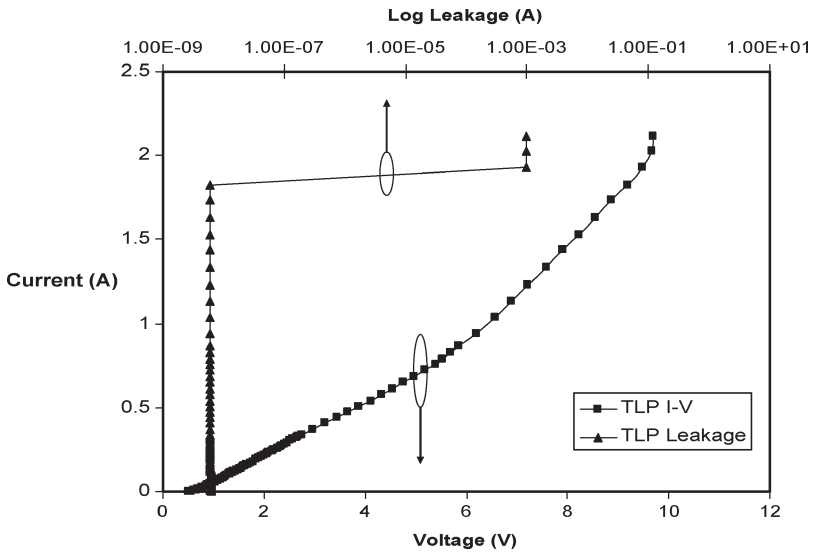

Fig. 23. TLP measurement results for the proposed clamp.

Similar phenomenon happens during power up as well. In this case, as the voltage of the power line increases from zero to $V_{\rm DD}$ (with a much slower rate than the ESD event), the voltage of node 1 increases as well. Due to the high RC delay time, the voltage difference between nodes "1" and "$V_{\rm DD}$" starts to increase. Therefore, after a while, the voltage of node "1" becomes less than the triggering voltage of the inverter, and the clamp turns off. Hence, the voltage of the "$V_{\rm DD}$" line increases, which, in turn, increases the voltage of node "1." This rapid change in the voltage of the "$V_{\rm DD}$" line creates oscillation on the power line. Again, the inverter-based clamp was simulated in Cadence, and Fig. 18 shows the oscillation observed during a power-up event with a 3-μs rise time.

The frequency and existence of this oscillation is a function of the rise time of power up as well as the load of the power line. Unlike the oscillations under ESD conditions, the oscillations under normal power up can cause serious issues in normal operating conditions of the main circuit and should be eliminated.

In order to compare the ESD clamps shown in Figs. 2, 3, and 6 based on their stability, we propose a quantitative analysis of their stability. Referring back to the oscillation theory, the condition of oscillation is based on the open loop gain of the clamp. The loop is unstable when the magnitude of the open loop gain is one and the phase of the open loop gain is 180°. In transient clamps, the loop is closed through the power supply rail. Due to the logic of the transient clamps, an odd number of inversions (including the R_C-C_C network) exists in the loop. Hence, the condition of 180° phase is satisfied, and in order to stabilize the loop, the magnitude of the open loop gain should be kept below 1. In order to simulate the open loop gain of the inverter-based clamp, the feedback loop is opened at node 1, and the impedance seen from each side is added to the other side. Fig. 19 shows the setup used to simulate the open loop gain of the inverter-based clamp.

In this figure, C_1 is the input capacitance of the first inverter, and the loop gain is defined as $V_o/V_{\rm in}$. By running an ac simulation in Cadence, the magnitude and the phase of the loop gain are evaluated. Fig. 20 shows the magnitude and the phase of the open loop gain.

It can be seen that, for the inverter-based clamp, a possibility of oscillation exists where the magnitude and the phase of the loop gain are 8.49 and -180°, respectively. Similar analysis is applied to the proposed clamp to ensure the stability of our design. Fig. 21 shows the magnitude and the phase of the proposed clamp.

It can be seen that the magnitude of the loop gain of the proposed clamp is always less than one, and hence, the clamp is immune to oscillation.

VII. TLP and HBM Measurements

The proposed clamp has been fabricated in the 0.18-μm CMOS technology. In this clamp, R_C and C_C were set to 500 fF and 80 kΩ, respectively, to detect the rise time of the ESD event. M_0 was 400 μm wide that is realized in a 20-finger configuration, and the total design was 50 μm $\times$ 55 μm. Fig. 22 shows the layout of the proposed clamp.

In the first step, the second breakdown current of this clamp was determined by using TLP test. Fig. 23 shows the TLP measurement results for this clamp using 100-ns-wide pulses with 10-ns rise time. It can be seen that the leakage current at $V_{\rm DD} =$ 1.8 V is 6 nA and that the second breakdown current is 1.83 A.

Furthermore, the HBM test has been done on the clamp as well. We applied both the positive and negative HBM stresses with 500-V step sizes. This clamp passes 3-kV stress but fails at 3.5-kV stress. These results are confirmed by using the device simulator as well. For the 3-kV input stress, the peak temperature of the transistors exceeds 500 K, whereas for 4 kV, the peak temperature was over 1000 K. Hence, this clamp should pass the 3-kV stress but fail the 4-kV HBM stress.

VIII. Conclusion

In this paper, a new transient clamp was presented that could increase the turn-on time significantly. This clamp was based on using a flip-flop to latch the clamp into "ON"-state during the

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ESD event and was modified to turn off after false triggering. Simulation results show that this clamp is immune to false triggering and power supply noise. Furthermore, an analysis on the stability of the clamp was presented, which shows that the new clamp is immune to oscillation as well. Finally, the TLP and HBM measurement results show that the new clamp passes the 3-kV ESD stress.

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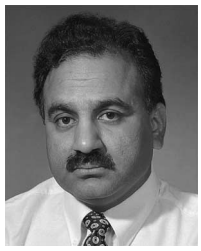

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