ESD Protection Circuit for 8.5Gbps I/Os in 90nm CMOS Technology

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***Abstract*—In this paper we designed an ESD protected CML driver for 8.5Gbps data rate. ESD protection for this circuit is provided with DSCR. A detailed analysis is done on the impact of ESD protection on performance of the driver. It is shown that DSCR offers up to 2.7kV HBM protection with very small impact on performance of the driver.**

I. Introduction

Electrostatic discharge protection is becoming ever more challenging as CMOS technology is scaled. This challenge is mainly due to thinner gate oxides, smaller channel lengths and shallower junctions. At the same time, scaling of CMOS technology is accompanied by increase in operating frequency of circuits. As a result, the maximum capacitance that can be added to high speed I/Os through the ESD protection device is becoming very limited. This trade off necessitates a full study on the interaction between the ESD protection device and the main circuit in high speed applications. There are a number of publications addressing this issue. Majority of these publications are targeting RF circuits, mainly low noise amplifiers. There are also a few papers on the interaction between high performance circuits and ESD protection devices [1], [2], [3]. In [1] the impact of ESD protection circuits on distortion of analog to digital converters is investigated. A comparison between MOS-based and SCR-based ESD devices on current mode logic (CML) drivers is presented in [2]. In [3] an ESD protection circuit is designed for a 2.5GHz receiver.

In this paper we studied ESD protection for I/Os with higher data rates than previous publications. The reference circuit is a CML driver operating with data rates as high as 8.5Gbps. Schematic of this driver is shown in Fig. 1.

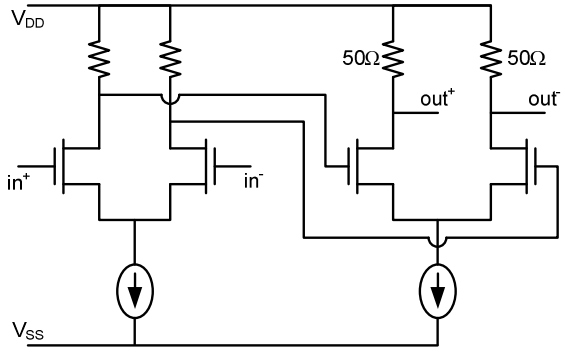


Fig. 1. Schematic of the two stage CML driver

The driver in Fig. 1 is designed in 90nm CMOS technology. The main requirement for ESD protection circuit in high speed applications is to minimize the overall capacitance of the ESD device. The rest of the paper is organized as follows: In section II different ESD protection devices are discussed. Section III presents measurement results for the driver with ESD protection. In the first part performance of the driver under normal conditions is evaluated and finally, in the second part ESD protection level of the driver is tested using TLP test method.

II. ESD Protection Device

In CMOS technology ESD protection is often provided with either diodes, MOSFETs or Silicon Controlled Rectifiers (SCRs). Due to its low capacitance, diode is a popular candidate for ESD protection in high speed applications. However, as diodes can only be used in forward bias conditions, discharge path should be through supply rails and a clamp between V_{DD} and V_{SS} [4]. The main drawback for this method is the extra voltage drop across supply path that can cause ESD failure especially in modern nano-metric technologies [5]. SCR is another popular ESD device that offers highest ESD protection level per unit area [6]. This feature makes SCR a promising device for high speed applications. The main drawback of SCR is its high first breakdown voltage. There are a number of techniques to reduce its first breakdown voltage. However, these methods are often accompanied by extra capacitance added through triggering devices [7], [8], [9]. Recently we designed an SCR-based device in 180nm technology that reduces the first breakdown voltage of a conventional SCR with very small capacitance overhead [10]. In this research we used the same device to protect a high speed circuit with minimum impact on the performance. Fig. 2 shows cross section and schematic of this ESD protection device, which is called Darlington-based SCR (DSCR) [10].

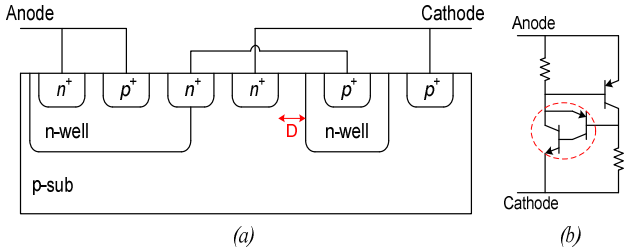


Fig. 2. Darlington-based SCR (DSCR) (a) cross section (b) schematic

The first breakdown voltage of this device is a function of n^+ to n-well spacing which is called 'D' (Fig. 2(a)). Reducing 'D' reduces the first breakdown voltage of DSCR. At the same time, designing 'D' too small increases leakage of the device under normal operating conditions. In the first step, this device is simulated using Medici in 90nm technology. The first breakdown voltage of DSCR is simulated by running quasi-DC simulation in Medici. Fig. 3 shows the I-V characteristic of a 100µm wide DSCR by setting 'D' to 0.4µm. It can be seen that the first breakdown voltage of this device is 3.5V. The main feature of this device is that reduction in the first breakdown voltage is done without requiring any triggering transistors.

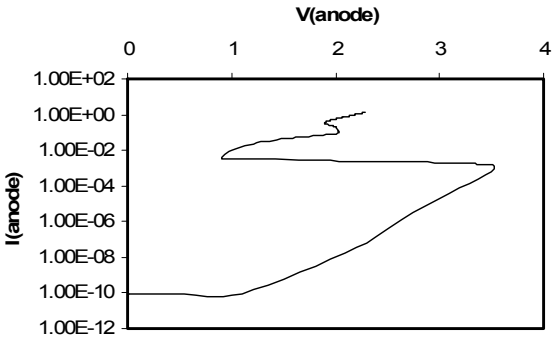


Fig. 3. Simulated I-V characteristic of the DSCR

In order to verify simulation results, a 50µm wide DSCR was fabricated in 90nm technology by setting 'D' to 0.4µm. TLP measurements are done using 100ns pulses with 10ns rise time. Fig. 4 shows TLP measurement results for the DSCR device.

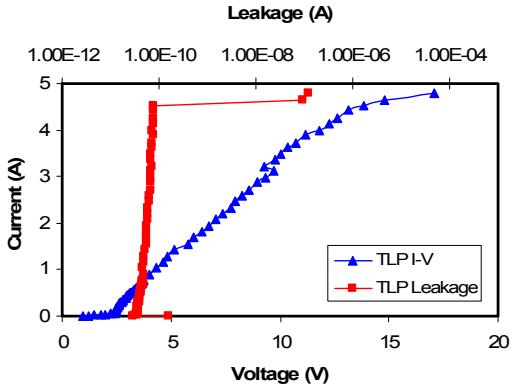


Fig. 4. TLP measurement results for the DSCR

It can be seen that the first breakdown voltage of this device is 2.7V and the second breakdown current is 4.6A. The first breakdown voltage of this device is low enough to provide the required ESD protection in 90nm technology. It should be noted that our simulations predicts a less than 50fF capacitance for this device.

III. High Speed Driver with ESD Protection

This DSCR is used to design an ESD protected high speed driver. The driver is designed for 8.5Gbps data rate in 90nm technology. In order to study the impact of ESD protection device on circuit performance, two identical drivers were designed in the test chip. One driver is designed without ESD protection and the other driver is designed with DSCR ESD protection. Measurements on the test chip are done in two steps: In the first step, performance of the driver with ESD protection is compared with performance of the driver without ESD protection. In the next step ESD protection level of the driver is evaluated.

A. Performance of the driver

Performance of the driver is evaluated by its output swing, rise time and jitter. A pseudo random signal is applied to the driver using a pattern generator. Fig. 5 shows the measured eye diagram of the single ended output of the driver with and without ESD protection for 1.06Gbps data rate.

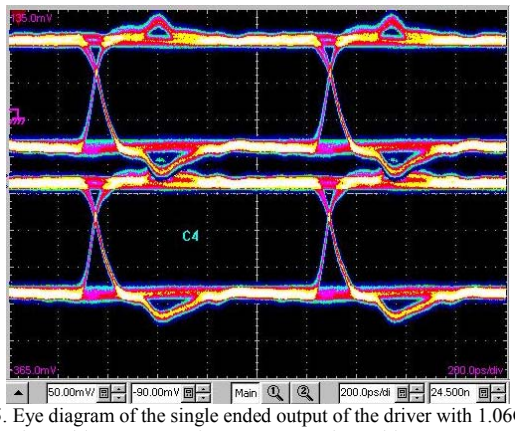


Fig. 5. Eye diagram of the single ended output of the driver with 1.06Gbps: Top: Driver with ESD protection - Bottom: Driver without ESD protection

The eye diagram on the top belongs to the driver with ESD protection and the eye diagram at the bottom belongs to the driver without ESD protection. It can be seen that the difference between two drivers is very small. RMS jitter of the driver without and with ESD protection are 2.25ps and 2.28ps respectively.

In the next step, data rate is increased to 5Gbps. Fig. 6 shows the eye diagram of the single ended output of the driver with and without ESD protection for this data rate.

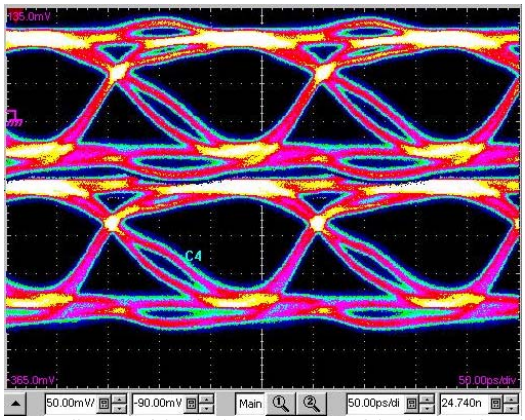


Fig. 6. Eye diagram of the single ended output of the driver with 5Gbps: Top: Driver with ESD protection – Bottom: Driver without ESD protection

The eye diagram on the top belongs to the driver with ESD protection and the eye diagram at the bottom belongs to the driver without ESD protection. Again, the difference between two drivers is negligible. RMS jitter of the driver without and with ESD protection are 2.65ps and 2.75ps, respectively.

Finally, data rate is increased to 8.5Gbps. Eye diagram of the two drivers are shown in Fig. 7.

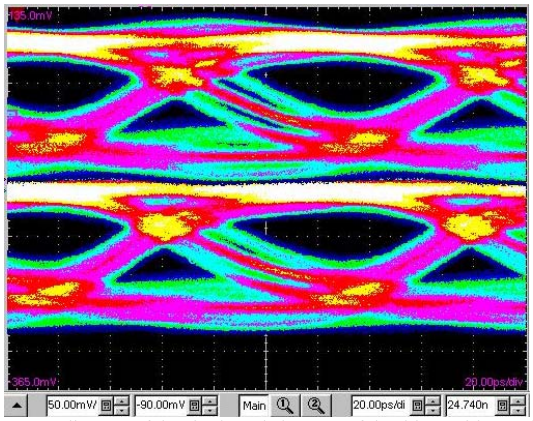


Fig. 7. Eye diagram of the single ended output of the driver with 8.5Gbps: Top: Driver with ESD protection – Bottom: Driver without ESD protection

Again, the eye diagram on the top belongs to the driver with ESD protection and the eye diagram at the bottom belongs to the driver without ESD protection. It can be seen that even for 8.5Gbps data rate the difference between two drivers is very small. RMS jitter of the driver without and with ESD protection are 4.27ps and 4.35ps respectively.

Table I summarizes performance of the driver with and without ESD protection for 1.06Gbps, 5Gbps and 8.5Gbps data rates. It can be seen that degradation in jitter of the driver with this ESD protection is less than 4%.

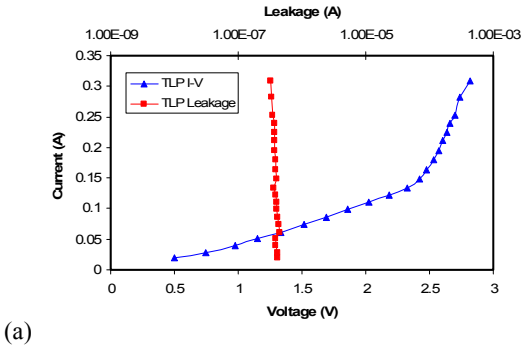
TABLE I: COMPARING JITTER OF THE DRIVER WITH AND WITHOUT ESD PROTECTION FOR DIFFERENT DATA RATES

RMS Jitter	1.06 Gbps	5 Gbps	8.5 Gbps
No ESD	2.25 ps	2.65 ps	4.27 ps
With ESD	2.28 ps	2.75 ps	4.35 ps

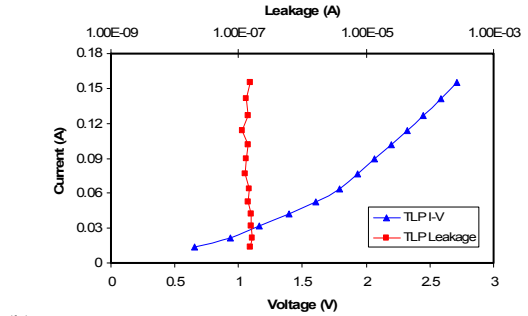
B. ESD Protection Level of the Driver

In the next step ESD protection level of the driver is evaluated. The driver is stressed in few steps, while performance of the driver is evaluated after each stress. As we didn't have access to an HBM tester, we used our TLP tester for this purpose. In order to find the protection level with reasonable accuracy, we increased maximum current of the TLP test in several steps.

In the first step, we stressed pad with respect to V_{DD} and V_{SS} up to 0.3A and 0.15A respectively. Fig. 8 shows TLP results for this step. After the first stress performance of the driver is tested at 1.06Gbps, 5Gbps and 8.5Gbps data rates. We saw that the driver is working properly and jitter of the driver at 1.06Gbps is 2.04ps, at 5Gbps is 2.75ps and at 8.5Gbps is 4.37ps.



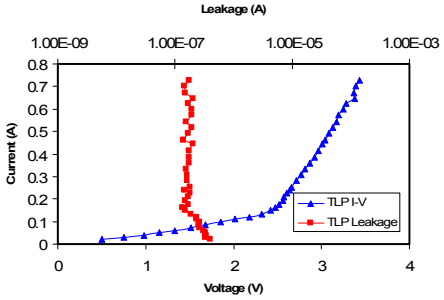
(a)



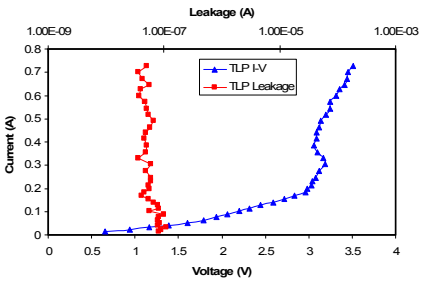
(b)

Fig. 8. Stressing the driver: first step (a) pad wrt V_{DD} (b) pad wrt V_{SS}

In the second step, we increased the TLP current and stressed the pad with respect to V_{DD} and V_{SS} to 0.72A. This current is approximately equivalent to 1.1kV HBM. Fig. 9 shows TLP measurement results for this step. Now, performance of the driver is measured after the second stress. Again the driver is still working properly and jitter of driver after the second stress becomes 2.73ps at 5Gbps data rate and 4.37ps at 8.5Gbps data rate.



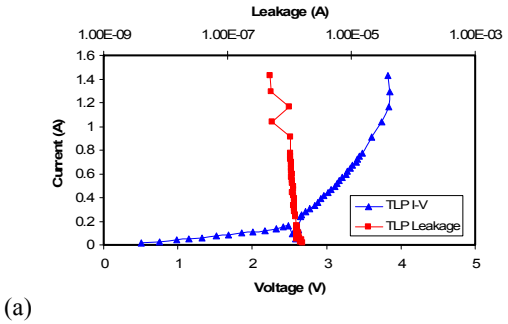
(a)



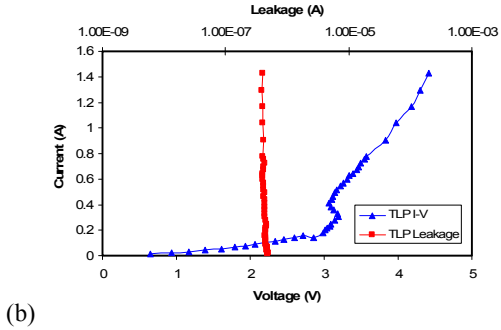
(b)

Fig. 9. Stressing the driver: second step (a) pad wrt V_{DD} (b) pad wrt V_{SS}

In the third step, we further increased TLP current and stressed the pad with respect to V_{DD} and V_{SS} up to 1.4A. This current is approximately equivalent to 2.1kV HBM. Fig. 10 shows TLP measurement results for this step. Next, performance of the driver after the third stress is measured. Jitter of the driver is 2.2ps at 1.06Gbps, 3ps at 5Gbps and 4.09ps at 8.5Gbps.



(a)



(b)

Fig. 10. Stressing the driver: third step (a) pad wrt V_{DD} (b) pad wrt V_{SS}

In the fourth step, we further stressed the driver. However, as we started stressing the pad with respect to V_{DD} we observed a failure in the driver. Fig. 11 shows TLP measurement results for this step. It can be seen that a failure is observed after 1.82A. After this step, driver is failed and the output of the driver is remained constant. Based on TLP results of Fig 11 we can estimate that failure current of the driver is around 1.8A, which can be estimated to be 2.7kV.

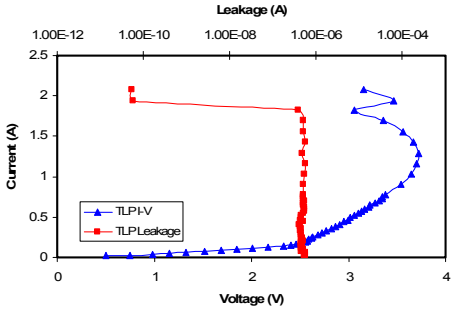


Fig. 11. Stressing the driver: fourth step: pad wrt VDD

It can be seen that using DSCR the driver is protected to over 2kV HBM in 90nm technology. At the same time, the ESD protection device has very small impact on rise time, output swing and jitter (less than 4%) of the driver in data rates as high as 8.5Gbps.

Table II summarizes results of the ESD protection level test. In this table an estimate of the HBM protection level after each TLP test is shown along with jitter of the driver after each TLP test.

TABLE II: SUMMARY OF ESD PROTECTION LEVEL TEST

	I_{TLP}	HBM	RMS Jitter after stress		
			1.06Gbps	5Gbps	8.5Gbps
step 1	0.3A	0.45kV	2.04ps	2.75ps	4.37ps
step 2	0.7A	1.1kV	-	2.73ps	4.37ps
step 3	1.4A	2.1kV	2.2ps	3ps	4.09ps
step 4	2.1A	3.1kV	failed	failed	failed

Based on the results of tables I and II using DSCR as ESD protection device allowed us to protect a high speed driver up to 2.7kV while having negligible impact on performance in data rates as high as 8.5Gbps.

IV. CONCLUSION

In this paper we designed an ESD protection for a high frequency CML driver. ESD protection is provided using darlington-based SCR (DSCR). This device offers very high ESD protection level per unit area. In order to do a complete comparison, we fabricated two CML drivers; one with ESD protection and one without ESD protection in 90nm CMOS technology. The drivers are tested at 1.06Gbps, 5Gbps and 8.5Gbps data rates. Measurement results show that this ESD device increases jitter of the driver by less than 4% in 8.5Gbps data rate. At the same time, TLP measurements show that the driver has a protection level as high as 2.7kV HBM.

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