A LEAKAGE TOLERANT ENERGY EFFICIENT WIDE DOMINO CIRCUIT TECHNIQUE

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ABSTRACT

Deep submicron noise, especially leakage current, greatly impacts the performance of wide dynamic gates. Quite often, energy is traded off for increased leakage tolerance. In this paper, a leakage tolerant energy efficient wide domino gate is presented. The proposed technique achieves faster evaluation by splitting the wide gate into two sections and consequently slashing the capacitance of the dynamic node by half. Using the new technique, the same level of leakage tolerance can be achieved with around 12% and 28% reduction in energy for 16-input and 32-input OR gates, respectively, compared to the conventional technique.

1. INTRODUCTION

Technology scaling has paved the way for cramming more transistors on a single chip and improving the performance of the ever growing VLSI systems. However, technology feature downsizing has raised several concerns that have to be carefully taken into consideration. Noise immunity is one important concern in deep submicron (DSM) designs. The increasing leakage current, large process variations, low supply voltages, high clock frequencies, crosstalk, and many other DSM noise sources, all contribute to a degradation in noise immunity.

As technology feature size is shrunk, supply voltage has to be reduced in order to keep a constant electric field inside the device. With constant field scaling, maximum device performance for each technology generation can be achieved while maintaining adequate device reliability [1]. However, the resultant degradation in performance due to supply voltage scaling often forces designers to reduce threshold voltage of the device to meet performance goals. Threshold voltage reduction severely degrades noise immunity for DSM VLSIs due to the exponential increase in subthreshold current in low threshold devices. Subthreshold leakage power is expected to increase by a factor of 5× each technology generation [2]. Therefore, it is often a challenge to maintain leakage power within bounds while achieving a certain performance target. This challenge is quite evident in the design of dynamic gates. The high performance advantage of dynamic logic is often traded off for improved noise immunity and leakage tolerance.

2. LEAKAGE TOLERANT WIDE DOMINO LOGIC

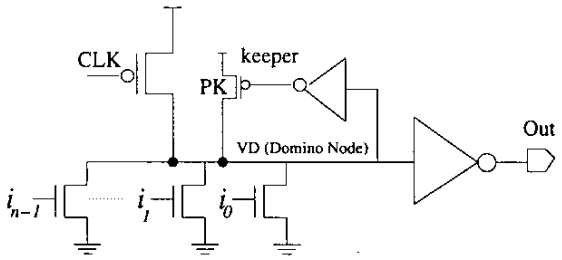

Figure 1: Conventional Wide Fan-In Domino n-input OR gate.

Dynamic logic is often deployed in speed critical paths of high performance systems where static logic fails to meet performance targets. Dynamic gates typically provide 30% delay reduction over static logic [2]. The use of wide fan-in dynamic logic such as domino circuits results in simple and fast structures at the expense of reduced noise margin. Figure 1 shows a conventional n-input wide domino gate. In this configuration, the pulldown NMOS devices are all low threshold (LVT) while all other devices are high threshold (HVT) to minimize leakage current. The utilization of dual threshold technologies in the implementation of dynamic circuits was first reported in [3]. The dual threshold configuration is preferred since noise immunity degradation decreases from 60-70% in the all LVT implementation to 30-40% in the dual threshold implementation [4].

A footer transistor (connected between sources of the pulldown devices and ground) is often avoided to maximize performance as shown in Figure 1. Removing the footer transistor restricts the clock signal to arrive before data arrival to avoid DC conduction (when both the precharge and a pulldown device are conducting). However, charge leakage increases dramatically when the footer transistor is re-

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moved. In order to compensate for the charge loss during the evaluation phase when all input devices are OFF, a keeper transistor is utilized. Upsizing the keeper device in order to compensate for leakage current, however, results in a performance degradation to the extent that domino logic may fail to operate correctly if the keeper device becomes too large (a single pulldown device fails to discharge the dynamic node). Anders *et.al.* [5] predicted that upsizing the keeper device to compensate for increased charge leakage is going to render conventional domino to be nonfunctional around the 70 nm technology generation, increasing the demand for leakage tolerant domino circuit techniques.

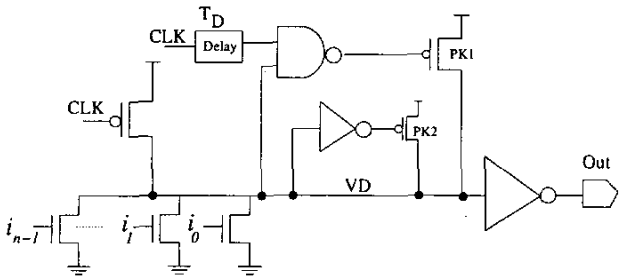

Figure 2: Conditional Keeper technique.

Recently, a conditional keeper (CKP) technique, shown in Figure 2, for noise tolerant wide fan in gates was proposed in [6, 7]. In this technique, the keeper device (PK) in conventional domino (see Figure 1) is divided into two smaller ones, $PK1$ and $PK2$. The keeper sizes are chosen such that $PK = PK1 + PK2$. Such sizing guarantees the same level of leakage tolerance as the conventional gate but yet allows for faster evaluation. The large keeper ($PK1$) in Figure 2 is deployed after a certain delay T_D, to prevent erroneous discharge of the dynamic node (VD) when all inputs remain LOW. The small keeper ($PK2$), however, remains ON to compensate for charge leakage until $PK1$ is activated. Deploying a larger portion of the keeper device after the delay T_D, depending upon the condition of the dynamic node, reduces contention power and hence enhances performance.

In this paper, a new leakage tolerant energy efficient split domino (SD) circuit is presented. The proposed technique addresses the classical trade off between energy dissipation and increased level of robustness and leakage tolerance. The SD gate mitigates the impact of leakage current in wide domino circuits by splitting the number of evaluation devices into two sections, and hence the name split domino. Such splitting results in a smaller dynamic node capacitance and consequently a faster evaluation. Reducing the number of transistors in each pulldown network also allows for the use of smaller keeper devices and hence a reduction in contention power. The SD technique is described in more details in the next section.

3. SPLIT DOMINO CIRCUIT TECHNIQUE

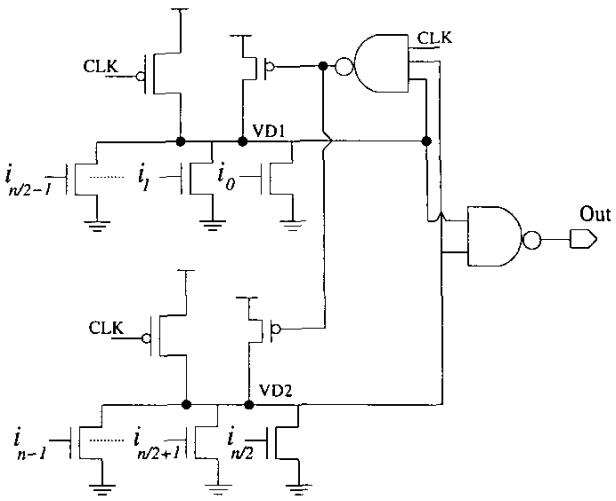

Figure 3: n-input split domino (SD) OR gate.

The SD gate shown in Figure 3 achieves higher performance of operation through splitting the pulldown devices into two networks. A logical 2-input NAND operation is then utilized to generate the output. The output inverter shown in Figures 1 and 2 is no longer required in the SD circuit. The keeper device is also split equally between the two networks. The main advantage of splitting the pulldown network into two sections, is the reduction of the dynamic node capacitance and consequently faster evaluation. Also, the large keeper transistor in the conventional case is replaced by two devices each of which is nearly half the original keeper size leading to less contention.

The operation of the SD circuit is described as follows. During precharge, CLK is LOW, the keeper devices are OFF and the output is LOW. At the onset of evaluation, the keeper devices remain OFF resulting in minimum contention. There are two different cases that need to be considered during the evaluation phase. When all inputs remain LOW and leakage current is at its maximum, the keeper devices controlled by the 3-input NAND gate are quickly activated to prevent the dynamic node from drooping and to keep output noise within the required limit. The 3-input NAND gate is skewed in such a way to allow for a very fast discharge of the keeper control signal in case all inputs remain LOW. The second case is when any input goes HIGH. In this case, the corresponding dynamic node discharges very quickly due to decreased dynamic node capacitance and nearly keeps the keeper devices in the OFF state and contention is therefore minimized. Figure 4 shows the different waveforms for both SD and conventional techniques. Clearly, the SD keeper is OFF at the onset of evaluation while the conventional keeper

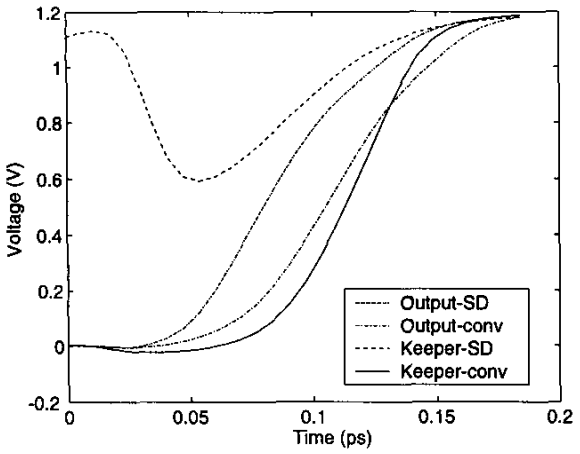

Figure 4: Keeper and output waveforms for SD and conventional 32-input OR gate

is ON. The keeper control signal can be seen to droop and quickly recovers to *VDD*, as shown in Figure 4, maintaining keeper devices virtually OFF.

The overhead of the SD gate represented in the 2-input and 3-input NAND gates results in a slight increase in power dissipation compared to the conventional case. The overhead can be fairly justified by the resultant performance improvement as discussed in detail below.

4. SIMULATION RESULTS AND COMPARISON

The SD circuit technique is compared to both conventional domino as a reference design and to the CKP technique. The comparison is based upon simulations of the three techniques for 16 and 32 -input OR gates implemented in 0.13μm dual threshold technology. Low threshold devices are used for the NMOS evaluation network. High threshold devices are used otherwise (e.g. keepers, inverters, etc.). The output load is set to a fan out of 4. The clock frequency is 2 GHz. The keeper sizing process is performed at worst case leakage condition, i.e. at temperature of 110°C, V_{DD} of 1.2 V, and the Fast-Fast process corner. The keeper transistors are sized such that the noise level at the output node does not exceed that at the inputs. The unity noise gain (UNG) as defined in [4] is used as the leakage tolerance criterion. As the DC noise level increases at the inputs, leakage current increases dramatically. A limitation of 12% of V_{DD} on DC input noise is set such that the input noise is always below the low threshold voltage for the pulldown devices. The performance metrics (delay, power, and power-delay-product (PDP)) are then measured at typical process corner, normal operating temperature (27°C), and zero DC input noise.

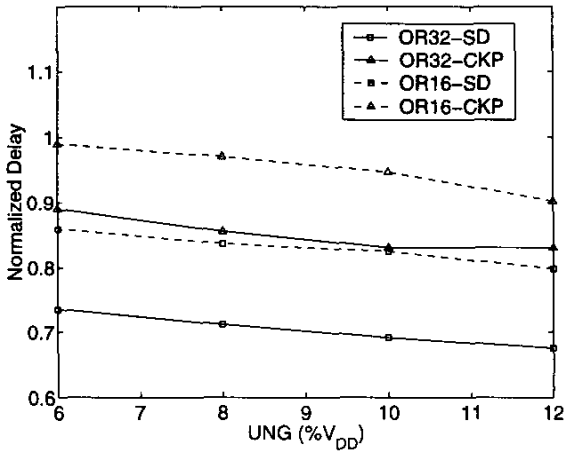

Figure 5: Delay of the SD and the CKP gates relative to the conventional technique.

Figure 5 shows the delay reduction of the SD technique compared to CKP technique both normalized to the delay of the corresponding conventional gates. The delay metric is defined here as the Data-to-Output delay. As mentioned earlier in section 2, data arrival time should be when or after the clock arrives. As the DC input noise level is increased, the performance improvement of the SD gate becomes evident. For the OR16 and OR32 and at a noise level of 12% UNG, the SD gate offers 20% and 32% performance improvement respectively over the corresponding conventional gate delay. The delay reduction is 7% and 12% compared to the CKP technique for the OR16 and OR32 respectively.

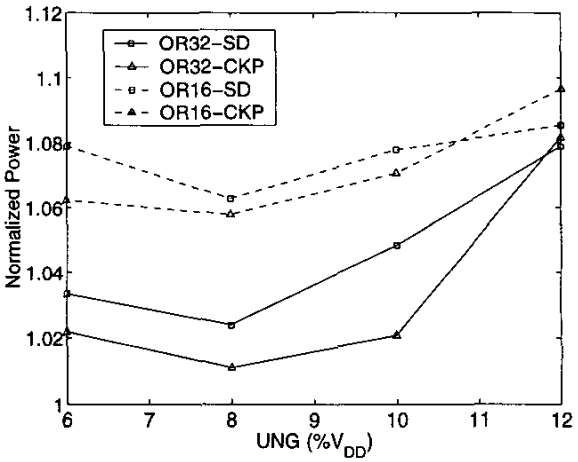

Figure 6: Power dissipation of the SD and the CKP gates relative to the conventional technique.

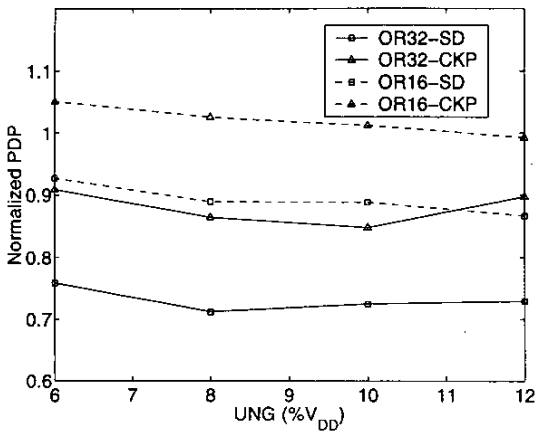

Figure 7: Power-Delay-Product (PDP) of the SD and the CKP gates relative to the conventional technique.

Table 1: Simulation results at 12% UNG

Gate	Technique	Delay	Power	PDP
OR16	Conventional	1	1	1
	CKP	0.9	1.1	1
	SD	0.8	1.08	**0.88**
OR32	Conventional	1	1	1
	CKP	0.84	1.08	0.9
	SD	0.68	1.08	**0.72**

Power dissipation of SD gates compared to that of CKP technique is shown in Figure 6. The results are normalized to power dissipation of the corresponding conventional gates. Power dissipation of SD gates are 6 to 8 % higher than that of the corresponding conventional gates due to the overhead of the two NAND gates used in the SD logic. Since keeper devices and the 3-input NAND gate have to be upsized to sustain higher leakage, power dissipation reaches a maximum at 12% UNG compared to conventional logic. Power dissipation of the CKP gates is slightly lower than that of the SD gates at low noise levels.

Figure 7 shows how the proposed technique is more energy (PDP) efficient compared to the other wide domino gates at high noise levels. The SD technique can achieve up to 28% PDP reduction for the OR32 case at 12% UNG compared to conventional. At the same noise level, PDP saving is 12% for the OR16 case. The CKP technique also results in energy savings of up to 10% in the OR32 case compared to conventional. The PDP savings of SD technique are 12% and 18% for OR16 and OR32 respectively compared to the CKP technique. A comparison between delay, power, and PDP at 12% UNG for OR16 and OR32 using the three different techniques is summarized in Table 1.

5. CONCLUSION

A leakage tolerant energy efficient split domino (SD) circuit technique for wide fan-in gates has been presented. The SD 32-input OR gate is 32% and 12% faster compared to the conventional and the conditional keeper counterparts respectively. The proposed technique offers 12% and 28% energy reduction for 16-input and 32-input OR gates, respectively, compared to conventional domino. Relative to the conditional keeper technique, the corresponding savings are 12% and 18% respectively. Energy savings are a result of the faster evaluation of the proposed technique due to the reduced dynamic node capacitance and reduced contention power.

Acknowledgment

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