Multi Giga Hertz Digital Test Challenges and Techniques

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1. Introduction

The clock frequency of high performance VLSIs has exceeded 2GHz. Over the years, aggressive scaling of CMOS process technology has resulted in a 30% annual performance improvement for digital circuits. However, tester speed has improved by only 12% every year. Figure 1 shows data from the International Technology Roadmap for Semiconductors (ITRS'01) [1], for device under test period (DUT), automatic test equipment (ATE), and overall device accuracy requirements. As it is apparent from the figure, at-speed testing is becoming increasingly difficult. Thus, tester inaccuracy, shrinking geometries, and higher device speed are expected to compromise IC yield and quality.

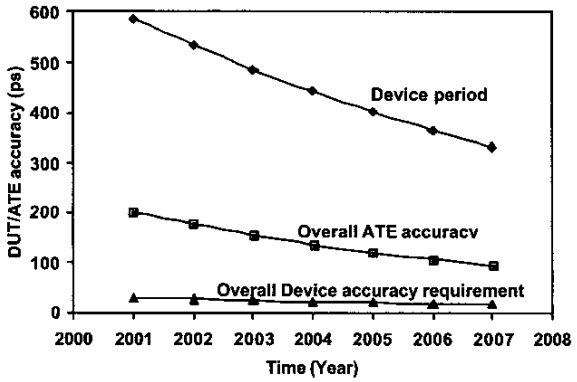

Figure 1: ITRS'01 projections for DUT and ATE performances

2. High-Performance Circuit Testing: Background

Techniques used to detect delay defects can broadly be categorized as indirect (correlation based) methods and direct test methods. A methodology proposed by Hao and McClusky [2], is based on the Very Low Voltage Test (VLV) technique where ICs are performance tested at reduced V_{dd}. It was observed that delay faults were more noticeable at a lower V_{dd} and hence easier to detect. However, there has been an increased focus on direct test techniques. These methods are based on the incorporation of additional DFT structures and the creation of a low frequency TEST mode. The basic idea is to include an externally controlled, quantifiable delay to enable slow-speed testing. Such techniques are applicable to combinational circuits bounded by flip-flips (F/Fs) [3,4]. The F/Fs are designed to have large D-Q delay (T_{prop}) in the TEST mode. Therefore, in the TEST mode, the test clock frequency can be reduced while the combinational logic is tested for specified delay.

3. DFT in Dynamic Circuits

Dynamic CMOS circuit implementations offer higher performance over their static counterparts. Therefore, building blocks of high performance ICs, such as adders, ALUs and multipliers are often implemented using dynamic circuits. An implementation of the proposed DFT technique is illustrated in Figure 2. This dynamic circuit has two modes of operation: 1) NORMAL, and 2) TEST. In the NORMAL mode of operation, input signal Test_Clk is a dc signal connected to V_{dd}. As a result, transistor N4 is always ON allowing normal operation of the circuit. However, in the TEST mode, the Test_Clk input signal is inverted and phase-shifted with respect to the Clk signal, as shown in the timing diagram. The signals Clk and Test_Clk create an "evaluation window" equal to the phase shift between the two signals. It is only during this time that both N3 and N4 are ON allowing logic evaluation.

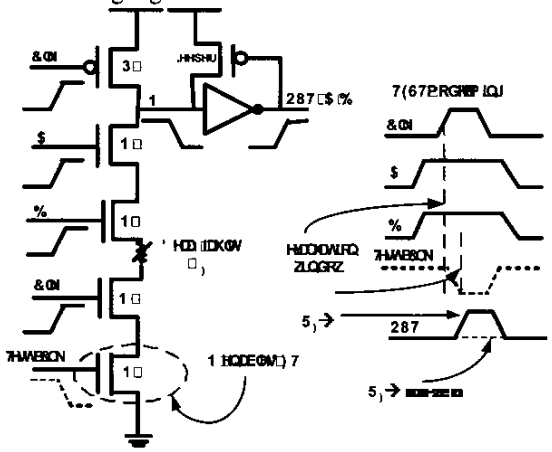

Figure 2: Dynamic gate with DFT (TEST mode operation)

References

[1] Semiconductor Industry Associations, "International Technology Roadmap for Semiconductors, 2001Edition", 2001.

[2] H. Hao, and E.J. Mc Cluskey, "Very-Low Voltage Testing for Weak CMOS Logic ICs", *ITC93*, pp. 275-284.

[3] V. D. Agrawal, T. J. Chakraborty, "High-Performance Circuit Testing with Slow-Speed Tester", ITC95, pp. 302-310.

[3] M. Shashaani, and M. Sachdev, "A DFT Technique for High Performance Circuit Testing", *ITC99*, pp. 267-285.

[4] B. Chatterjee, M. Sachdev, A. Keshavarzi, "A DFT Technique for Low Frequency Delay Fault Testing in High Performance Digital Circuits, *ITC02*.

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