Multiple-Parameter CMOS IC Testing with Increased Sensitivity for I_{DDQ}

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ABSTRACT

Technology scaling challenges the effectiveness of current-based test techniques such as I_{DDQ}. Furthermore, existing leakage reduction techniques are not as effective in aggressively scaled technologies. We exploited intrinsic dependencies of transistor and circuit *leakage* on *clock frequency, temperature,* and *reverse body bias (RBB)* to discriminate fast ICs from defective ones. Transistor and circuit parameters were measured and correlated to demonstrate leakage-based testing solutions with improved sensitivity. We used a test IC with available body terminals for our experimental measurements. Our data suggest adopting a sensitive multiple-parameter test solution. For high performance IC applications, we propose a new test technique, I_{DDQ} versus F_{MAX} (maximum operating frequency), in conjunction with using temperature (or RBB) to improve the defect detection sensitivity. For cost sensitive applications, I_{DDQ} versus temperature test can be deployed. Our data show that temperature (cooling from 110 °C to room) improved sensitivity of I_{DDQ} versus F_{MAX} two-parameter test by more than an order of magnitude (13.8X). The sensitivity can also be tuned by proper selection of a temperature range to match a required DPM level.

1. Introduction

There is significant research that describes the impact of technology scaling on various aspects of VLSI testing [1-7]. Our ability to perform leakage-based tests is threatened by elevated transistor leakage in scaled process technologies. This trend challenges conventional I_{DDQ} test methods. Recently, several methods were reported to sustain the effectiveness of I_{DDQ} testing for sub-0.25 μm technologies. These methods include reverse body bias (RBB), current signatures, delta I_{DDQ} testing, and transient current testing [2,3,9,16-20]. By applying a reverse body bias, a low leakage I_{DDQ} test mode is created [2,3]. Gattiker et al. suggested sorting of I_{DDQ} test vectors in ascending order. An abrupt discontinuity in the current level is an indication of a defect [16]. Maxwell et al. demonstrated the effectiveness of current signatures with silicon data [17]. Thibeualt [18] and Miller [19] proposed delta I_{DDQ} test technique to uncover defects. Conceptually, delta I_{DDQ} technique is similar to that of current signatures where sudden elevation in current level is an indication of a defect. Some researchers suggested utilization of transient current test techniques [9,20]. The search for new test strategies is motivated primarily by the increasing adverse device leakage trends.

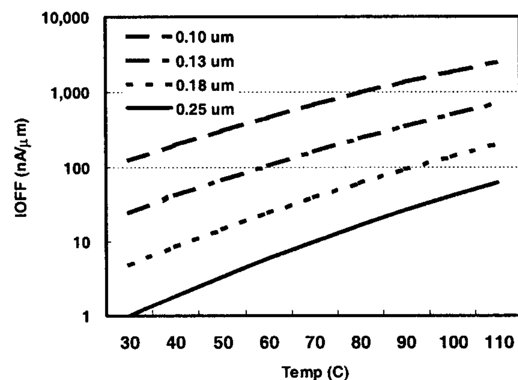

Fig. 1: Projected transistor off-state current (I_{OFF}) [10].

We will illustrate one aspect of the problem of elevated intrinsic leakage by estimating the subthreshold transistor leakage component and computing leakage of future chips [10]. We start with the 0.25 μm technology [11] and project subthreshold leakage currents for 0.18 μm, 0.13 μm, and 0.1 μm technologies. Subthreshold leakage is not the only component of a transistor leakage, but is increasingly the dominant component [3,4]. A typical 0.25 μm transistor with V_T of 450 mV has I_{OFF} of about 1na/μm at 30 °C (room temperature). If subthreshold slopes are 80 and 100 mV/decade at 30 °C and 100 °C, and if V_T changes by 0.7 mV/°C and scales by 15% per generation, then I_{OFF} increases by 5X for each new technology generation [10].

Since I_{OFF} increases with temperature, it is important to consider leakage currents and leakage power as a function of temperature. Fig. 1 shows I_{OFF} projected for the four different technologies as a function of temperature [10]. I_{OFF} at room temperature increases from 1 nA/μm for 0.25 μm technology to larger than 100 nA/μm for a 0.10 μm

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technology. At 110 °C, these values correspond to 100 nA/μm and greater than 1 μA/μm. We may use these projected I_{OFF} values to estimate the active leakage of a 15 mm^2 die integrated circuit. The total transistor width on the die is expected to increase by ~50% for each technology generation. Hence, the total leakage current increases by ~7.5X.

Our approach to testing intrinsically leaky integrated circuits is different, yet complementary to other state-of-the-art solutions. We correlate intrinsic transistor device and circuit parameters to develop multiple parameter test solutions. An example correlates I_{DDQ} and F_{MAX} while using a third parameter such as temperature and/or reverse body bias (RBB) to enhance test sensitivity. This test method saves fast intrinsically leaky ICs while discriminating against defective ones. Defect detection capability of this method is more enhanced by two-temperature testing.

2. Leakage versus Frequency Characterization

Our test solution is critically dependent on characterizing and quantifying change in I_{DDQ} as a function of change in F_{MAX}, where I_{DDQ} and F_{MAX} are leakage and chip speed respectively. Keshavarzi et al., correlated leakage current (I_{DDQ}) of a 32-bit microprocessor to its maximum clock frequency (F_{MAX}) in a 0.35 μm technology [3]. We reexamined this relation for a 0.18 μm technology on a test chip circuit. This test IC provided more flexibility and degrees of freedom such as availability of body terminals to explore the fundamental concepts prior to actual product specific test development. The roots of leakage to frequency correlation exist in device physics and for a circuit designed on a given process technology, one can establish and characterize such a relationship [3].

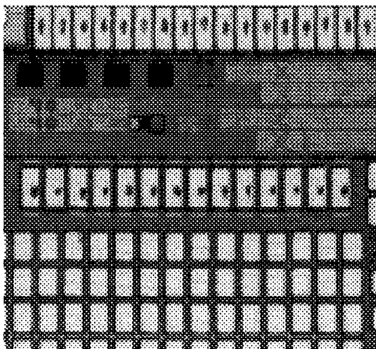

Fig.2: Die photograph of the test chip.

We used our high-performance test chip containing 20,000 transistors to study the relationships between leakage, RBB, F_{MAX}, V_T, channel length (L), power supply voltage, and temperature for various technologies. Fig. 2 is a photo of the test chip showing multiple circuit blocks. We used a ring oscillator (RO) and a delay chain circuit for our studies in this paper. The body (well and substrate) terminals of these devices on the ICs were externally available for RBB application. RBB is a potential between the body and source terminal that reverse biases the body to source *pn* junction. The body of the *p*MOS (*p*-channel) device is located in the *n*-well and the body of the *n*MOS (*n*-channel) device is linked to the *p*-well and to the *p*-substrate. The technology was a twin-well CMOS process with the *p*-well inside the *p*-substrate. All *n*-channel transistor bodies have the same body voltage when a bias is put on the substrate.

Fig. 3 is a semi-log plot of log I_{DDQ} versus F_{MAX} without applying any RBB (zero body bias or RBB = 0 V) in our 0.18 μm technology. This semi-log curve plots the relationship between test chip ring oscillator (RO) normalized I_{DDQ} leakage and its normalized maximum operational frequency. Normalization is with respect to the lowest chip leakage and frequency (Fig. 3). Data came from more than 100 ICs from two wafers where each data point in Fig. 3 represents a die.

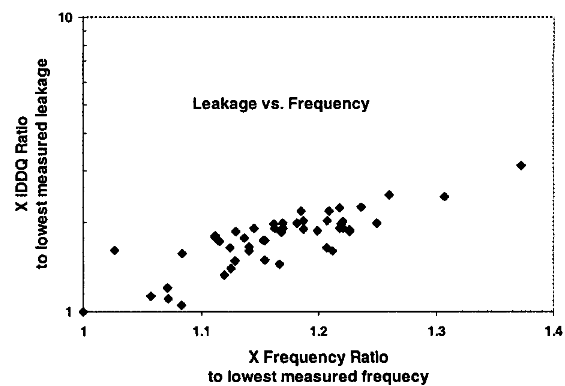

Fig. 3: Normalized RO circuit frequency versus I_{DDQ} leakage at room temperature without any applied body bias.

The data indicate a linear relationship between log I_{DDQ} and RO frequency. This linear dependency is observed across the range of natural variation in transistor and circuit parameters in our ICs. No parameter such as V_T or L was intentionally skewed, so we are seeing natural range of parameter variation in our experiment. For this

collection of IC's, a 35% increase in CUT frequency (1.35X change) increased I_{DDQ} by 4.1X at room temperature. Alternatively, the CUT that was faster by 35% also had 4.1X higher leakage. Slower (faster) circuits have lower (higher) leakage. This fundamental relationship between IC's maximum operating frequency and its aggregate leakage is essential to the concept of two-parameter testing.

3. Multiple-Parameter Testing

We will explain a universal multi-parameter test solution based on the intrinsic leakage to frequency correlation. Multiple-parameter testing correlates a parameter such as circuit leakage against another parameter such as circuit's speed (operating frequency) or temperature and uses a third variable for example RBB or temperature to enhance the test sensitivity. Multiple-parameter testing is a low cost alternative solution for discriminating fast intrinsically leaky ICs from defective ones. It is a method to extract a defect signal from a variable and noisy leakage to frequency dependence.

During characterization and test development, leakage (I_{DDQ}) and maximum operating frequency (F_{MAX}) are measured and plotted against each other for many ICs. A trend line is superimposed on the measured data in Fig. 4 and an arbitrary limit line is shown. The leakage limit will be frequency dependent and can be determined by statistical analysis. The dependency trend line defines the shape of a limit line (Fig. 4). Then, we may make a decision on a measured IC depending on where it lies on Fig. 4 with respect to the proposed adjustable frequency (speed) dependent leakage limit line. If for a given frequency, an IC has substantially higher leakage than forecast by the intrinsic dependency (similar to the circled IC in Fig. 4), then the IC is classified as defective. However, the IC identified in Fig. 4 is a questionable IC because its leakage is not substantially higher. This IC is a candidate for further examination.

Thus, the two-parameter test limit should distinguish fast and slow die from those that are defective. The test improves signal to noise ratio for defect detection for high performance ICs with high background (intrinsic) leakage levels. If the decision is doubtful, we may seek other variables to enhance the defect discrimination sensitivity of this test. The frequency dependent leakage limit must be established a priori. Then each IC's speed and leakage is measured as usual (a single point). This single IC data will be compared against the relationship (frequency-dependent limit). No parameter sweep is necessary. We emphasize that any two or any number of parameters can be used for multiple-parameter test method.

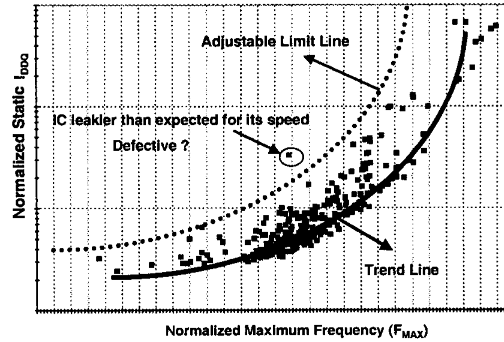

Fig. 4: Microprocessor I_{DDQ} versus F_{MAX} with trend line and test limit [3].

A more basic multi-parameter microprocessor test, the two-parameter test, was originally proposed in [3] by measuring I_{DDQ} and F_{MAX} parameters and comparing them against a pre-characterized, already-established I_{DDQ} versus F_{MAX} relation curve (similar to Figs. 3 and 4). It should be clarified that the channel length of ICs in Fig. 4 was intentionally skewed smaller during fabrication to increase the leakage. Consequently, data in Fig. 4 have a much broader range than data in Fig. 3 that only consists of natural range in parameter variation without actually modulating any parameter. The curve in Fig. 4 would have been linear (in a semi-log plot) if we had plotted it for a more limited range in frequency, if we had not skewed the channel length or if we had only considered natural parameter variation.

4. Sensitivity Gain with RBB and Temperature

Since the leakage to frequency correlation relation is intrinsic, then varying transistor, circuit, and environment parameters such as temperature and body bias cause predictable changes in this dependency. We used this concept to improve sensitivity of the two-parameter test solution. Reverse body bias (RBB) lowers IC leakage and reduces its performance/speed [3,4]. Lower temperature increases the transistor switching speed and reduces its leakage current. In this section, we show that applying temperature and/or RBB as a third parameter improves the signal to noise ratio of our proposed I_{DDQ} versus F_{MAX} test.

Fig. 5 plots normalized RO (CUT) frequency change against its leakage as the reverse body bias voltage, V_{bs},

was varied from 0 V to 1.5 V in steps of 250 mV for two different temperatures. We used absolute values of the RBB as we applied the RBB to both *n*MOS and *p*MOS transistors in our RO CUT. Data in Fig. 5 are from a typical RO die. The lower curve is at room temperature (27.7 °C). As temperature rose to 110 °C, the leakage increased by about 30-40X; however, the frequency reduced. Curves at both temperatures show the reduced leakage as RBB magnitude increases (going from right to the left along each curve). Moving from right to left along the T=27.7 °C curve, we see only a modest 2X reduction in leakage by applying 0.5 V of RBB (second data point with a square around it in Fig. 5). Furthermore, 0.5 V of RBB appears to be an optimum value as the leakage reduction saturated beyond this point.

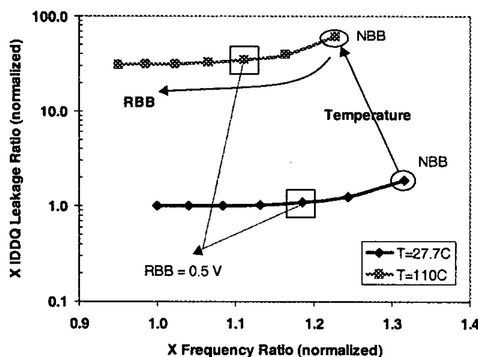

Fig. 5: A typical RO leakage versus frequency at room temperature (27.7 °C) and at hot (110 °C) with varying reverse body bias from 0 to 1.5 V in steps of 250 mV.

Fig. 5 shows that lowering the temperature from 110 °C to 27.7 °C changed the CUT leakage much more than varying RBB from no bias to effectively 1.5 V. Consequently, temperature can enhance the two-parameter test sensitivity. RBB provides minimal leakage reduction and hence has a limited application for this 0.18µm technology [14].

Despite RBB's limited effectiveness in reducing leakage of scaled technologies, we studied its use as a third variable to improve the sensitivity of two-parameter test for defect discrimination. RBB alters the fundamental I_{DDQ} versus F_{MAX} relationship and statistics. Fig. 6 shows the shift in RO leakage and frequency by applying 0.5 V of RBB to ICs of Fig. 3. The arrows shown in Fig. 6 pictorially represent the direction of the shift in speed and leakage as a result of applying reverse body bias. On average for all ICs tested, we quantified that with 0.5 V of RBB leakage reduced by 1.8X while speed reduced by 10% (1.1X).

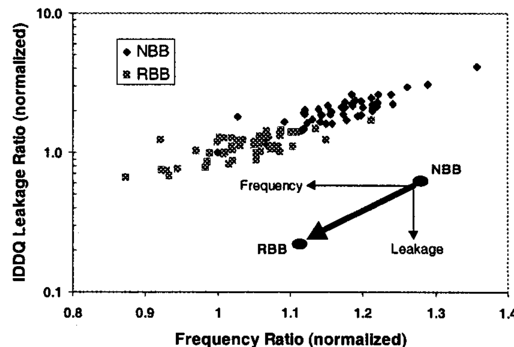

Fig. 6: IC leakage versus frequency with and without reverse body bias of 0.5 V at room temperature (27.7 °C).

Next we reanalyzed the data in Fig. 6 by only considering the leakage reduction from applying a reverse body bias voltage (Fig. 7). If we ignore the frequency shift (slow-down) associated with RBB, we can plot the IC's leakage before and after applying reverse body bias as a function of the IC's original frequency with RBB = 0 V. Thus, the frequency identifies each die or IC allowing for tracking of leakage with applying reverse body bias. Fig. 7 shows data plotted in this manner (same data set as Fig. 6). The vertically paired points are the two bias conditions results for the same IC. The arrow in Fig. 7 shows the direction of leakage reduction with RBB.

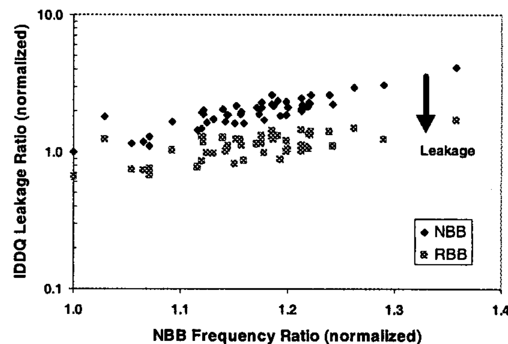

Fig. 7: IC leakage with and without reverse body bias of 0.5 V versus IC's original frequency (i.e. no body bias) at room temperature (27.7 °C).

Fig. 7 more clearly shows that reverse body bias reduces IC leakage creating a new leakage versus frequency correlation curve separated from the original dependency

with a different slope. Physically this shift is caused by the increase in V_T due to applied reverse body bias. This suggests that leakage of defect-free intrinsically leaky ICs can be changed in a controlled manner by body bias. However, if an IC is defective and the defect creates a parallel leakage path between V_{DD} and V_{SS}, the shift in current will be different from the intrinsic physics-based behavior. This property can improve the sensitivity of the proposed two-parameter testing.

We emulated a small defect by adding a large 4 MΩ resistor between V_{DD} and V_{SS} of two of our ICs. For V_{DD} = 1 V, this resistor gave 25 nA of leakage path in parallel to our IC under test (CUT). Fig. 7 is re-plotted in Fig. 8 with two ICs having 4 MΩ rail bridge defects. The 4 MΩ resistance value was selected due to relatively low leakage in our 20,000 transistor test chip and it provided a defect with very low impact on signal disturbance. Our objective was to show how even subtle defects can be screened. Gross defects are otherwise detectable by the adjustable limit concept (a frequency-dependent leakage limit) in the original two-parameter testing. One does not need to use a third variable to improve the test sensitivity for catching gross defects.

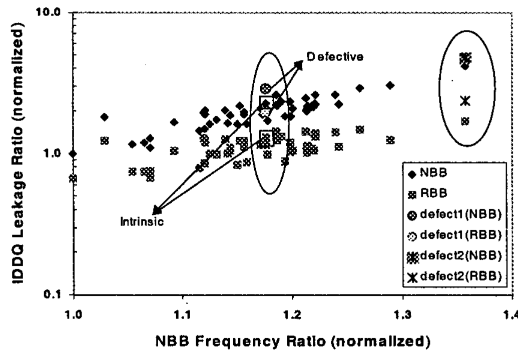

Fig. 8: Defective and defect-free IC leakage with and without reverse body bias versus IC's original measured frequency (with no applied body bias).

The emulated defective IC in the middle of Fig. 8 shows that the defective IC has slightly higher leakage than the original defect-free IC (1.25X or 25% more due to extra leakage between V_{DD} and V_{SS}). Intrinsically, the median leakage of the ICs under our study reduced by 1.8X when 0.5 V or RBB is applied. The "emulated" defective IC's leakage reduced by 1.45X. Our data show that 0.5 V of RBB still keeps the leakage of this defective IC inside the population of leakage versus frequency behavior of ICs without any body bias. Hence, RBB can distinguish such a defective IC. Fig. 8 shows that defective ICs do not follow the same intrinsic leakage versus frequency slope. Furthermore, The separation of the leakage of a questionable defective IC from intrinsic leakage of the same IC by RBB translates into a better test sensitivity. This is remarkable considering the minor impact of the 4 MΩ rail to rail bridge defect. Often resistive defects can result in subtle delay failures, depending upon whether defect is in series path like a via or in parallel like a signal to rail bridge, that may be isolated by multiple-parameter testing. RBB improves the signal to noise ratio for defect detection; however, it has a limited range. RBB was not able to fully separate out the leakage versus frequency curves.

Additionally, we emphasize that RBB leakage reduction and its application in improving test sensitivity is diminishing as the technology scales [12-13]. One limitation of RBB comes from GIDL and junction leakage [12-13] primarily the tunneling component mechanisms. Another limitation is degradation of body effect due to short channel effects. This means that body potential does not modulate V_T substantially in scaled technologies. Our 0.18 μm technology results suggest a different conclusion than reported for an older 0.35 μm process technology [3]. Reverse body bias lowered leakage and hence I_{DDQ} by three orders of magnitude in a 0.35 μm technology [3]. However, recent data showed that the effectiveness of RBB to lower I_{OFF} decreases as technology scales. Keshavarzi et al., showed that RBB could only reduce leakage by less than a single order of magnitude for scaled 0.18 μm technology [12-13]. Technology parameters, particularly junctions, play a major role in RBB effectiveness [12-13].

We then looked at temperature as another parameter to improve test sensitivity. Fig. 9 plots leakage versus frequency of the same ICs as a function of two temperatures. The arrow in Fig. 9 shows the direction of leakage and speed change as we cool down the ICs. Fig. 10 plots the same data in Fig. 9, but ignores the frequency shift of changing the temperature. In other words, we plotted the change in leakage as a function of IC's original frequency at room temperature. It is apparent that temperature is more effective in modulating the leakage for our 0.18 μm technology than RBB. As we scale the technology, temperature may become more effective than RBB. For our technology, we could only approach ~2X leakage reduction on average for RBB (at the optimum body bias point of 0.5 V) as opposed to approximately ~32X by cooling (from hot to room) in order to apply these leakage modulations to test sensitivity enhancement. We did not purely rely on the magnitude of leakage reduction,

but we used it for sensitivity purposes in two-parameter test.

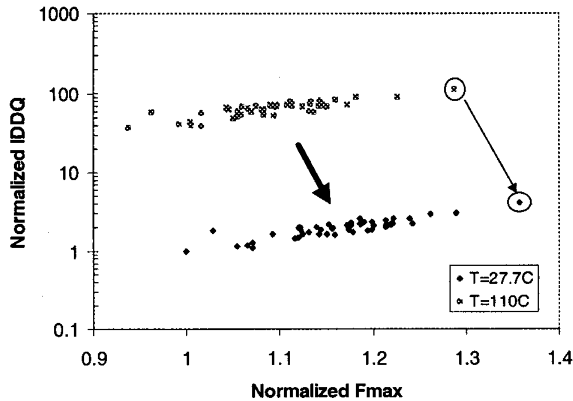

Fig. 9: IC leakage versus frequency at room temperature (27.7 °C) and at hot (110 °C) without any reverse body bias.

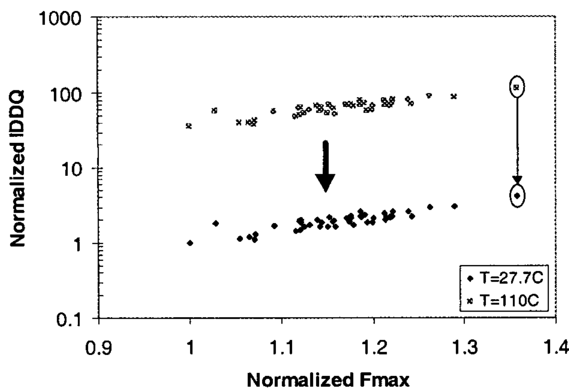

Fig. 10: IC leakage versus IC's original frequency (i.e. with no body bias at room temperature) for two different temperatures (27.7 °C and 110 °C).

We measured temperature dependence of our ICs for a wide range of temperature, from –50 °C to 110 °C in six steps. Intrinsic leakage versus frequency data shown in Fig. 11 suggest that we can change the leakage of our ICs by more than three orders of magnitude in this temperature range. We also see that ICs are slowing down as the temperature increases by a shift of the data to the left in Fig. 11. These data show that temperature is effective in improving the sensitivity of our proposed two-parameter test.

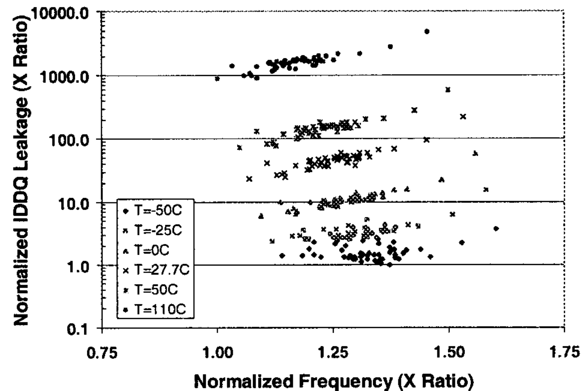

Fig. 11: IC leakage versus frequency for different temperatures without any reverse body bias.

We emulated a defective IC by adding a bridge 1 MΩ resistor between V_{DD} and V_{SS} (similar to the technique used for RBB analysis). Fig. 12 shows a good separation between intrinsic population of ICs at two temperatures studied for defect sensitivity improvement. No intrinsic data overlap (due to natural frequency versus leakage variation) occurred in frequency versus leakage data at two temperatures of 27.7 °C and 110 °C. Comparing of Fig. 12 to Fig. 8 shows once more that temperature is more effective.

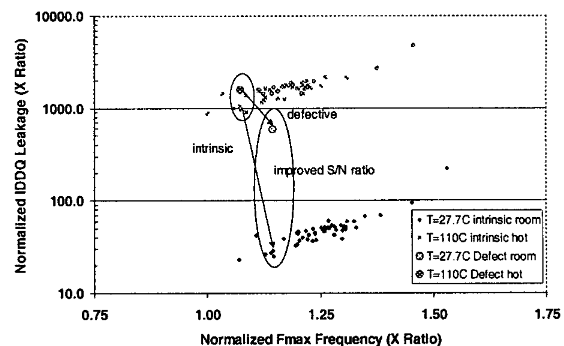

Fig. 12: Defect sensitivity improvement by temperature. Defective and defect-free IC leakage versus IC's measured frequency at two temperatures of 27.7 °C and 110 °C without any applied body bias.

The leakage of the original IC circled in Fig. 12 for our defect sensitivity study reduced intrinsically by 36X when temperature dropped from hot to room. When we added the defect to this IC, the leakage of this "emulated" defective IC shown in Fig. 12 increased by 1.6X due to the extra leakage path between V_{CC} and V_{SS}. This data point still belonged to the hot leakage versus frequency population plot making it a challenge to detect this defect purely by the adjustable limit concept.

In other words, two-parameter testing with the proposed adjustable frequency-dependent leakage limit lacked the necessary sensitivity to detect and isolate this defective IC. However, when the temperature was lowered, the leakage of this defective IC reduced by only a factor of 2.6X, keeping this defective IC outside of main population of frequency versus leakage behavior at lower (room) temperature. We quantified the gain in the test sensitivity by taking the ratio of intrinsic leakage reduction (36X) to the amount of leakage reduction for the defective IC (2.6X). The signal to noise ratio improved by more than an order of magnitude (36X/2.6X=13.8).

Fig. 12 shows that the defective IC's leakage at room temperature is still located at about the leakage versus frequency dependence distribution at hot. Consequently, a simple adjustable limit concept applied to this data point at room temperature can now detect this defect. Lowering temperature by 80 °C from hot to room provided an order of magnitude separation (approximately 40X versus 4X) between intrinsic and defect-induced amount of leakage reduction in the context of two-parameter testing. This is primarily why temperature improves sensitivity and signal to noise ratio for the two-parameter testing. Temperature in conjunction with the adjustable limit may detect more subtle defective ICs.

5. Leakage versus Temperature Two-Parameter Test Solution

I_{DDQ} may be combined with temperature for IC products or applications when F_{MAX} is not measured or is not relevant. An intrinsic two-parameter relationship between leakage and temperature can screen for defective ICs while considering the natural range of parameter variations. One may make two leakage (I_{DDQ}) measurements at two different temperatures. These are then mapped against a pre-characterized leakage versus temperature behavior. This is done for an IC product fabricated on a given process technology incorporating variation in temperature, frequency, and leakage. Fig. 13 shows non-defective IC's leakage as a function of temperature for a range of different temperatures from -50 °C to 110 °C. The spread in leakage data at each given temperature represents the natural spread in parameter variation. This variation is similar to the natural range of parameter variation observed in leakage versus frequency behavior (Fig. 3). This variation needs to be fully characterized in production worthy test solutions to select a proper temperature range.

Fig. 13 also complements our earlier conclusion by showing temperature is a good modulator of intrinsic leakage for our technology, over a range of our test chip frequencies and range of parameter variation. The key in selecting the temperatures for testing is to make sure that the two temperatures are separated enough for the parameter variation (spread in the data at a given temperature) not to overlap. For example, lowering temperature from 110 °C to 27 °C, reduces the mean intrinsic leakage by ~40X. And the natural spread in data won't overlap each other providing a means for defect detection sensitivity.

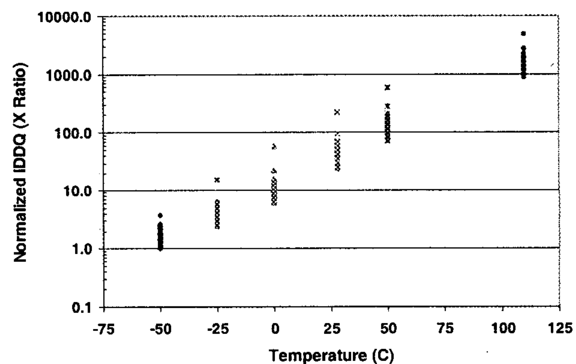

Fig. 13: IC leakage versus temperature for six different temperatures without any body bias.

We demonstrated the defect detection capability for I_{DDQ} versus temperature test using a defective IC (same defective IC used in Fig.12) to show how this test improves the signal to noise ratio. Fig. 14 shows that one can separate out a defective IC in a population of normal ICs at hot by lowering the temperature to room. The defective IC's leakage at room temperature is outside the natural range of leakage parameter variation at the same temperature. The defective IC's leakage reduced by 2.6X while it should have been lowered intrinsically by 36X, an order of magnitude larger. The lower we make the temperature, the better the separation resulting in a better signal to noise ratio. A wider temperature separation also allows for tolerating a wider range in the parameter variation. Furthermore, the sensitivity may be tuned to a desired level with a selection of a proper temperature range.

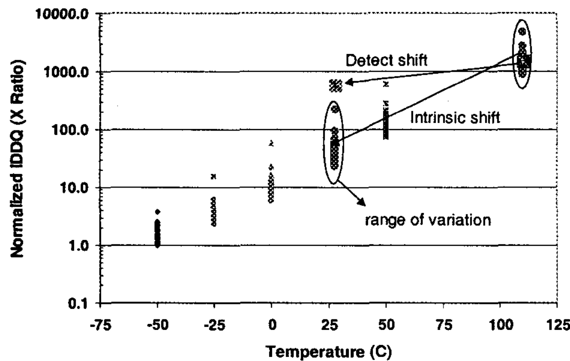

Fig. 14: IC defect detection for leakage versus temperature two-parameter test at two different temperatures (27.7 °C and 110 °C) without any body bias.

6. Discussions and Test Applications

Leakage reduction techniques by themselves (such as lowering temperature, lowering V_{DD}, applying RBB, chip segmentations, etc.) may not be sufficient for testing in future scaled technologies. To pursue average leakage reduction for all ICs, one needs to aggressively combine several of these techniques to maintain a reasonable efficiency. Furthermore, they add to the cost of an already expensive test process. For example very low temperature adds to the test cost and RBB adds to the design cost. Although we can use any leakage reduction we can get, we may have to look for other solutions for the problem of testing of ICs with elevated intrinsic leakage. The test proposed here views an IC's leakage (no matter how high) in the context of its maximum frequency (correlative). Consequently, it does not require an IC's average intrinsic leakage to be low making it a scalable test solution. It can also manage variability in leakage. Multiple-parameter testing is a low cost alternative for saving fast intrinsically leaky ICs while discriminating against defective ones. This test does not contradict any present I_{DDQ} test practices and measurement techniques. It actually complements all currently available techniques [2,3,9,16-20]. We defined two different test applications, one for the high performance IC market and one for low cost applications.

6.1 High Performance Products Test Applications

We proposed a two-parameter test solution based on the leakage to frequency relationship for high speed IC products fabricated on advanced process technologies. I_{DDQ} (at least in a simple form of a single vector I_{SB}) and F_{MAX} (maximum operating frequency) tests are performed for today's high performance ICs. I_{DDQ} is critical in measuring static power consumption of an IC to the specification (data sheet) at the very least, if not for defect screening. F_{MAX} is critical to speed bin the high performance ICs. Our primary multiple parameter test proposal utilized these two already measured parameters producing the I_{DDQ} versus F_{MAX} two-parameter test solution for high performance microprocessors. Adjustable frequency-dependent leakage limit and temperature (or RBB) enhanced this test's defect detection sensitivity.

This test can be inserted at the end of the test flow (not consuming any IC tester time) prior to inking defective ICs or throwing away the packaged units. It does not require any modification to currently established test flows. Furthermore, it does not take additional tester time because it only requires off-line data processing. We used an IC's measured I_{DDQ} and F_{MAX} parameters and compared them against a pre-characterized, already-established I_{DDQ} versus F_{MAX} relation curve (similar to Figs. 3 and 4). This relationship is fundamental in defining a frequency-dependent leakage limit. If for a given frequency, an IC has substantially higher leakage than expected by the intrinsic dependency (similar to the IC shown in Fig. 4); then, the IC is classified as defective. If the decision is doubtful, we may apply reverse body bias to the questionable IC only (if body terminal is available [15]) or lower its temperature and only measure its leakage. Temperature proved more effective for sensitivity.

There is a cost associated with improving sensitivity for low DPM applications since we introduced a third variable to the test. However, only leakage is measured. There is no need to re-measure the IC's frequency at temperature. This saves cost especially since the F_{MAX} test is expensive. Also, there is no need to sweep any parameters e.g. frequency. We compare against a priori known speed-adjusted leakage limit characterized at two temperatures. If the leakage was reduced in line with a pre-determined (pre-characterized) intrinsically expected value, then the IC is not defective. If not, the IC will be classified as potentially defective. The separation and test limit at lower temperature screens the defective IC. If the temperature range we use for sensitivity improvement is wide enough, then we can detect more subtle lower current conducting defects. Finally, the test is flexible and can be tuned to various applications requiring different degrees of quality, sensitivity and DPM levels.

6.2 Low Cost Products Test Applications

Some products do not measure F_{MAX} or are designed for a fixed frequency e.g., low cost products, fixed-speed ICs, ASICs, and constant throughput applications (DSPs). Here, one may use I_{DDQ} versus temperature to establish a correlative two-parameter test solution. Another approach is to add a ring oscillator (RO) circuit or any other delay chain circuits to the silicon white space for frequency measurement. Then we can measure this special circuit's frequency and plot it against actual IC product leakage for

testing purposes. Therefore, even this category of products can benefit from the advantages of I_{DDQ} versus F_{MAX} test.

7. Conclusions

This paper examined the impact of technology scaling on testability of deep submicron CMOS ICs. Elevated leakage currents are an essential element of aggressively scaled devices and technologies. These elevated intrinsic leakage distributions challenge the effectiveness of I_{DDQ} based test techniques. We characterized transistor and circuit leakage by measuring their sensitivities across frequency, temperature, and body bias. The results show that fundamental device behavior can be used to improve the testing sensitivity. Device leakage and its switching speed are functions of the threshold voltage (V_T) and transistor channel length (L_{eff}). Therefore, a strong correlation and dependency can be established between the I_{DDQ} and maximum operational speed (F_{MAX}) of a collection of ICs. Our characterization produced several testing solutions for ICs in aggressively scaled (0.13 μm and beyond) technologies. Multiple parameter testing solutions that combine parameters such as I_{DDQ}, F_{MAX}, temperature, reverse body bias and lowering power supply voltage can prolong the usefulness of I_{DDQ} or other effected tests. High performance MPUs may use two-parameter I_{DDQ} combined with F_{MAX} test. This test method is a low cost alternative for saving fast intrinsically leaky ICs while discriminating defective ones. In other IC applications where F_{MAX} is not being measured, one may use the two-parameter I_{DDQ} versus temperature test solution. We used RBB and temperature parameters as test variables to enhance the test sensitivity and have determined that temperature is the most effective parameter. We showed that temperature improved the test signal to noise ratio by an order of magnitude. Finally, the sensitivity can be tuned with a proper temperature range for meeting more stringent quality requirements.

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