A Sub-0.5 V Dynamic Threshold PMOS (DTPMOS) Scheme for Bulk CMOS Technologies

Mohamed Elgebaly and Manoj Sachdev
Department of Electrical and Computer Engineering
University of Waterloo, ON, Canada N2L 3G1
{mgebaly,msachdev}@vlsi.uwaterloo.ca

Abstract

A new dynamic threshold PMOS (DTPMOS) scheme is presented. In this scheme, the gate of a PMOS transistor is connected to its well in a conventional bulk CMOS technology. This technique results in improved switching speed compared to conventional CMOS in the sub-0.5 V regime. A 32-bit carry skip adder is designed for low voltage, low energy applications using the DTPMOS scheme. This adder consumes only 0.25 pJ of energy at a frequency of 5 MHz. The proposed design results in a 64 % reduction in delay and 26 % saving in energy compared to the conventional CMOS implementation.

1. Introduction

With the increasing demand for portable applications, low power, low energy VLSI design has been growing very rapidly over the recent years. Energy consumption is becoming a major constraint even for desktop systems due to the enormous increase of such systems and the impact of that increase on energy sources.

Reducing energy consumption can be accomplished in different ways on the system, logic, circuit and device levels. One of the main approaches for energy reduction is power supply, V_{DD}, scaling. Reducing V_{DD} results in a considerable energy saving due to the quadratic relationship between V_{DD} and power. However, reduction of V_{DD} is usually accompanied by a reduction in the switching speed. This degradation in performance is a result of the small current drive when the V_{DD} approaches the transistor's threshold voltage, V_{TH}. Therefore, V_{DD} reduction is usually accompanied by a reduction in V_{TH}.

Assaderaghi *et.al.* [1] introduced the concept of the dynamic control of the threshold voltage (DTMOS) by connecting the gate of the MOS transistor to its substrate in silicon on insulator (SOI) technology. Logic implemented using the DTMOS scheme has a low V_{TH} in the on-state and high V_{TH} in the off-state. Consequently, DTMOS has a high switching speed during the on-state.

In this paper, the concept of the dynamic control of the threshold voltage is extended to bulk CMOS technologies. However, only the gate of the PMOS transistor is connected to the well. This type of connection can be implemented in bulk CMOS since each PMOS transistor is implemented in a separate well isolated from other PMOS transistors. This technique allows for energy efficient realizations of digital blocks working at sub-0.5 V.

2. Dynamic Threshold PMOS (DTPMOS) Scheme

The proposed concept relies on the connection between the gate and the well of PMOS transistors to reduce V_{TH_p} during the on-state and maintain a high V_{TH_p} in the off-state. For simplicity, the threshold voltage of the DTPMOS transistor will be denoted V_{TH}. The dynamic nature of the DTPMOS threshold voltage can be explained from the expression [2]

$$V_{TH} = V_{TH_0} - \gamma(\sqrt{|-2\Phi_F|} - \sqrt{|-2\Phi_F + V_{BS}|}) \quad (1)$$

Here V_{TH_0} is the threshold voltage at zero body bias, γ is the body effect coefficient, $2\Phi_F$ is the surface potential at strong inversion, and V_{BS} is the body-source voltage. The minus sign of the body effect coefficient in (1) is due to the forward biased body-source junction [1]. During the on-state and assuming that V_{DD} is 0.5 V, V_{BS} for conventional CMOS is zero while it is -0.5 V for DTPMOS. Assuming that V_{TH_0} is -0.435 V, γ is 0.5667 and $2\Phi_F$ is 0.6 V, V_{TH} is reduced to -0.28 V (36% reduction) compared to its value at zero body bias. During the off-state, however, V_{BS} is set back to zero

and V_{TH} returns to its original value at zero body bias, V_{TH_0}. The low threshold voltage in the on-state leads to a significant reduction in delay at a low voltage supply.

Compared to conventional CMOS, DTPMOS results in a higher PMOS current drive and consequently a higher speed operation at a very low voltage. This is mainly due to a larger inversion charge and a lower effective normal field in the channel. The lower effective normal field leads to higher mobility and consequently higher current drive [1].

2.1. Pass-Transistor Full Adder Circuit Featuring the DTPMOS scheme

In order to explore the characteristics of operation of the DTPMOS scheme, a pass-transistor full adder (FA) circuit is implemented in both DTPMOS and conventional CMOS. Figure 1 shows the DTPMOS implementation of the FA circuit. Pass-transistors used are all minimum sizes. The pass-transistor logic style is chosen as it has an efficient energy consumption compared to other logic styles. The double-pass logic (DPL) was shown to be more energy efficient [3] but it fails to work in the sub-0.5 V regime. This mainly because of the NMOS transistors used which have threshold voltage of 0.48 V in the technology used in this work.

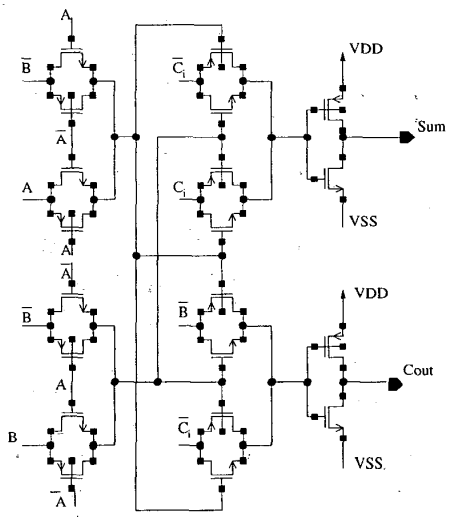

Figure 1. DTPMOS Full Adder circuit.

HSPICE simulations for the FA circuit for both the DTPMOS and conventional CMOS schemes are carried out in the TSMC 0.18 μm CMOS technology. The input frequency is 20 MHz. The simulation setup is to connect all the outputs of the FA circuit (*simulated* circuit) to inputs of a similar FA circuit (load circuit). The outputs of the load circuit are connected to 10 fF loads. Only the measurements of the *simulated* circuit are recorded.

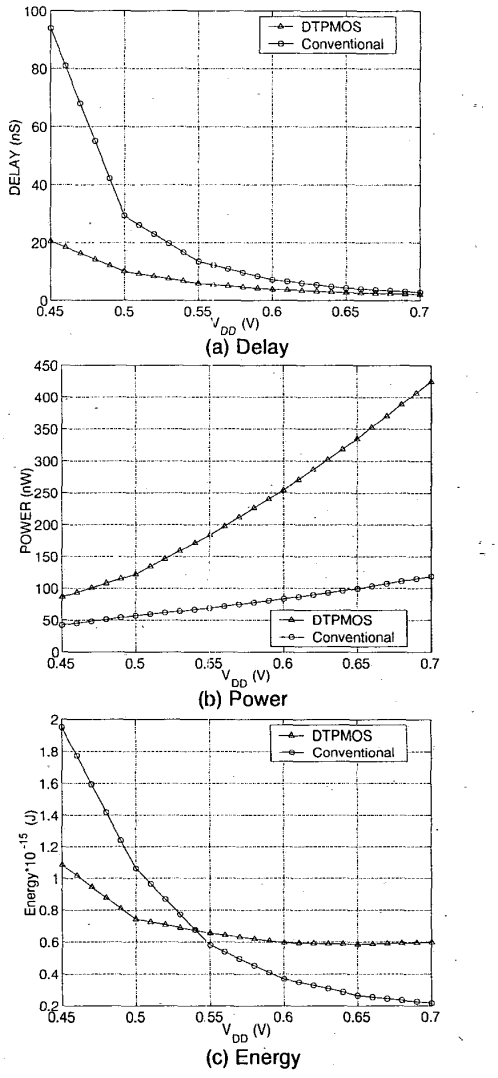

Figure 2. Simulation results for the different implementations of the FA circuit at different supply voltages.

A comparison between the DTPMOS FA and the conventional CMOS FA is illustrated in Figure 2. Figure 2 (a) shows

that using DTPMOS is advantages below the 0.5 V supply voltage. Above that point, the difference in delay compared to conventional CMOS becomes negligible. Increasing V_{DD} beyond the 0.5 V point, however, results in a significant increase in the leakage current and consequently an increase in power and energy as shown in Figure 2 (b) and (c). Therefore, the DTPMOS scheme is attractive for sub-0.5 V operation.

2.2. Leakage Power Reduction

When the gate is connected to to the well in the DTPMOS scheme, the leakage current increases. The source/drain-body junction becomes forward biased when the supply voltage is increased above the diode cut-in voltage [4]. Above the 0.5 V supply, this leakage current increases exponentially. Kawaguchi *et.al.* [5] proposed a scheme to reduce the high standby current by adding a low-V_{TH} PMOS transistor to control the supply voltage of the circuit. This cut-off transistor disconnects the circuit from the main supply during the standby mode. The addition of a low-V_{TH} PMOS cut-off transistor reduces the off-state leakage current significantly.

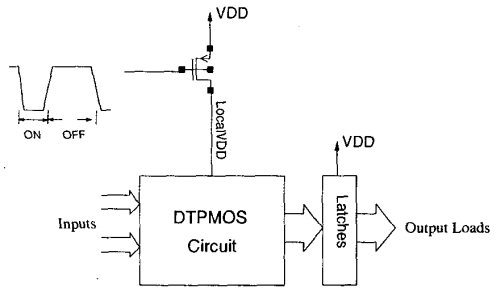

Figure 3. Controlling supply voltage to reduce the standby current using a cut-off DTPMOS transistor.

In this work, the DTPMOS serves as the low-V_{TH} cut-off device. The cut-off DTPMOS is advantageous since it can be implemented in normal bulk CMOS without the need for a multi-threshold technology. This approach is illustrated in Figure 3. A large cut-off DTPMOS transistor is required to supply a high current drive to the DTPMOS circuit. When $LocalVDD$ is turned OFF, the output signals have to be stored until the supply voltage turns back ON. The structure of a two cross-coupled inverters is used as a simple latch to store the output value of each signal. Those latches are directly connected to the main supply voltage, V_{DD}, as shown in Figure 3. Since the latches are always ON, conventional CMOS transistors are used in the latch's structure to minimize standby current.

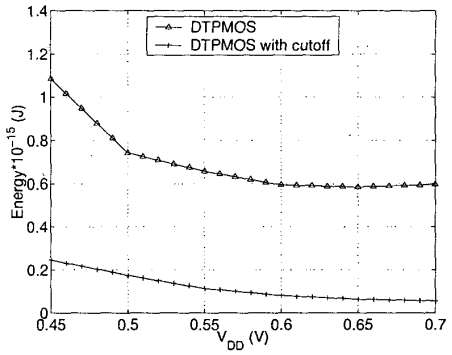

Figure 4. Energy reduction using the cut-off scheme.

The advantage of using a cut-off transistor in DTPMOS circuits is clearly shown in Figure 4. The cut-off transistor is turned OFF after the maximum FA delay (approximately 35 ns at 0.45 V). The simulation frequency is set to 5 MHz. The graphs illustrate the energy reduction that can be achieved compared to the DTPMOS scheme without a cut-off transistor. Although using the cut-off DTPMOS transistor results in a relatively reduced speed, it allows for significant power and energy savings specially when the circuit remains in the standby mode for a large portion of the system clock.

3. 32-Bit Carry Skip Adder Implementation and Simulation Results

A 32-bit carry skip adder (CSA), sometimes is called manchester adder, is chosen since it is one of the most energy efficient structures compared to other adder implementations [6]. The CSA is implemented using a variable carry skip group size. The carry skip group size has been optimized to minimize the carry propagation time. The optimal number of groups is 10 with sizes of $1, 2, 3, 4, 5, 6, 5, 3, 2, 1$ [7]. This architecture yields a carry propagation time $\leq 9t_{FA}$ where t_{FA} is the delay of a full adder.

The CSA is implemented using both DTPMOS and conventional CMOS schemes. The load capacitance is set to and the simulation frequency is 5 MHz. This due to the fact that the conventional CMOS CSA has a delay of 330 ns and therefore the simulation time has to be greater than that. Table 1 shows simulation results for both implementations. The power

consumed by each design is a result of the average consumption over 100 cycles of randomly distributed inputs. The DTPMOS scheme is 64% faster and 26% more energy efficient compared to the conventional CMOS implementation. The DTPMOS scheme consumes more power due to the forward biased source body junction as explained earlier in section 2.

Table 1. Simulation results for the different CSA implementations

Design	Delay (ns)	Power (μW)	Energy (pJ)
DTPMOS	120	2.11	0.25
Conventional CMOS	330	1.03	0.34

4. Conclusion

A dynamic threshold PMOS (DTPMOS) scheme was presented. By connecting the gate and the well of the PMOS transistor, the DTPMOS demonstrates a low threshold voltage in the on-state and a high threshold voltage in the off-state. The new scheme allows for sub-0.5 V operation in bulk CMOS technologies with a significant improvement in performance and a reasonable reduction in energy compared to conventional CMOS. A 32-bit carry save adder was designed utilizing the DTPMOS scheme in the 0.18 μm bulk CMOS technology. Simulation results show that 64% reduction in delay and 26% energy saving can be achieved compared to the conventional CMOS implementation at 0.48 V and a frequency of 5 MHz. The DTPMOS scheme is mostly suitable for sub-0.5 V operation. Above the 0.5 V, the efficiency of the DTPMOS scheme is reduced due to the increase in static power dissipation.

Acknowledgment

This work has been supported by a strategic grant from the Natural Sciences and Engineering Research Council (NSERC) of Canada and Gennum corporation.

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