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Dual Supply Voltage Clocking for 5GHz 130nm Integer Execution Core

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Abstract

This paper describes dual-V_{cc} clocking on a 1.2V, 5GHz integer execution core fabricated in 130nm CMOS to achieve up to 71% measured clock power (including 15% active leakage) reduction. A write-port style pass-transistor latch and split-output level-converting local clock buffer are described for robust, DC power free low-V_{cc} clock operation.

Introduction

Increasing complexity of synchronous clocking has resulted in clock power as the dominant source of total power in multi-gigahertz processors. Low supply voltage (low-V_{cc}) clock grid with high supply voltage (high-V_{cc}) core logic and latches enables full-chip clock power reduction without sacrificing logic performance. However, DC power at the V_{cc} interface due to improper PMOS shutoff renders conventional pass-gate latches and local clock buffers (LCBs) impractical. Further, every successive stage of clock drivers at low-V_{cc} degrades supply noise sensitivity and edge-rates, increasing cycle-to-cycle jitter. Two dual-V_{cc} clocking schemes are described for a 0.8V, 1.5x1.5mm clock grid of a 1.2V, 5GHz integer execution core (IEC) fabricated in 130nm CMOS technology (Fig. 1) [1]. Clock power vs. jitter tradeoff of (i) low-V_{cc} on both grid drivers/repeaters and LCBs (G+L), and (ii) low-V_{cc} only on grid drivers/repeaters but high-V_{cc} on the LCBs to achieve full-swing faster edge-rate clock at the latches (G-only) are presented. A glitch-free write-port pass-transistor latch with single-ended low-V_{cc} clock is described for G+L clocking. A split-output LCB for fast clock level conversion for G-only clocking is also described.

IEC Clock Grid

Fig. 2 shows organization of the 1.5x1.5mm IEC clock network. External at-speed 200mV low-swing differential clock is locally converted to full-swing single-rail core clock and driven to grid center. H-tree distribution is used to route core clock into four corner grid repeaters. LCBs are located at 9 tap-off locations to drive their respective execution units' latch loads. All drivers are nominal-skewed double inverters for good P/N mismatch tolerance. Low-V_t transistors are used throughout the clock network to achieve best performance. Effective 50% duty-cycle control is maintained via on-die differential op-amp tuning. Detailed field-solver simulations were performed to model the accurate RLC clock grid. Separate off-chip supply for clock grid and LCBs enables low-V_{cc} clocking with high-V_{cc} logic and latches. Robust clocking is measured up to 6.5GHz at 1.2V, 30°C.

G+L vs. G-only Dual-V_{cc} Clocking

Fig. 3(a) shows total clock energy measured at 5GHz for low-V_{cc}=0.8V and high-V_{cc}=1.2V at 30°C for G+L and G-only clocking. Fig. 3(b) shows worst-case jitter of all 9 load points simulated for ±15% DC supply noise on both high- and low-V_{cc}. Compared to conventional high-V_{cc} clock grid, the G+L scheme achieves 56% switching and 15% active leakage energy reduction; the latter is attributed to the strong dependence of subthreshold and gate leakage on V_{cc} in 130nm technology (Fig. 4). This benefit is especially important in the context of increasing active leakage with process scaling. Jitter increases by 3.3x and attendant clock edge-rate degradation at the latches due to low-V_{cc} is 35%. G-only low-V_{cc} clocking trades off energy savings in the LCBs for better jitter and achieves 39% switching energy and 10% leakage reduction for 1.7x jitter increase and same full-swing clock edge-rate at the latches as conventional clocking.

Dual-V_{cc} Latch and Local Clock Buffer

To enable practical G+L and G-only dual-V_{cc} clocking, DC power free latches and LCBs are proposed. Fig. 5(a) shows the proposed pass-transistor latch for G+L clocking, which uses a register file write-port style structure. Conventional low-V_{cc} clocked latches either require multiple clock rails or suffer from severe charge transfer glitch due to local D# inverters [2]. In the proposed latch, the local D# and CLK# inverters are eliminated, resulting in robust glitch-free operation (Fig. 5(b)) and a dense 9T implementation. Clock fanin load is only two NMOS transistors, enabling further clock power savings. Table 1 shows 130nm simulated worst-case D→out delay, latch energy (D-activity=0.1, CLK-activity=1.0) at 5GHz operation, and setup time comparisons against a production 32-bit processor's regular high-V_{cc} clocked pass-gate latch [3] and sense-amplifier style low-V_{cc} clocked latch [4]. All latches are optimized for constant fanout load and input capacitance using a Lagrange-multiplier based quadratic optimizer. The proposed latch is 14% faster than sense-amplifier latch and only 2% slower than the best-speed pass-gate latch despite reduced V_{GS} underdrive. Speed benefit is due to absence of D# inversion delay and inherent positive feedback of the bitcell inverters. Elimination of local D# inverter also improves setup times by 24% compared to sense-amplifier latch. Fig. 6 shows susceptibility of all latches to ±15% DC supply noise on both V_{cc}'s and across worst-case 130nm fast/slow process corners. The proposed latch shows acceptable D→out spread across voltage and process corners, comparable to pass-gate and sense-amplifier latches.

Fig. 7 shows the proposed split-output level-converting LCB for G-only clocking. To drive the large fanout latch loads, conventional CVSL level converter LCBs require significant upsizing, which aggravates contention power in CVSL stage or require several output gain stages that amplifies jitter [5]. The split-output scheme decouples the fanin CVSL stage from the output driver stage, enabling fast level conversion with lower contention, fanin load and area (Table 2). Fig. 8 shows energy-delay simulations between proposed and conventional CVSL LCBs. The proposed LCB achieves 47% delay or 16% energy reduction for 0.8V→1.2V clock level conversion.

Conclusion

Dual-V_{cc} clocking on a 1.2V, 5GHz IEC fabricated in 130nm CMOS is described for 71% clock power reduction. DC power free dual-V_{cc} latch and LCB are also described.

Acknowledgement

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References

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[5] Y. Kanno et al, 2000 VLSI Circuits Symp. Digest, pp. 202-203.

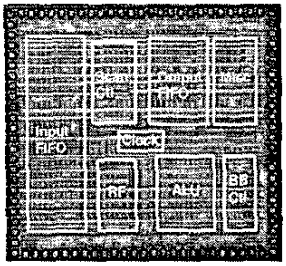
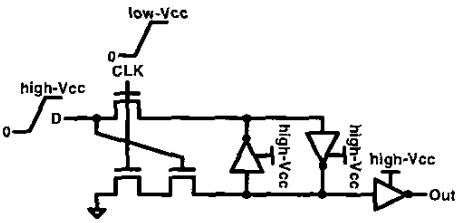


Fig. 1. 130nm IEC testchip



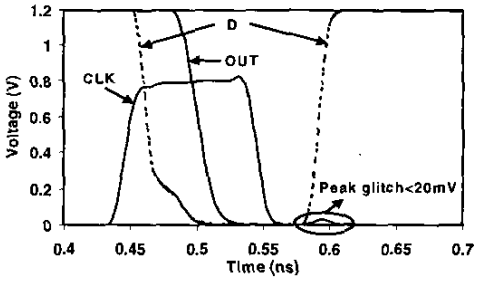


Fig. 5(a) Proposed dual-Vcc latch and (b) operation

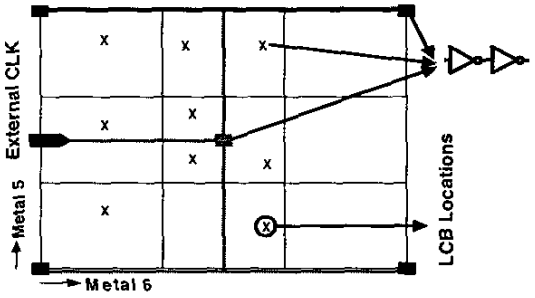
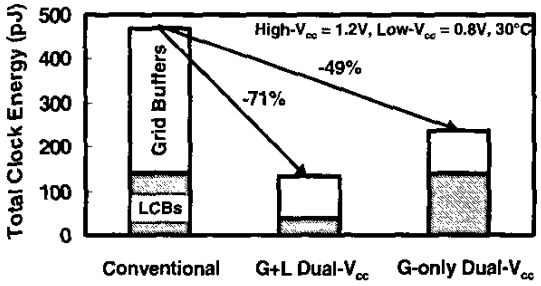


Fig. 2. IEC clock network



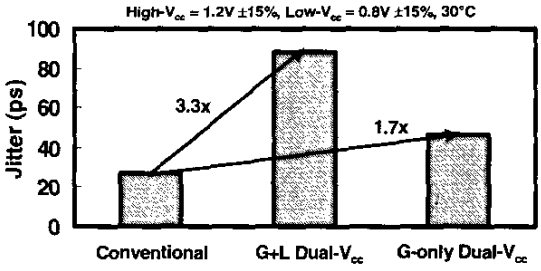


Fig. 3(a) Clock energy measurements & (b) jitter simulation

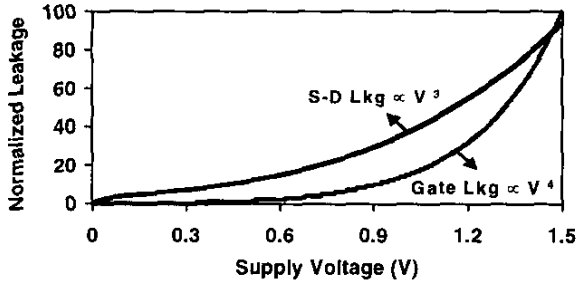


Fig. 4. 130nm Vcc vs. leakage measurements

Latch Scheme	# Transistors	D→OUT (ps)	Energy (pJ)	Tsetup (ps)
Pass-gate high-V_{cc}	11	37	0.76	20
Sense-amp dual-V_{cc}	11	44	0.59	57
This work	9	38	0.66	43

Table 1. 130nm latch comparisons (high-V_{cc}=1.2V, low-V_{cc}=0.8V, 30C)

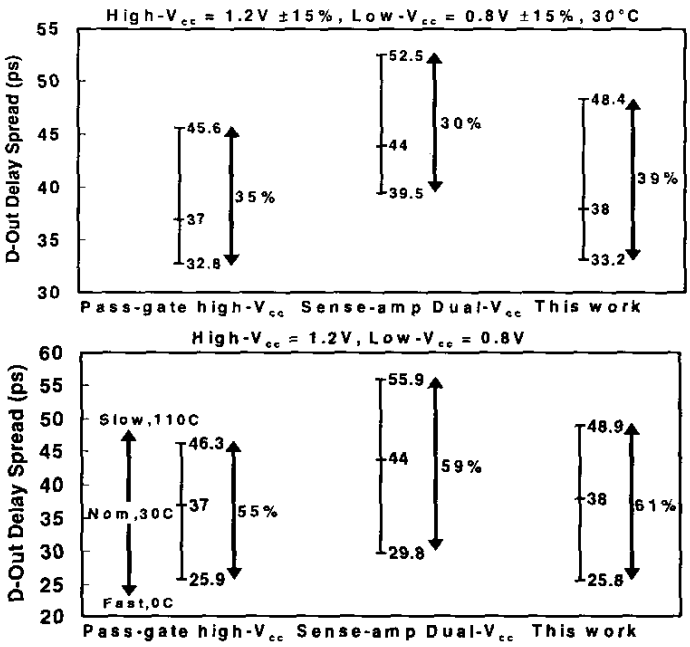


Fig. 6. Latch supply and process variation sensitivity

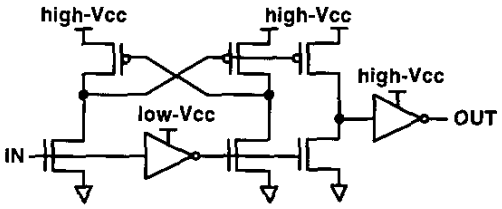


Fig. 7. Proposed LCB scheme

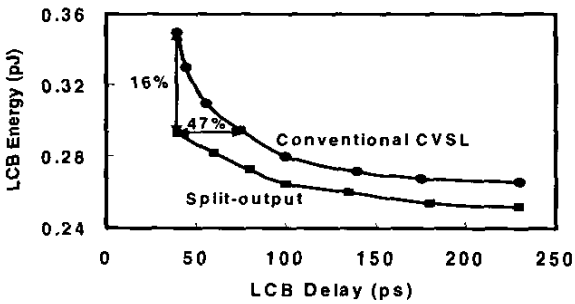


Fig. 8. LCB energy-delay comparison

LCB Scheme	Fanin cap (fF)	Total area (μm²)	CVSL-stage contention energy (pJ)
Conventional CVSL	8.2	15.5	0.085
This work	7.1 (-14%)	13.8 (-11%)	0.039 (-54%)

Table 2. 130nm LCB comparisons (high-V_{cc}=1.2V, low-V_{cc}=0.8V, 30C)