# An Analytical Equation for the Oscillation Frequency of High-Frequency Ring Oscillators

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***Abstract*—An analytical equation for the oscillation frequency of a ring oscillator is derived. The derivation is done using a novel method which does not need to find an expression for the delay of each stage. The resulting equation includes the effect of time-varying parasitics. It also includes the effect of the gate resistance, which has a large effect on the oscillation frequency at high frequencies. Measurement results of ring oscillators fabricated in a 0.18-$\mu$m CMOS process show that the resulting equation has an average error of 8% over a large range of parameter variations.**

***Index Terms*—Equations, high-speed integrated circuits, ring oscillators, voltage-controlled oscillators.**

## I. Introduction

THE voltage-controlled oscillator (VCO) is a commonly investigated circuit due to its use in communications circuits such as phase-locked loops (PLLs) and clock and data recovery circuits (CDRs) [1]–[7]. A common VCO architecture is based on the ring oscillator. Despite its widespread usage, the ring oscillator still poses difficulties when it comes to design, analysis, and modeling. The design of a ring oscillator involves many tradeoffs in terms of speed, power, area, and application domain. For the designer to make informed decisions regarding these tradeoffs, an accurate method to determine the oscillation frequency of the ring oscillator is necessary. One way to determine the oscillation frequency is to simulate the circuit using a numerical simulator, such as HSPICE. Although the oscillation frequency predicted may be accurate for the simulated circuit, there is no clear way for the designer to know how to improve the desired circuit parameters. The designer can find some basic trends by running several different simulations, but even then, the impact of modified variables may not be apparent.

An alternative method of design is to derive an analytical equation for the oscillation frequency of the VCO. This analytical equation will contain terms based on circuit and process parameters. The circuit parameters can show the designer what tradeoffs are possible based on design changes such as increasing the power dissipation. The process parameter components of the equation can be used to determine the limits of the VCO for a given technology. This can be important if a high-frequency VCO is required, or if the designer wishes to determine how the frequency limits of the VCO will change with technology scaling.

The work proposed in this paper is an extension of the method described in [8]. In [8], we derived an analytical expression for the oscillation frequency of ring-oscillator-based VCOs. However, the expression had relatively large error at high frequencies owing to second-order parasitic effects. The proposed work accounts for the contribution of time-varying parasitics. Furthermore, it includes the effect of the gate resistance that cannot be neglected at higher frequencies. This paper is organized as follows. Section II provides an overview of the method used to derive the oscillation frequency equation. Section III explains the steps needed to include time-varying parasitics and Section IV describes the inclusion of the gate resistance in the model. Section V presents the experimental results and compares the measured frequency values with those predicted by the derived analytical equation.

## II. Overview of Method Used to Derive Oscillation Frequency Equation

The most common way to derive an equation for the oscillation frequency of an $N$-stage ring oscillator is to assume each stage provides a delay of $t_d$. The signal must go through each of the $N$ delay stages twice to provide one period of oscillation. Therefore, the period is $2N \cdot t_d$, resulting in the frequency equation in (1).

$$f = \frac{1}{2N \cdot t_d}. \tag{1}$$

The difficulty in obtaining an expression for the frequency arises when trying to determine an expression for $t_d$, mainly due to the nonlinearities and parasitics of the circuit. This paper will focus on differential delay stages, such as the one shown in Fig. 1. This delay stage contains a source-coupled pair $N_1$ and $N_2$, a tail current $I_{SS}$, and pMOS transistors $P_1$ and $P_2$. However, even with a circuit that appears as simple as this one, many assumptions and simplification are necessary to obtain an accurate value for $t_d$. Examples of derivations of the expressions for $t_d$ and the resulting frequency equations can be found in [9]–[11].

A different method to derive an equation for the oscillation frequency is proposed in [8]. This method does not try to find a value for $t_d$. Instead, the method creates a system of equations which can be reduced to a single equation where the only unknown is the frequency. The method begins by assuming that the voltage waveform at the input of a stage is sinusoidal with an unknown frequency. Therefore, an expression

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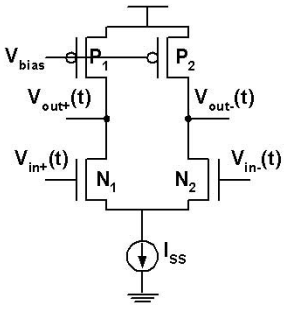



Fig. 1. Delay stage.

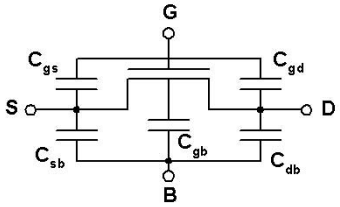



Fig. 2. MOSFET with parasitic capacitances.

for the output voltage of the stage is also known, as it is a phase-shifted version of the input voltage. These voltage expressions can be used to create expressions for currents in the delay stage. These expressions can be reduced and solved for the frequency of oscillation. Ref. [8] describes this method in detail and demonstrates it with an example using a common ring-oscillator topology. The example in [8] includes many parasitics and secondary effects. However, it still makes some simplifying assumptions for demonstration purposes. For example, the effect of a time-varying capacitance on the current equation was not fully accounted for. Also, the gate resistance of the source-coupled pair was ignored, which has a very large effect at high oscillation frequencies. These effects will be included and a new equation will be derived which is accurate over a larger range of parameter variations.

## III. Equation Including Parasitic Capacitances

A new frequency equation will now be derived based on a ring oscillator using a delay stage such as that in Fig. 1. The parasitic capacitances of a MOSFET have a large effect on the oscillation frequency. A model of the MOSFET including parasitic capacitances is shown in Fig. 2 [12].

The expressions for many of these capacitances include hspice parameters. The definitions of the relevant parameters are given in Table I.

A frequency equation taking into account the parasitic capacitances was derived in [8]. However, one assumption from [8] related to the time-varying drain–bulk capacitances will be removed here. An expression for the drain–bulk capacitance is given in (2).

$$C_{db} = \frac{Cj \cdot Ad}{\left(1 + \dfrac{V_{db}(t)}{pb}\right)^{mj}} + \frac{Cjsw \cdot Pd}{\left(1 + \dfrac{V_{db}(t)}{pbsw}\right)^{mjsw}}. \quad (2)$$

For a delay stage such as that in Fig. 1, the drain voltage on all four transistors is time-varying, and therefore the value of the drain–bulk capacitance is time-varying. To derive the frequency equation, expressions for the currents needed charge the parasitic capacitances in the delay stage must be found. A general expression for the current into a capacitor is given in (3). The derivation in [8] ignored the second term on the right-hand side of (3) related to the time-varying capacitance. This simplification will be removed here.

TABLE I
HSPICE Parameters

| | |
|---|---|
| Cj | Zero-bias area junction capacitance |
| Cjsw | Zero-bias sidewall junction capacitance |
| Cgdo | Gate-drain overlap capacitance |
| pb | *p-n* junction potential |
| pbsw | *p-n* junction sidewall potential |
| mj | Area junction grading coefficient |
| mjsw | Sidewall junction grading coefficient |
| Ad | Drain area |
| Pd | Drain perimeter |

$$I = C\frac{dV}{dt} + \frac{dC}{dt}V. \quad (3)$$

Using the method described in [8] and the current equation given in (3), the oscillation frequency given in (4) can be derived. It is important to note that many steps to obtain this equation have been skipped and a detailed example demonstrating the necessary steps are given in [8].

$$f = \frac{I_{SS}}{2NV_{\rm sw}\left(C_{\rm in} + Cgd_p + Cdb_n + Cgdov_n + Cdb_p\right)}. \quad (4)$$

where $I_{SS}$ is the tail current, $N$ is the number of delay stages in the ring, $V_{\rm sw}$ is the amplitude of the voltage swing across the load and the capacitance values are given by the following expressions.

$$C_{\rm in} = \frac{2}{3}W_nL_nC_{\rm ox} \quad (5)$$

$$C_{gdp} = \frac{1}{2}W_pL_pC_{\rm ox} \quad (6)$$

$$Cdb_n = \frac{Cj_nAd_n}{\left(1 + \dfrac{V_{\rm dd}}{pb_n}\right)^{mj_n}}\left[2 - mj_n\left(1 - \frac{1}{\left(1 + \dfrac{V_{\rm dd}}{pb_n}\right)}\right)\right] + \frac{Cjsw_nPd_n}{\left(1 + \frac{V_{\rm dd}}{pbsw_n}\right)^{mjsw_n}} \cdot \left[2 - mjsw_n\left(1 - \frac{1}{\left(1 + \dfrac{V_{\rm dd}}{pbsw_n}\right)}\right)\right] \quad (7)$$

$$Cgdov_n = \left(1 + \cos\left(\frac{\pi}{N}\right)\right)W_nCgdo_n \quad (8)$$

$$Cdb_p = 2Cj_pAd_p + 2Cjsw_pPd_p. \quad (9)$$

Equation (4) shows the contribution of the time-varying parasitics on the oscillation frequency. The weighting of the drain–bulk capacitance terms, (7) and (9), is higher than in previously derived equations. Some equations, such as the one

derived in [9], use the average value of these time-varying terms, but our method suggests the actual weighting is about twice that value [the expression in the square brackets in (7) is approximately 1.8 for typical process parameters]. This is due to the nonzero $dC/dt$ term in (3). Moreover, the gate–drain overlap capacitance in (8) is multiplied by a factor of $1+\cos(\pi/N)$. This factor is equivalent to showing the effect of the Miller capacitance at this node because the voltages at both nodes of the capacitor, $V_{\text{in}+}(t)$ and $V_{\text{out}+}(t)$, are moving in opposite directions. As $N$ increases, the phase difference of these voltages approaches $\pi$, and the value of $1+\cos(\pi/N)$ approaches 2, resulting in a doubling of the gate–drain overlap capacitance.

## IV. Gate Resistance

Equation (4) can be shown to be accurate at low frequencies, but starts to deviate from simulated and measured values at higher frequencies. This increase in error is because the parasitics included in the derivation of (4) are based on a low-frequency compact model. It is generally agreed that at least a gate resistance and a substrate coupling network should be added to the model if it is to be used at radio frequencies (RF) [13]–[15]. However, adding the whole network will substantially increase the complexity of the resulting equation. Since the purpose of the analytical equation is to easily show the tradeoffs to a designer, a simpler RF model is desirable. It can be shown that an RF model with gate resistance is a minimum requirement [15]. Therefore, only a gate resistance will be added to the model for this derivation. The gate resistance in this case only represents the resistance of the polysilicon gate and does not include any bias-dependent components. Fig. 3 depicts the schematic of a delay stage with gate resistances for the source-coupled pair $N_1$ and $N_2$

As shown in Fig. 3, the gate resistance will affect the differential input voltage to the source-coupled pair. The change in differential input voltage, $V_{id}(t)$, will affect the current through $N_1$ and $N_2$. To determine an expression for $V_{id}(t)$, expressions for $V_{\text{ing}+}(t)$ and $V_{\text{ing}-}(t)$ must first be determined and are given by (10) and (11).

$$V_{\text{ing}+}(t) = V_{\text{in}+}(t) - I_{\text{cin}}(t)\, R_g \tag{10}$$

$$V_{\text{ing}-}(t) = V_{\text{in}-}(t) + I_{\text{cin}}(t)\, R_g. \tag{11}$$

$I_{\text{Cin}}(t)$ is a function of $V_{id+}(t)$, resulting in an equation that is difficult to solve. To remove this dependence, first note that the phase of the current into a capacitor has a $\pi/2$ phase shift from the voltage. Since the voltage is a sine wave, the current will be a cosine. Also, the amplitude of the current waveform for $I_{\text{Cin}}(t)$ can be represented as a fraction of the total tail current $I_{SS}$. This fraction is fairly constant, although it is a weak function of $I_{SS}$, $V_{\text{sw}}$, and $N$. This fraction will be called $I_{\text{frac}}$, which simulations show to be about 0.2. Therefore, (10) and (11) can be rewritten as (12) and (13).

$$V_{\text{ing}+}(t) = V_{\text{in}+}(t) - I_{\text{frac}} I_{SS} \cos(2\pi f t) R_g \tag{12}$$

$$V_{\text{ing}-}(t) = V_{\text{in}-}(t) + I_{\text{frac}} I_{SS} \cos(2\pi f t) R_g. \tag{13}$$

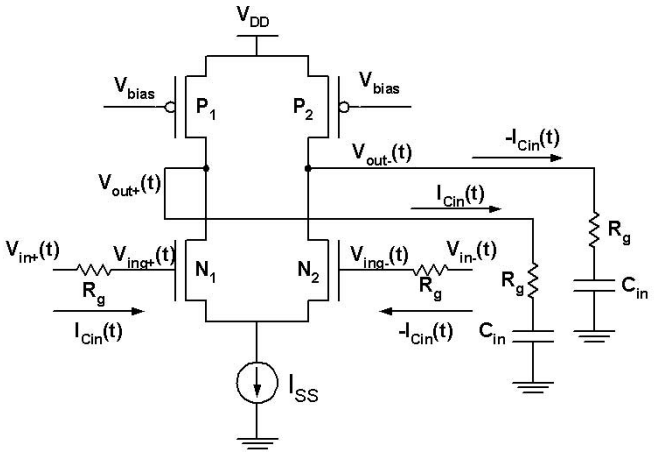



Fig. 3. Delay stage with gate resistance.

Therefore, the current through $R_g$ is no longer a function of $V_{\text{in}+}(t)$. Without gate resistance, the differential input voltage $V_{id}(t)$ was given by $V_{\text{in}+}(t) - V_{\text{in}-}(t)$. With gate resistance, the differential input voltage is now found as $V_{\text{ing}+}(t) - V_{\text{ing}-}(t)$, which is shown in (14).

$$V_{idg}(t) = V_{id}(t) - 2I_{\text{frac}} I_{SS} \cos(2\pi f t) R_g. \tag{14}$$

Using this new expression for the differential input voltage and the method described in [8], a new equation for the oscillation frequency of a ring oscillator can be derived. The final resulting equation is given in (15), an equation for the oscillation frequency of a ring oscillator accounting for time-varying parasitics and the gate resistance.

$$f = \frac{I_{SS}}{2NV_{\text{sw}}(C_{\text{in}} + C_{\text{par}})} \cdot \left[1 - \frac{I_{SS} R_g}{V_{\text{sw}}} \left( \left( \frac{C_{\text{par}}}{C_{\text{in}} + C_{\text{par}}} \right) \left( 2 - N \left( \frac{1}{2} - \frac{1}{\pi} \right) \right) + \frac{2\sqrt{2} N I_{\text{frac}}}{\pi} \right) \right] \tag{15}$$

where $C_{\text{par}} = Cgd_p + Cdb_n + Cgdov_n + Cdb_p$. The addends of $C_{\text{par}}$ were given in (6)–(9).

Equation (15) can be used to quantify the effect of the gate resistance on the oscillation frequency. Note that if $R_g$ is set to 0, (15) becomes (4), the equation previously derived for the oscillation frequency. Therefore, the effect of the gate resistance is to add a multiplier term to the frequency equation. The maximum value for the multiplier is 1, which occurs when $R_g$ is 0. The value of the multiplier decreases as the gate resistance increases, showing that a higher gate resistance decreases the oscillation frequency. Also, note that the weighting of the $R_g$ term increases as $I_{SS}$ increases or $V_{\text{sw}}$ decreases. Therefore, the weighting of this term is greater at high frequencies, meaning that the gate resistance has a larger effect at high frequencies. Equation (15) can also be used to analyze tradeoffs at the layout stage of the design since the gate resistance and the drain–bulk capacitances are both layout dependent. For example, having

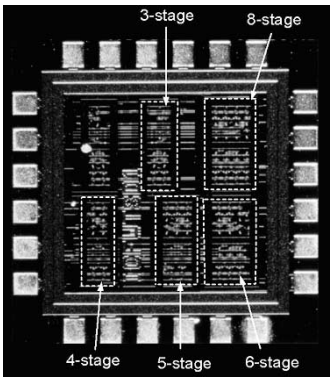



Fig. 4. Microphotograph of test chip.

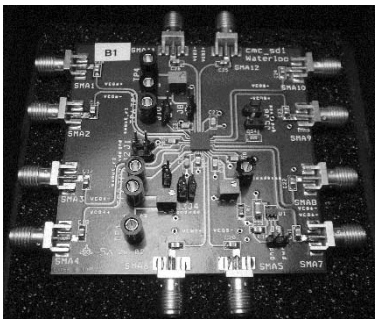


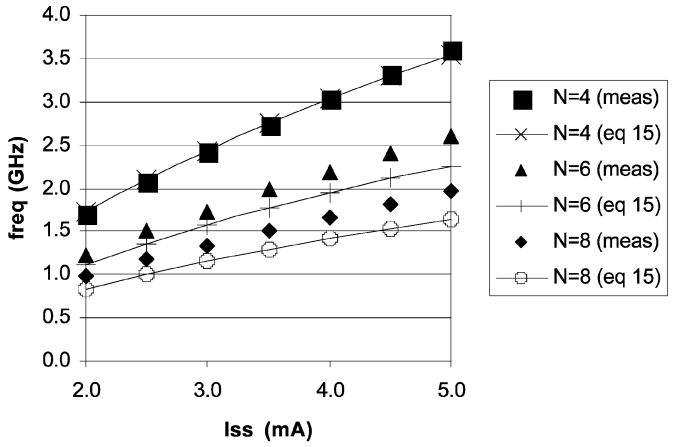
Fig. 5. Test board.

two gate contacts can minimize the gate resistance, but this can also complicate and increase the area of the layout. The designer can use (15) to quantify this tradeoff and make a more informed design decision. Section V will show experimental results that will demonstrate the importance of including the gate resistance when predicting the oscillation frequency of multigigahertz ring oscillators.

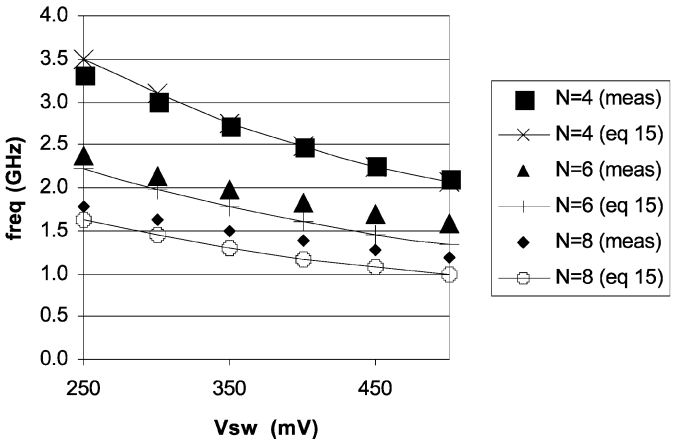
## V. Test Setup and Results

To verify (15), a test chip was designed in a 1.8-V 0.18-$\mu$m CMOS process. The main design parameters of a ring oscillator, $I_{SS}$, $V_{\rm sw}$, and $N$, were made variable to see how the frequency changes with respect to these parameters. To vary $N$, the test chip contains five separate ring oscillators with different numbers of delay stages (3, 4, 5, 6, and 8). An external resistor was utilized to vary $I_{SS}$. This external resistor controls the current of a current source that is mirrored in each delay stage. Finally, an external bias voltage on the pMOS load is used to control $V_{\rm sw}$. For each of the five ring oscillators, $I_{SS}$ was varied from 2 to 5 mA and $V_{\rm sw}$ was varied from 250 to 500 mV. A microphotograph of the chip is shown in Fig. 4 and a picture of the test board in Fig. 5. For the test chip, the layout of the gate of concern has been done using 16 fingers where each finger is 7.5 $\mu$m/0.18 $\mu$m resulting in a gate resistance of 12 $\Omega$. The chip was packaged in a Quad Flatpack No lead (QFN) package.

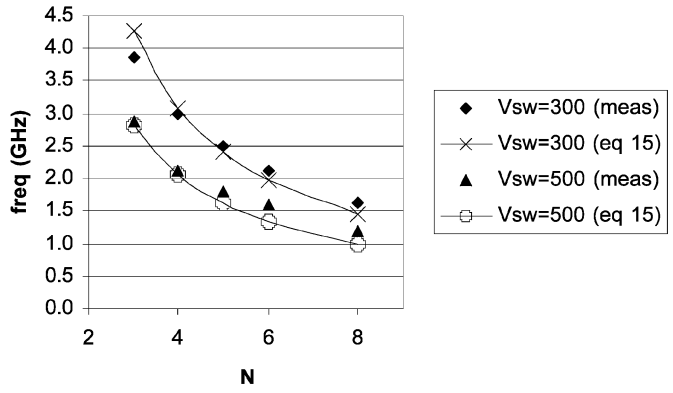
The experimental results are shown in Fig. 6. Fig. 6(a) shows the frequency versus $I_{SS}$, Fig. 6(b) shows the frequency versus $V_{\rm sw}$, and Fig. 6(c) shows the frequency versus $N$. The reported results are an average of the measurements from four test chips. The average error between the predicted frequency value using




a) frequency versus $I_{SS}$ with $V_{sw}$=350mV




b) frequency versus $V_{sw}$ with $I_{SS}$=3.5mA




c) frequency versus N with $I_{SS}$=3.5mA

Fig. 6. Comparison of experimental and analytical results based on (15). (a) Frequency versus $I_{SS}$. (b) Frequency versus $V_{\rm sw}$. (c) Frequency versus $N$.

(15) and the measured frequency value over the range of parameter variations is found to be 8.2%. It can also be noted that, since the derivation was performed using SPICE parameters, the average error between (15) and the simulated frequency value over the same range of parameters was 7.7%.

Prediction of the oscillation frequency is an important aspect of any analytical equation. However, it is also important to show the tradeoffs between the frequency and various design

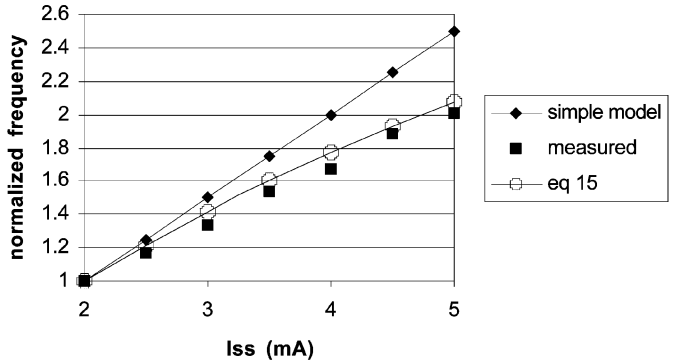



Fig. 7. Normalized frequency versus $I_{SS}$.

parameters so as to build an intuitive understanding of the design. For example, (4) and equations derived in [10] and [11] suggest that the frequency increases linearly with an increase in $I_{SS}$. Since $I_{SS}$ is directly proportional to power, this suggests a direct tradeoff between the oscillation frequency and the power dissipation. However, simulation and experimental results show that the actual increase in frequency is less than linear. Therefore, it is important that the designer be able to predict the actual increase in frequency with respect to the increase in $I_{SS}$. Equation (15), which accounts for the effect of the gate resistance, is able to accurately predict this trend, as is shown in Fig. 7. In this figure, frequency has been normalized so that the frequency at the lowest value of $I_{SS}$ is equal to 1. According to a simple model for the oscillation frequency, which does not account for the effect of the gate resistance, if the current is increased by 2.5 times to 5 mA, the frequency should increase by 2.5 times. However, measurements show that the actual increase in frequency is only about 2 times. This trend is well predicted by (15), meaning that it can be used to accurately predict the tradeoffs between important design parameters, such as power and frequency.

## VI. Conclusion

A new equation for the oscillation frequency of a ring oscillator has been presented. The derivation of the equation used a method that does not find the delay of each stage, but instead finds expressions for currents in the delay stage and reduces the system to an equation in which the only unknown is the frequency. The equation accounts for time-varying parasitics and for the gate resistance of the source-coupled pair. The effect of the gate resistance increases as higher frequencies and its inclusion quantifies the nonlinear relationship between the tail current and the oscillation frequency viewed in practice. The equation can be used to quantify the effects of layout dependant design parameters such as the gate resistance and drain–bulk capacitance. The derived equation has an average error of 8% over a wide range of parameter variations when compared to experimental data.

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