Transactions Briefs

A Method to Derive an Equation for the Oscillation Frequency of a Ring Oscillator

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***Abstract*—A new method for deriving an equation for the oscillation frequency of a ring oscillator is proposed. The method is general enough to be used for a variety of types of delay stages. Furthermore, it provides a framework to include various parasitic and secondary effects. The method is used to derive an equation for a common ring oscillator topology. The validity of the method and the resulting equation have been verified through simulation. The oscillation frequencies predicted by the proposed method are more accurate than existing equations and account for more secondary effects.**

***Index Terms*—CMOS analog integrated circuits, equations, high-speed integrated circuits, voltage-controlled oscillators.**

I. Introduction

The ring oscillator (RO) is a commonly investigated circuit due to its use in phase-locked loops (PLLs) and clock and data recovery circuits [1]–[7]. Despite its widespread usage, the RO still poses difficulties when it comes to analysis and modeling. Its design involves many tradeoffs in terms of speed, power, area and application domain. For the designer to make informed decisions regarding these tradeoffs, an accurate method to predict the frequency of oscillation of the RO is necessary.

Several equations exist to predict the frequency of oscillation of an RO [8]–[10]. These equations differ due to varying assumptions and simplifications made in their derivations. An accurate prediction of the frequency of oscillation is important for various reasons. It reduces the design time by making hand calculations more closely reflect the simulations. Moreover, the circuit element parameters in the equation can show the designer what tradeoffs are possible, and the process parameter components of the equation can be used to determine the limits of the RO for a given technology.

This brief discusses a new method to derive an equation for the oscillation frequency of a RO. The method results in a closed form, analytical equation. Furthermore, parasitic and secondary effects can be modeled that were ignored in other derivations. In this brief, Section II discusses existing equations and assumptions used to predict the oscillation frequency of an RO. Section III describes the methodology proposed in this brief to derive an equation for the frequency of oscillation. Section IV will illustrate how additional effects such as time-varying resistances and capacitances can be incorporated in the equation for more accurate results. Section V compares simulation results with the values predicted by the equations.

II. Existing RO Frequency Equations

An RO is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a dc inversion [11]. This means that for an oscillator with single-ended delay stages, an odd number of stages is necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped. Examples of these two circuits are shown in Fig. 1.

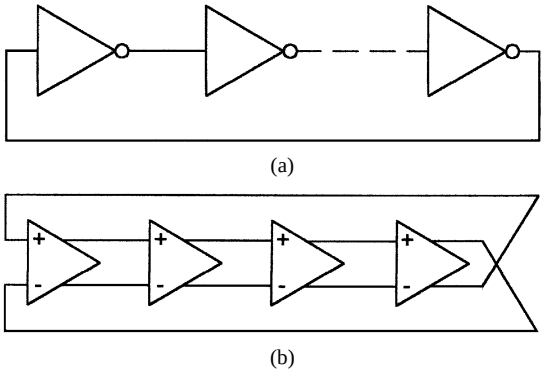

Fig. 1. (a) Single-ended RO. (b) Differential RO.

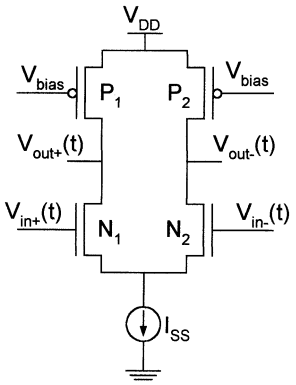

Fig. 2. Delay stage.

The most common way to derive an equation for the frequency of oscillation of the ring is to assume that each stage provides a delay of t_d. The signal must go through each of the N delay stages once to provide the first π phase shift in a time of $N \cdot t_d$. Then, the signal must go through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2N \cdot t_d$. Therefore, the frequency of oscillation is

$$f = \frac{1}{2N \cdot t_d}. \tag{1}$$

The difficulty in obtaining a value for the frequency arises when trying to determine t_d, mainly due to the nonlinearities and parasitics of the circuit. This brief will focus on differential delay stages, such as the one shown in Fig. 2. Even with a circuit that appears as simple as this one, many assumptions and simplifications are necessary to obtain a value for t_d. Therefore, numerous equations exist for determining the oscillation frequency of an RO, each derived with a separate set of assumptions and simplifications. Most of these derivations use a common set of parameters, which are listed in Table I.

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TABLE I
DELAY STAGE PARAMETERS

I_{SS}	Tail current used in the delay stage
V_{sw}	Peak to peak amplitude of the voltage waveform
N	Number of delay stages in the RO
t_d	Delay of each stage in the RO
R_L	Load resistance of the delay stage
C_L	Load capacitance of the delay stage

Reference [8] assumes that one stage initiates switching when the differential voltage of the previous stage crosses zero. As a result, the delay per stage is defined as the total change in differential output voltage at the midpoint of the transition, $V_{\rm SW}$, divided by the differential slew rate, $I_{\rm SS}/C_L$, resulting in a delay per stage of $C_L V_{\rm SW}/I_{\rm SS}$. Using this definition and (1), the oscillation frequency is given by (2)

$$f = \frac{I_{\rm SS}}{2NC_L V_{\rm SW}}. \tag{2}$$

A different method is used in [9], which models the delay stage as an RC circuit. In this case, the PMOS load is assumed to be biased in the linear region, acting as a resistor. Using (3), with $V_{\rm out}$(initial) as $V_{\rm DD}$ and $V_{\rm out}$(final) as $V_{\rm DD} - V_{\rm SW}$, t_d is found to be $R_L C_L \ln(2)$. Hence, the frequency is given by (4)

$$V_{\rm out}(t) = V_{\rm out}(\text{final}) + [V_{\rm out}(\text{initial}) - V_{\rm out}(\text{final})] \times \exp\left(\frac{-t}{RC}\right) \tag{3}$$

$$f = \frac{1}{2NR_L C_L \cdot \ln 2}. \tag{4}$$

A more accurate method is used in [10], which assumes a ramp input to find the ratio of delay to RC time constant to obtain (5), shown at the bottom of the page. The transistor capacitances in (5) correspond to the transistors labeled in Fig. 2.

III. EXPLANATION OF NEW TECHNIQUE TO DERIVE AN EQUATION FOR THE RO FREQUENCY

The method presented in this brief differs from others in that it does not try to find an expression for t_d. Instead, the method is based upon forming equations where the only unknown is the oscillation frequency. The key assumption made in this method is that the voltage waveform is sinusoidal. Although the output of an RO will not be purely sinusoidal, the frequency domain representation of a practical RO output shows that it is a reasonable assumption [5], [12]. Also, the error due to this assumption is small based on the accuracy of the results given in Section V. Once this assumption is made, equations for the currents and voltages throughout the circuit can be made as a function of the unknown frequency. Then, Kirchhoff's Current Law (KCL), which states that the sum of all currents entering a node is zero, can be used to create an equation which can be solved to determine an analytical equation for the frequency. This technique is illustrated with an example. The example is formatted such that each step is stated for the general case, then details are given that apply to this specific example. For this example, the circuit in Fig. 2 is used as the delay stage [13]. This topology consists of a source coupled pair with PMOS loads biased in the linear region.

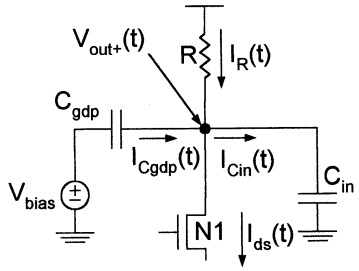

Fig. 3. Definition of currents for KCL.

Step 1: Define the Input Waveform as a Sinusoid With Unknown Frequency, f: For a delay such as that shown in Fig. 2, the tail current, $I_{\rm SS}$, will switch between N_1 and N_2. When all the current is through N_2, $V_{\rm out+}$ will rise to $V_{\rm DD}$, as there is no voltage drop across P_1. When all the current is through N_1, there will be a voltage drop of $V_{\rm SW}$ across P_1, and therefore $V_{\rm out+}$ will be $V_{\rm DD} - V_{\rm SW}$. This output voltage is the input voltage to the next stage. Therefore, the expression for the input voltage waveform will be a sinusoid with a maximum value of $V_{\rm DD}$ and a minimum value of $V_{\rm DD} - V_{\rm SW}$. The expression in (6) for $V_{\rm in+}(t)$ meets these criteria

$$V_{\rm in+}(t) = V_{\rm DD} - \frac{V_{\rm SW}}{2}(1 - \sin(2\pi f t)). \tag{6}$$

Step 2: The Output Waveform Must be Defined as a Phase Shifted Version of the Input Waveform: As stated in Section II, each stage must provide a phase shift of π/N radians. However, because $V_{\rm out+}(t)$ is on the same half circuit as $V_{\rm in+}(t)$, there is also a phase inversion. Note that as $V_{\rm in+}(t)$ increases, more current is steered through P_1, which acts as a resistor, and therefore $V_{\rm out+}(t)$ drops. Therefore, the total phase shift from $V_{\rm in+}(t)$ to $V_{\rm out+}(t)$ is $\pi/N + \pi$, or $\pi(1 + 1/N)$ radians, resulting in the expression for $V_{\rm out+}(t)$ in the following:

$$V_{\rm out+}(t) = V_{\rm DD} - \frac{V_{\rm SW}}{2}\left(1 - \sin\left(2\pi f t - \pi\left(1 + \frac{1}{N}\right)\right)\right). \tag{7}$$

Step 3: The Currents Flowing in and Out of the Output Node Must Be Defined in Terms of the Voltages Defined in Steps 1 and 2: By defining the voltages as in steps 1 and 2, equations for the currents shown in Fig. 3 can be found. Here, R is the equivalent resistance of the PMOS load, $C_{\rm gdp}$ is the gate-drain capacitance of the PMOS load, and $C_{\rm in}$ is the input capacitance of the next delay stage. These values will be further explained in this section.

To facilitate the explanation of this method, the first example will make many simplifications. This will result in a simpler, but also less accurate, expression for the oscillation frequency. Many of these simplifications will be removed in Section IV. First, it will be assumed that the resistance of the PMOS load in the linear region is constant. Therefore, the current flowing through this resistance is given by

$$I_R(t) = \frac{V_{\rm DD} - V_{\rm out}(t)}{R}. \tag{8}$$

Because P_1 and P_2 are in the linear region, the gate to drain capacitance, $C_{\rm gdp}$, becomes relevant. $C_{\rm gdp}$ is equal to $(1/2)WLC_{\rm ox}$ of the PMOS transistor. The current necessary to charge and discharge $C_{\rm gdp}$ is given as

$$I_{\rm Cgdp}(t) = C_{\rm gdp} \cdot \frac{d}{dt}\left(V_{\rm bias} - V_{\rm out+}(t)\right). \tag{9}$$

$$f = \frac{1}{2N(0.8)R \cdot (C_{GD(N1)} + C_{DB(N1)} + C_{GD(P1)} + C_{DB(P1)} + C_{\rm in})}. \tag{5}$$

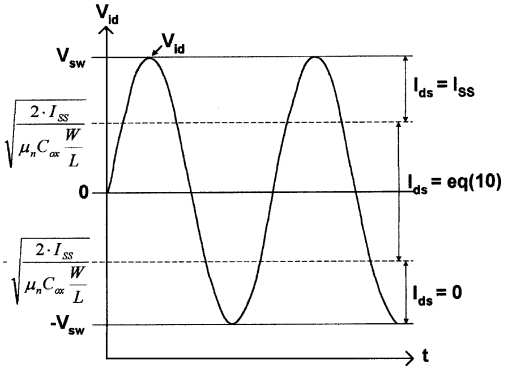

Fig. 4. Expression for I_{ds} depends on V_{id}.

Some difficulty arises in determining the drain current in the differential pair transistors, I_{ds}. As derived in [14], the drain current, I_{ds} is

$$I_{ds}(t) = \frac{I_{\rm SS}}{2} + \frac{\mu_n C_{\rm ox}\frac{W}{L}V_{id}(t)}{4}\sqrt{\frac{4\cdot I_{\rm SS}}{\mu_n C_{\rm ox}\frac{W}{L}} - V_{id}^2(t)} \qquad (10)$$

where $V_{id}(t) = V_{\rm in+}(t) - V_{\rm in-}(t)$.

As the magnitude of V_{id} becomes large, it is possible that all of $I_{\rm SS}$ will be directed through only one of N_1 or N_2, making (10) invalid. The range in which (10) is valid is

$$-\sqrt{\frac{2\cdot I_{\rm SS}}{\mu_n C_{\rm ox}\frac{W}{L}}} \le V_{id}(t) \le \sqrt{\frac{2\cdot I_{\rm SS}}{\mu_n C_{\rm ox}\frac{W}{L}}}. \qquad (11)$$

When V_{id} equals the left-hand side of the relation in (11), all of $I_{\rm SS}$ is flowing through N_2, and any decrease in V_{id} cannot increase the current through N_2. Conversely, once V_{id} equals the right-hand side of this relation, all of $I_{\rm SS}$ is flowing through N_1, and any increase in V_{id} cannot increase the current flowing through N_1. This range will become important in subsequent steps. This range can be easier to visualize using Fig. 4. Note the voltage lines showing where V_{id} crosses over the ranges defined in (11). On the right-hand side of the diagram, the value for I_{ds} through N_1 is shown for each region.

Step 4: Define the Capacitance Between the Output of One Stage and the Input of the Next, as Well as the Current Needed to Charge This Capacitance: For the delay stage used in this example, the capacitance at the output of the delay stage is defined as $C_{\rm in}$, and the current charging this capacitance is defined as $I_{\rm Cin}(t)$, as shown in Fig. 3. $C_{\rm in}$ is the gate capacitance of the source-coupled transistor of the next stage plus and is approximately $(2/3)WLC_{\rm ox}$.

Step 5: Use KCL to Find $I_{\rm Cin}(t)$ From Step 4 in Terms of the Currents Defined in Step 3: The current charging up the next stage is called $I_{\rm Cin}(t)$. Using KCL and the currents shown in Fig. 3

$$I_{\rm Cin}(t) = I_R(t) + I_{\rm Cgdp}(t) - I_{ds}(t). \qquad (12)$$

Step 6: Create an Equation Relating the Change in Voltage on the Output Capacitance in Terms of the Charging Current (Both Defined in Step 4): Using the current-voltage relation for a capacitor

$$C_{\rm in}\cdot(V_{\rm out+}(t_{n+1}) - V_{\rm out+}(t_n)) = \int_{t_n}^{t_{n+1}} I_{\rm Cin}(t)dt. \qquad (13)$$

Step 7: Determine the Time Ranges to Be Used in Step 6: To determine the frequency, (13) must be evaluated over one full period. However, note that if the integral is done for a full period, (13) will become $0 = 0$, as both sides contain periodic functions. Therefore, the period must be divided into sections in which $V_{\rm out+}(t)$ is monotonic, and the expressions from each section must be averaged to obtain a final expression. To determine the time and voltage values to be inserted into (13), a plot of the input and output voltage waveforms, such as Fig. 5, should be used. The time range of interest begins when $V_{\rm out+}$ passes through the midswing point, $V_{\rm DD} - V_{\rm SW}/2$, at t_0, and continues for one full cycle until t_4. There are four separate sections of interest labeled on Fig. 5 for which $V_{\rm out+}$ is monotonic, each corresponding to a quarter period. For each of these sections, the value to be substituted into (13) for $(V_{\rm out+}(t_{n+1}) - V_{\rm out+}(t_n))$ is either $V_{\rm SW}/2$ or $-V_{\rm SW}/2$. The other important times are when V_{id} crosses the ranges determined in step 3. These crossings mean a different expression must be substituted for I_{ds}, as shown on the right-hand side of Fig. 5. These times are labeled as t_{1a}, t_{1b}, t_{3a}, and t_{3b}

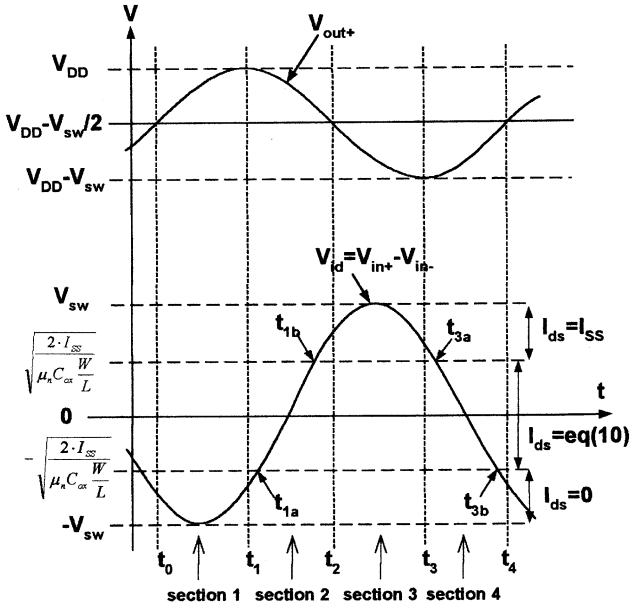

Fig. 5. Figure to determine limits of integration.

Step 8: Substitute the Values From Steps 1 to 7 Into the Equation Determined in Step 6 and Solve for the Frequency: For each section labeled in Fig. 5, (6)–(10) and (12) should be substituted into (13). To demonstrate this, equations for the first two sections will be shown. For Section I, between t_0 and t_1 in Fig. 5, V_{id} is below the bottom threshold line, meaning that for the entire time period, no current is flowing through N_1. Therefore, for this segment, $I_{ds} = 0$. Using (12) and (13)

$$C_{\rm in}\cdot\frac{V_{\rm SW}}{2} = \int_{t0}^{t1}(I_R(t) + I_{\rm Cgdp}(t))dt. \qquad (14)$$

After substituting in the appropriate expressions for $I_R(t)$ and $I_{\rm Cgdp}(t)$, ((8) and (9) respectively) the only unknown becomes the frequency, f. Therefore, solving for f gives

$$f_1 = \frac{1}{4}\cdot\frac{\pi - 2}{\pi\cdot R\cdot(C_{\rm in} + C_{\rm gdp})}. \qquad (15)$$

We have completed Section I and now move onto Section II. For Section II, there are two additional times labeled between t_1 and t_2. These times, t_{1a} and t_{1b}, correspond to times when V_{id} crosses the threshold values corresponding to a new range in the relation given in (11). These threshold crossings mean that the equation giving I_{ds} becomes piecewise. From time t_1 to t_{1a}, $I_{ds} = 0$. From time t_{1a} to t_{1b}, I_{ds} is given by (10). From time t_{1b} to t_2, $I_{ds} = I_{\rm SS}$. Therefore, substituting (6)–(12) and these time values into (13) results in

$$C_{\rm in}\cdot\frac{-V_{\rm SW}}{2} = \int_{t1}^{t2}(I_R(t) + I_{\rm Cgdp}(t))dt + \int_{t1}^{t1a}(0)dt + \int_{t1a}^{t1b}(I_{ds}(t))dt + \int_{t1b}^{t2}(I_{\rm SS})dt. \qquad (16)$$

TABLE II
HSPICE PARAMETERS

Cj	Zero-bias area junction capacitance
Cjsw	Zero-bias sidewall junction capacitance
Cgdo	Gate-drain overlap capacitance
pb	*p-n* junction potential
pbsw	*p-n* junction sidewall potential
mj	Area junction grading coefficient
mjsw	Sidewall junction grading coefficient
Ad	Drain area
Pd	Drain perimeter

Again, the only unknown in (16), after substitution, is the frequency, and solving for f gives

$$f_2 = \frac{1}{4} \cdot \frac{V_{\rm SW} N(2-\pi) + 4\pi I_{\rm SS} R}{\pi N V_{\rm SW} R(C_{\rm in} + C_{\rm gdp})}. \tag{17}$$

The same method can be used for Sections III and IV to find f_3 and f_4, respectively.

Step 8: Calculate the Overall Frequency Equation by Averaging the Four Values Obtained in Step 7: Now that four separate frequency expressions have been found, these expressions can be used to determine an equation for the frequency of oscillation of the RO. To do this, average the four values obtained in Step 7. In this case, the frequency becomes

$$f_{\rm ave} = \frac{I_{\rm SS}}{2 \cdot N \cdot V_{\rm SW} \cdot (C_{\rm in} + C_{\rm gdp})}. \tag{18}$$

Note that this equation is equivalent to (2), suggesting some validity to this method. Simulation results and a more accurate equation derived later also reinforce the validity of the method proposed here. Also, note that due to the symmetry of the differential delay stage, (18) can be found by averaging only f_1 and f_2.

Equation (18) shows that the frequency is directly proportional to the tail current and is inversely proportional to the number of delay stages, the voltage swing and to the parasitic and load capacitances.

IV. ADDITION OF PARASITIC AND SECONDARY EFFECTS

As mentioned, equations in Section III are based on several simplifying assumptions. In this section, we will remove some of these assumptions to develop a more accurate expression for the frequency. One of the benefits of the proposed method is that the designer can determine which parasitic and secondary effects should be included in the frequency derivation. The parasitics introduced in this section use some hspice parameters, which are shown in Table II.

The equations use an "n" or "p" following these parameters to refer to the NMOS or PMOS parameter, respectively. For example, Cj_p refers to the zero-bias area junction capacitance of a PMOS transistor.

The derivation for (18) assumes that the equivalent resistance of the PMOS load is constant. In reality this resistance is a function of V_{ds}. Since V_{ds} is a function of time, this resistance is also a function of time. The general equation for the transistor resistance in the linear region is given as

$$R = \frac{1}{\left[\mu_p C_{\rm ox} \frac{W}{L}(|V_{gs}| - |V_{tp}| - |V_{ds}|)\right]}. \tag{19}$$

For the circuit in Fig. 2, $|V_{gs}| = V_{\rm DD} - V_{\rm bias}$ and $|V_{ds}| = V_{\rm DD} - V_{\rm out+}(t)$. Making these substitutions in (19) gives (20), an expression for the PMOS load resistance as a function of time we get

$$R(t) = \frac{1}{\left[\mu_p C_{\rm ox} \frac{W}{L}(V_{\rm DD} - V_{\rm bias} - |V_{tp}| - (V_{\rm DD} - V_{\rm out+}(t)))\right]}. \tag{20}$$

In the derivation of (18), we also ignored the drain-bulk capacitances of all four transistors shown in Fig. 2. These capacitances are a function of the drain voltage. Since the drain voltage varies with time, these capacitances are also a function of time. The expression for this capacitance is given in the following [15]:

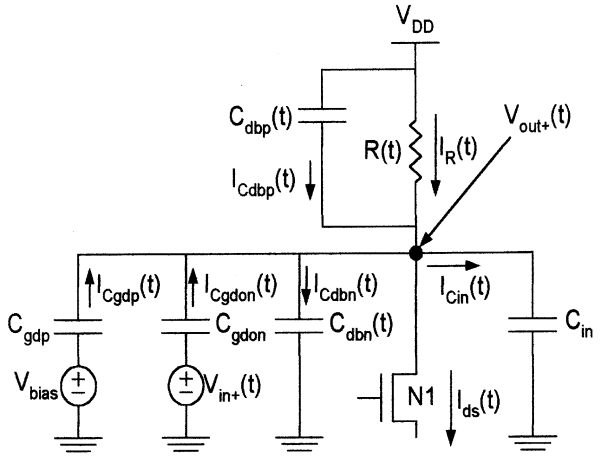

Fig. 6. KCL including additional effects.

$$C_{db}(t) = \frac{Cj \cdot Ad}{\left(1 + \frac{V_{db}(t)}{pb}\right)^{mj}} + \frac{Cjsw \cdot Pd}{\left(1 + \frac{V_{db}(t)}{pbsw}\right)^{mjsw}}. \tag{21}$$

For the differential pair, the drain voltage is $V_{\rm out+}(t)$ and the bulk voltage is ground, meaning that $V_{db}(t)$ is equal to $V_{\rm out+}(t)$. For the PMOS load, the drain voltage is $V_{\rm out+}(t)$ and the bulk voltage is $V_{\rm DD}$, meaning that $V_{db}(t)$ is equal to $V_{\rm out+}(t) - V_{\rm DD}$.

A third simplification made in the derivation of (18) is that the gate-drain overlap capacitance of the differential pair transistors was ignored. This capacitance is given in (22). The voltages on both nodes of this capacitance are time varying, with the gate voltage being $V_{\rm in+}(t)$ and the drain voltage being $V_{\rm out+}(t)$. Since both node voltages are time varying, the contribution of this capacitance with respect to the oscillation frequency becomes difficult to determine. Since these voltages are predefined as $V_{\rm in+}(t)$ and $V_{\rm out+}(t)$, the proposed method is able to determine their contribution

$$C_{\rm gdovn} = W_n \cdot C_{\rm gdon}. \tag{22}$$

At this point, we have removed three of the assumptions made in Section III. We have made the equivalent resistance of the PMOS load a time-varying function of V_{ds}. We have included the drain-bulk capacitances of all four transistors shown in Fig. 2. Furthermore, we have also included the gate-drain overlap capacitance of the differential pair transistors. Note that, for a time-varying capacitor, the following must be used to determine the current :

$$I(t) = C(t) \cdot \frac{dV(t)}{dt} + \frac{dC(t)}{dt} \cdot V(t). \tag{23}$$

If the capacitance is constant, $dC(t)/{\rm dt} = 0$, and (23) simplifies to

$$I(t) = C \cdot \frac{dV(t)}{dt}. \tag{24}$$

However, (23) will be used in this example to simplify the final expression, as it only affects the drain-bulk capacitances. These three additional effects and the related currents are shown in Fig. 6

We now have expressions for the resistance, the parasitic capacitances, and the related currents, all of which are time varying. To solve for the frequency, the method is identical to that described in Section III. The new time-varying expressions for all currents and parasitics must be substituted. Including these additional currents, the new KCL equation is given as

$$I_{\rm Cin}(t) = I_R(t) + I_{\rm Cgdp}(t) + I_{\rm Cgdovn}(t) - I_{\rm Cdbn}(t) + I_{\rm Cdbp}(t) - I_{ds}(t). \tag{25}$$

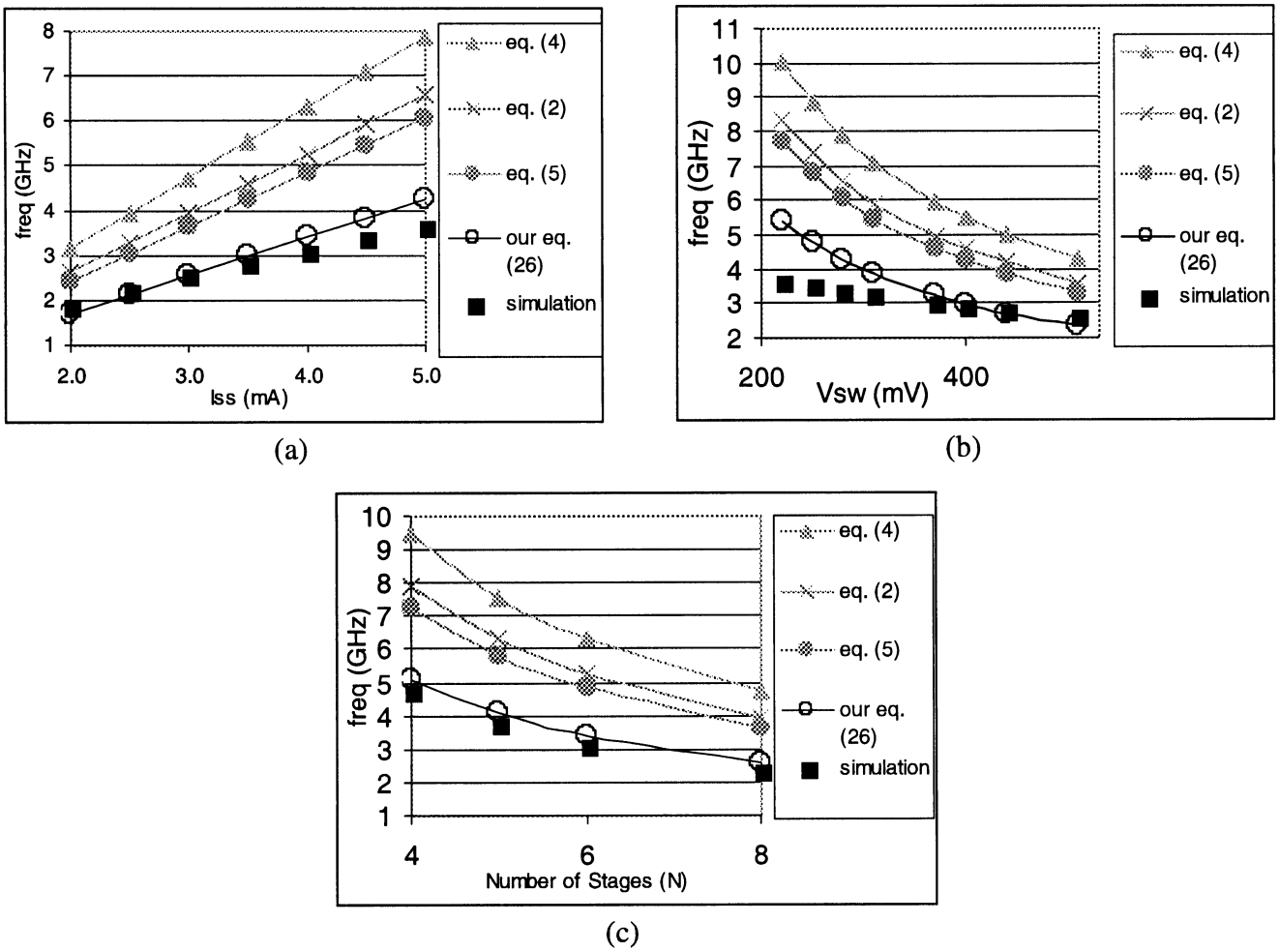

Fig. 7. Comparison of simulation and analytical results:(a) frequency versus $I_{\rm SS}$ (b) frequency versus $V_{\rm SW}$ (c) frequency versus N.

Following the steps outlined in Section III, and using the binomial expansion for simplification of the Cj and $Cjsw$ terms, the resulting equation for the frequency is given in (26), shown at the bottom of the page.The time-varying PMOS load resistance, $R(t)$, adds no additional terms in (26). This means that including the time-varying nature of the variable PMOS load resistance has no effect on frequency. However, the drain-bulk capacitances of the PMOS and NMOS transistors add to the denominator, and decrease the frequency. Moreover, the gate-drain overlap capacitance is multiplied by a factor of $1 + \cos(\pi/N)$. This factor is equivalent to showing the effect of the Miller capacitance at this node because the voltages at both nodes of the capacitor, $V_{\rm in+}(t)$ and $V_{\rm out+}(t)$, are moving in opposite directions. As N increases, the phase difference of these voltages approaches π and the value of $1 + \cos(\pi/N)$ approaches 2, resulting in a doubling of the gate-drain overlap capacitance.

At this point, we have shown that the proposed method, which results in (26), is able to incorporate additional parasitic and secondary effects. These time-varying parameters are easily included in the frequency equation. Note that this method can be used for modern scaled geometries, as all steps and equations are based on transistor and circuit equations. However, it is important to use equations that account for short channel effects, such as velocity saturation, for the current equations.

V. Simulation Versus Analytical Results

To determine the validity of the frequency equation derived here, (26), a test bench was created with ROs using the delay stage shown in Fig. 2. The simulations were done in a 1.8 V, 0.18-μm CMOS process. The transistor sizes were chosen such that the circuit would oscillate over a wide range of $I_{\rm ss}$ and $V_{\rm SW}$ values. ROs with different numbers of delay stages were also simulated to see how the frequency varied with N. Fig. 7 plots the simulated and analytical results predicted by (26) and other equations discussed in Section II. The frequency is plotted as a function of $I_{\rm SS}$, $V_{\rm SW}$, and N, respectively. As is evident from plots, (26) has the least error with respect to the simulated results. Equation (26) appears to be accurate for low $I_{\rm SS}$ and high $V_{\rm SW}$ values.

Different analytical equations are derived with varying assumptions. Therefore, when plotted, they predict different behavior. For example,

$$f := \frac{I_{\rm SS}}{2NV_{\rm SW}\left[C_{\rm in}+C_{\rm gdp}+\frac{Cj_nAd_n}{\left(1+\frac{V_{\rm DD}}{\rm pb_n}\right)^{\rm mjn}}+\frac{Cjsw_nPd_n}{\left(1+\frac{V_{\rm DD}}{\rm pbsw_n}\right)^{\rm mjswn}}+\left(1+\cos\left(\frac{\pi}{N}\right)\right)W_n{\rm Cgdo_n}+{\rm Cj_pAd_p}+{\rm Cjsw_pPd_p}\right]} \tag{26}$$

the difference between (26) and (2) is that (2) does not take into account the gate-drain overlap capacitance. Moreover, (2) does not let the designer know what values to use for the drain-bulk capacitances. Equation (4) has similar issues as (2). This equation also overestimates the frequency due to the ln (2) factor that arises from the assumptions made in the equation's derivation. Equation (5) contains the same parasitic capacitance values as (26) with the exception of the Miller effect on the overlap capacitance. Moreover, (5) also contains a 0.8 factor related to the equation derivation and seems to overestimate the frequency.

Although (26) results in a more accurate prediction of the frequency, it does not fully predict the trends in the changes in frequency with changes in parameter values. The relationship between frequency and the number of stages is accurate, but as Fig. 7(a) shows, the frequency is not directly proportional to $I_{\rm SS}$, as (26) suggests. The relative gains in frequency diminish as $I_{\rm SS}$ increases, suggesting a law of diminishing returns. Also, Fig. 7(b) shows that as $V_{\rm SW}$ becomes small, the inverse relationship suggested by (26) is not accurate. Therefore, further improvements need to be made to this equation. These improvements might be in the form of accounting for velocity saturation and RF effects.

VI. Conclusion

This brief has provided the framework for a new method to derive an analytical equation for the oscillation frequency of an RO. The method creates an equation where the only unknown is the frequency of oscillation. This is achieved by assuming a sinusoidal waveform. The method can account for many parasitics and secondary effects. The equation derived in this brief more accurately predicts the frequency than previous equations for a simulated RO.

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Flexible Multivariable Design Procedure for Optimum Operation of the Class-E Amplifier Using State Space Techniques

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***Abstract*—The Class-E amplifier is a highly efficient tuned switching power amplifier with a linear drain amplitude modulation characteristic ideally suited for high-efficiency amplifier systems (e.g., Kahn-amplifiers). This brief describes a design procedure to determine the circuit elements for optimum operation of the amplifier using state space methods. Finite feed inductance and quality factor of the resonant circuit are taken into account. It is shown that high efficiency can be sustained for a wide variety of element combinations, allowing relaxed demands on the output capacitance of the active device. This is especially useful for high-frequency amplifiers where the maximum operation frequency of a given device is often limited by its intrinsic drain–source capacitance.**

***Index Terms*—Class-E amplifier, design procedure, high efficiency, multiple element combinations.**

I. Introduction

Class-E amplification introduced by the Sokals [1] (Fig. 1) has been applied in RF generators, e.g., in lighting applications, or in high-efficiency amplification systems such as "Envelope Elimination and Restoration" [2], [3]. The frequency ranges from a few megahertz over personal communication systems (PCS) band applications [4], [5] to microwave dc–dc converters [6].

When properly designed, voltage and current will at no point of time be present simultaneously across the active device, thus eliminating, in theory, any loss of power. Boundary conditions for optimized operation of the Class-E amplifier are zero-drain voltage $U_{C_{\rm DS}}$ and zero slope of drain voltage at the time the switch turns on [1].

Several design procedures to obtain amplifier elements for optimum operation have been described. Earlier works [7], [8] derived solutions analytically assuming that the feed inductance $L_{\rm dc}$ and the quality factor Q_L of the series filter C_0 and L_0 be infinite. Both assumptions inhibit amplitude modulation of the amplifier, discarding the advantage of a linear-drain-modulation characteristic. The existence of solutions for finite feed inductance and quality factor has been proven in [9] using steady-state methods and was applied by Mandojana in [10].

This brief derives a description of the generalized Class-E amplifier based on [9] and [10] with some changes for computational efficiency.

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