A Method to Derive an Equation for the Oscillation Frequency of a Ring Oscillator

by

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Abstract

The voltage-controlled oscillator (VCO) is a commonly investigated circuit due to its use in phase-locked loops (PLLs) and clock and data recovery circuits (CDRs). A common VCO architecture is the ring oscillator. Despite its widespread usage, the ring oscillator still poses difficulties when it comes to design, analysis and modeling. The design of a ring oscillator involves many trade-offs in terms of speed, power, area and application domain. For the designer to make informed decisions regarding these trade-offs, an accurate method to determine the frequency of oscillation of the ring oscillator is necessary. One way to determine the oscillation frequency is to simulate the circuit using a numerical simulator, such as hspice. Although the oscillation frequency predicted may be accurate for the exact circuit simulated, there is no clear way for the designer to know how to improve the circuit. The designer does not know which circuit elements are controlling the oscillation frequency, and the effect design changes will have. The designer can find some basic trends by running hundreds of different simulations, but even then, the effect of each part of the circuit may not be clear.

An alternative method of design is to generate an analytical equation for the oscillation frequency of the VCO. An analytical equation will contain terms based on circuit and process parameters. The circuit parameters can show the designer what trade-offs are possible based on design changes such increasing the power dissipated. The process parameter components of the equation can be used to determine the limits of the VCO for a given technology. This can be very important if a high frequency VCO is required, or if the designer wishes to determine how the frequency limits of the VCO will change with scaling.

Several equations exist to predict the oscillation frequency of a ring oscillator based VCO. These equations differ due to varying assumptions and simplifications made in their derivations. As a result, their predictions vary, even for the same circuit. Also, the derivations are generally done making many assumptions that don't hold over wide parameter variations. In some cases, it is not clear what values to use for certain parameters, such as some parasitic capacitances, as they may be time-varying. Therefore, a general method to derive an analytical equation for the oscillation frequency of a ring oscillator is needed. This method should have the capability of including many parasitics and second order effects.

A new method to generate an analytical equation for the oscillation frequency of a ring oscillator will be described in this thesis. The majority of previous methods are based on finding the delay through each stage of the ring oscillator. This method differs in that it generates a system of equations which can be reduced to one equation where the only unknown is the frequency. Solving the equation will result in a closed-form analytical equation for the oscillation frequency. The new method will be described, and further explained with an example. Additional equations will be derived as more parasitic and secondary effects are included. The frequency limits of the example topology will also be determined. The results are verified through comparisons with measurements from a test chip.

Experimental results show that the equation derived using the proposed method predicts the oscillation frequency with an average error of 8% over a wide range of parameter variations. The results

also show that inclusion of the gate resistance in the model is very important in predicting high frequency operation. The proposed method allows the inclusion of the gate resistance of the differential pair in the oscillation frequency equation. The equations derived also show that the frequency reduction due to parasitic capacitances is higher than previously reported.

Acknowledgements

I would to thank my supervisor, Manoj Sachdev for make grad school a rewarding experience. His easy going demeanor has made working with him a pleasure, and the advice and experiences he shares are always much appreciated.

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Chapter 1

Introduction

1.1 Motivation

The voltage-controlled oscillator (VCO) is a commonly investigated circuit due to its use in phase-locked loops (PLLs) and clock and data recovery circuits (CDRs) [1]-[7]. The architecture of the VCO falls into two main categories: the ring oscillator and the LC oscillator. Although LC oscillators have superior phase noise performance compared to ring oscillators, ring oscillators still have numerous advantages. They generally require a relatively small area and can be more easily integrated with digital CMOS circuits, reducing cost. Also, they have a wider tuning range than LC oscillators, making them more robust over process and temperature variations. Despite its widespread usage, the ring oscillator still poses difficulties when it comes to design, analysis and modeling.

The design of a voltage-controlled oscillator involves many trade-offs in terms of speed, power, area and application domain. For the designer to make informed decisions regarding these trade-offs, an accurate method to determine the frequency of oscillation of the VCO is necessary. One way to determine the oscillation frequency is to simulate the circuit using a numerical simulator, such as hspice. Although the oscillation frequency predicted may be accurate for the exact circuit simulated, there is no clear way for the designer to know how to improve the circuit. The designer does not know which circuit elements are controlling the oscillation frequency, and the effect design changes will have. The designer can find some basic trends by running hundreds of different simulations, but even then, the effect of each part of the circuit may not be clear.

An alternative method of design is to generate an analytical equation for the oscillation frequency of the VCO. An analytical equation will contain terms based on circuit and process parameters. The circuit parameters can show the designer what trade-offs are possible based on design changes. The process parameter components of the equation can be used to determine the limits of the VCO for a given

technology. This can be very important if a VCO with a high oscillation frequency is required, or if the designer wishes to determine how the frequency limits of the VCO will change with scaling.

Several equations exist to predict the oscillation frequency of a ring oscillator [6], [8]-[11]. These equations differ due to varying assumptions and simplifications made in their derivations. As a result, their predictions vary, even for the same circuit. Also, the derivations are generally done making many assumptions that don't hold over wide parameter variations. In some cases, it is not clear what values to use for certain parameters, such as some parasitic capacitances, as they may be time-varying. Therefore, a general method to derive an analytical equation for the oscillation frequency of a ring oscillator is needed. This method should have the capability of including many second order effects and parasitics.

A new method to generate an analytical equation for the oscillation frequency of a ring oscillator will be described in this thesis. The majority of previous methods are based on finding the delay through each stage of the ring oscillator. This method differs in that it generates a system of equations which can be reduced to one equation where the only unknown is the frequency. Solving the equation will result in a closed-form analytical equation for the oscillation frequency. The new method will be described, and further explained with an example. Additional equations will be derived as more parasitic and secondary effects are included. The results are verified through comparison with oscillation frequency measurements from silicon. The frequency limits of the example topology will also be determined.

1.2 Contributions

The key contributions of this work are:

1. A new method to generate a closed form analytical equation for the oscillation frequency of a ring oscillator. The method can be used on a variety of delay stage topologies. The method can also account for parasitics, including time-varying parasitics, and second order effects. The extent to which these effects should be included can be decided upon by the designer.
2. Analytical equations for the oscillation frequency of a common ring oscillator topology have been generated using the proposed method. Each subsequent equation takes into account additional parasitics and secondary effects. The equations including the additional effects more closely predict the actual oscillation frequency than do existing equations. The highest order equation also accurately predicts trends in the oscillation frequency as a function of design parameters.
3. A test chip in a 0.18µm CMOS process to validate the proposed method and derived oscillation frequency equation.

1.3 Thesis Organization

Chapter 2 will discuss important concepts related to VCOs. It will discuss common application of VCOs. It will discuss the two main VCO architectures, which are LC oscillators and ring oscillators. It will discuss important VCO parameters such as phase noise and tuning range. The relative performance of LC and ring oscillators will then be compared with respect to these parameters. Chapter 3 introduces and describes the new method of generating an equation for the oscillation frequency. First, the steps are outlined. This is followed by a detailed example for a common ring oscillator topology. Chapter 4 expands on the example by showing how parasitic and secondary effects can be included. These include time-varying capacitances and RF effects, such as the gate resistance. The chapter will also show how the equations can be used to determine an expression for the maximum oscillation frequency of the ring oscillator. Chapter 5 compares the frequency measurements from the test chip with the frequencies predicted by the equations derived here. It also compares these results with existing equations. Chapter 6 will conclude this thesis.

Chapter 2

VCOs

2.1 Introduction

The voltage-controlled oscillator (VCO) is a commonly investigated circuit due to its use in phase-locked loops (PLLs) and clock and data recovery circuits (CDRs). The architecture of the VCO falls into two main categories: the ring oscillator and the LC oscillator. Although LC oscillators have superior phase noise performance compared to ring oscillators, ring oscillators still have numerous advantages. They generally require a relatively small area and can be more easily integrated with digital CMOS circuits, reducing cost. Also, they have a wider tuning range than LC oscillators, making them more robust over process and temperature variations.

The VCO is a useful circuit because its oscillation frequency can be set to a desired value. The governing equation for a VCO is given in (1).

$$f_{vco} = f_0 + K_{VCO} V_{ctrl} \tag{1}$$

In (1), f_0 is the center frequency of the VCO. It is the frequency at which it will oscillate with no external control. It is also referred to as the free-running frequency. K_{VCO} is the gain of the VCO that controls how much a change in control voltage will change the VCO's frequency. V_{ctrl} is the input to the VCO that sets it to the desired frequency. It is this tunability that makes the VCO such an important and useful circuit.

This chapter will discuss important background information regarding VCOs. It will describe some of the common applications of VCOs, focusing on the use of VCOs in phase-locked loops (PLLs). It will describe the two most common VCO architectures: LC oscillators and ring oscillators, as these two circuits oscillate based on very different principles. Important VCO parameters such as phase noise and tuning range will also be explained. These parameters must be considered when choosing a VCO architecture. The relative performance of LC and ring oscillators will then be compared with respect to these parameters.

2.2 Applications

One of the reasons the VCO is a commonly used circuit is because it is a key component of a PLL. A typical PLL is shown in Figure 1. The purpose of a PLL is to create an output signal which oscillates at the same frequency as the input signal. When the PLL is in lock, it works as follows: The phase detector produces an output whose dc value is proportional to the phase difference between the input signal and the VCO output. The loop filter is a low pass filter than attenuates the high frequency variations in the phase detector output so that the VCO input signal is dc. This dc input to the VCO then controls the oscillation frequency of the VCO so that its frequency is equal to that of the input signal.

Once in lock, the PLL tracks small changes in the input frequency. If the frequency of the input signal increases, the phase difference between the input signal and the VCO output will increase, which will increase the dc output of the phase detector and loop filter. Therefore, the input into the VCO will increase, and its frequency will increase to match the increase in the frequency of the input. It is possible that the VCO frequency will increase over the desired value and then decrease to the desired value, as the loop won't regain lock until the VCO frequency equals the input frequency and the static phase error has settled to its proper value [12].

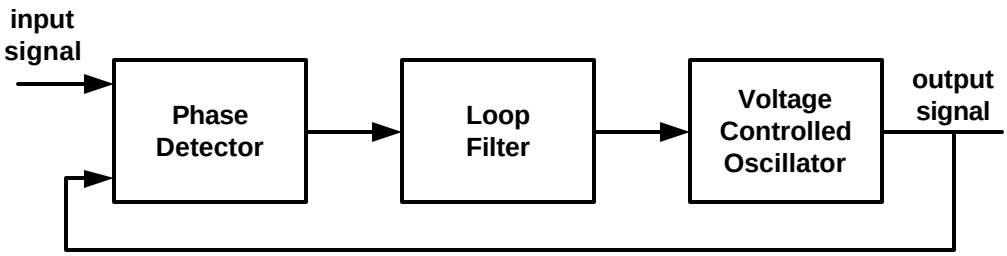


Figure 1: Block diagram of a phase-locked loop

A PLL can be used in a variety of applications, many of which are in the realm of communications. A PLL can be used in a clock and data recovery circuit, as shown in Figure 2 [13]. In such a system, the data is sent without a clock reference, and therefore the receiver must determine the frequency of the incoming data, and when to sample the data to recover it. The PLL can be used to determine the frequency of the incoming data and generate a clock at the same frequency at the VCO output. If there are small changes in the input frequency, the PLL can also track these changes so that it continues to optimally sample the data. For example, if the data input speeds up, the zero crossings of the data will lead those of the VCO, which will increase the control voltage to the VCO, which will increase its frequency to match that of the incoming data. The clock generated by the VCO and the data can both go into a decision circuit, which will use the generated clock to sample, and then determine the value of the data.

The properties of the VCO can have a large impact on the performance of the CDR system. One important characteristic of the VCO in this application is the tuning range, as it is crucial that the VCO

frequency can be varied to exactly equal the frequency of the incoming data. The phase noise generated by the VCO also has a large impact on the bit-error rare (BER) of the CDR system. The transfer function of the phase noise from the VCO to the output takes the form of a high-pass filter. Therefore, any fast changes in phase generated by the VCO will be transferred to the output. The phase noise can be reduced by increasing the loop bandwidth of the PLL. However, increasing the loop bandwidth will increase the phase noise transferred from the input to the output. Therefore, the designer must find a tradeoff between minimizing noise from the input and minimizing noise from the VCO.

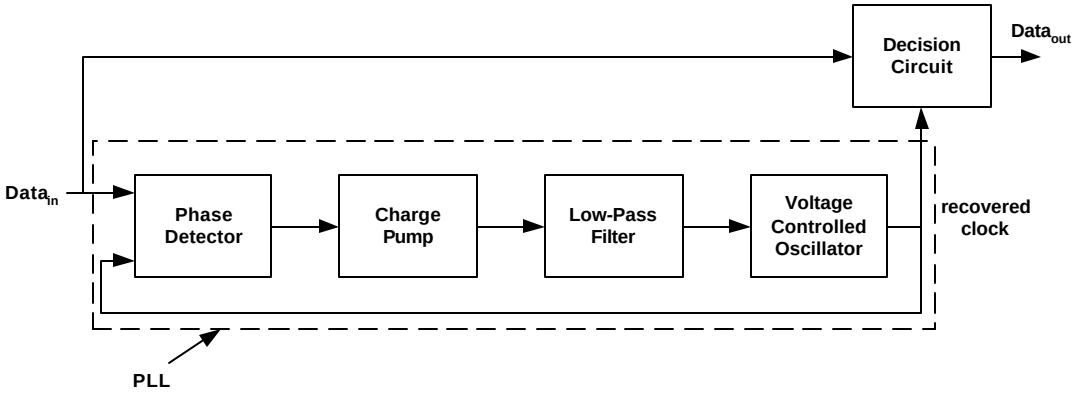


Figure 2: CDR architecture based on a PLL

A PLL can also be used in a frequency synthesizer, as shown in Figure 3. A frequency synthesizer can be used to generate an accurate local oscillator (LO) whose frequency can be changed in small steps to select different channels. This ability is required in many wireless receivers. In this circuit, a divider is used in the feedback path so that $f_{out}=N \bullet f_{ref}$. To see why $f_{out}=N \bullet f_{ref}$, note that the two phase detector inputs must be at the same frequency for the PLL to achieve lock. In this case, the two inputs are at frequencies f_{ref} and f_{out}/N. Therefore, $f_{out}=N \bullet f_{ref}$. In order to select a different channel, N can be changed. For example, in a DECT (Digital Enhanced Cordless Telecommunications) receiver, the VCO must be able to sweep from 1.884 GHz to 1.9 GHz and the channel spacing is 1.728 MHz. Therefore, if f_{ref} is set to the channel spacing of 1.728 MHz, different channels can be selected by varying N from 1090 to 1099 [10]. In a wireless system, the phase noise of the VCO is an important characteristic, as it can result in down-converting power from an adjacent channel into of the desired signal band. This is further explained in section 2.4.1.

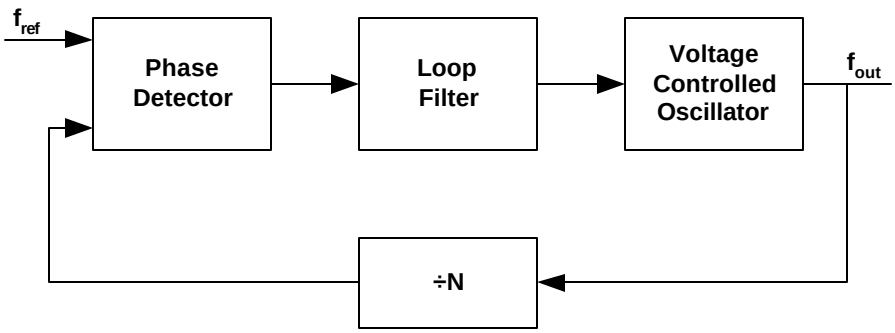


Figure 3: Block diagram of a frequency synthesizer

2.3 VCO Architectures

A key property of a VCO is that the output frequency is a linear function of the control voltage, as shown in (1). There are many circuits which can provide this behavior, most of which can be divided into two main architectures: the ring oscillator and the LC oscillator. These two architectures achieve oscillations based on very different principles, as will be described here.

2.3.1 Ring Oscillator

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a DC inversion [14].

The most basic ring oscillator is simply a chain of single ended digital inverters, with the output of the last stage fed back to the input of the first stage. This circuit is shown in Figure 4. Note that to provide the DC inversion, an odd number of stages must be used. To see why this circuit will oscillate, assume that the output of the first inverter is a '0'. Therefore, the output of the Nth inverter, where N is odd, must also be '0'. However, this output is also the input to the first inverter, so the first inverter's output must switch to a '1'. By the same logic, the output of the last inverter will eventually switch to a '1', switching the output of the first inverter back to '0'. This process will repeat indefinitely, resulting in the voltage at each node oscillating.

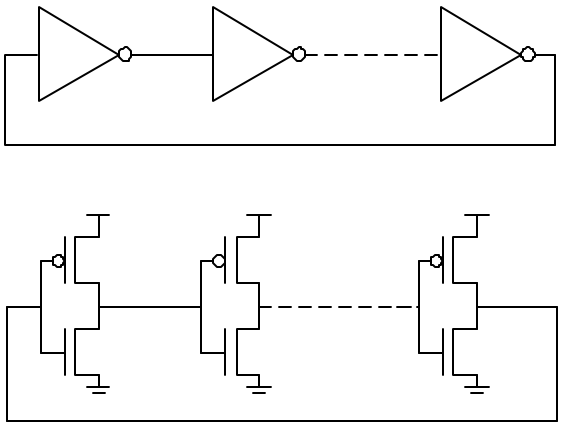


Figure 4: Ring Oscillator using Single Ended Inverters

To determine the frequency at which this circuit will oscillate, assume that the delay through each inverter is t_d. The signal must go through N inverters, each with delay t_d, for a total time of $N \cdot t_d$, to obtain the first π phase shift. Then, the signal must go through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2N \cdot t_d$. The frequency is the reciprocal of the period, resulting in the frequency shown in (2).

$$f = \frac{1}{2N \cdot t_d} \tag{2}$$

To make this circuit useful, the oscillation frequency must be controllable. As seen in (2), the only parameters that affect the frequency are the number of stages, N, and the delay per stage, t_d. It is difficult to implement a circuit that can vary the number of stages in the ring. Therefore, to make this oscillator voltage-controlled, t_d must be variable. One way to control the delay is to control the amount of current available to charge or discharge the capacitive load of each stage. This type of circuit is called a current starved inverter and is shown in Figure 5 [15]. The maximum charge and discharge current is now controlled by the current source of value I_{ref}. If V_{cont} is increased, I_{ref} increases, which in turn increases the current through M_3 and therefore reduces the time to discharge the load capacitance of the next stage. Since the current through M_4 mirrors the current through M_3, the charging time is also decreased. Therefore, an increase in V_{cont} reduces t_d and thereby increases the oscillation frequency.

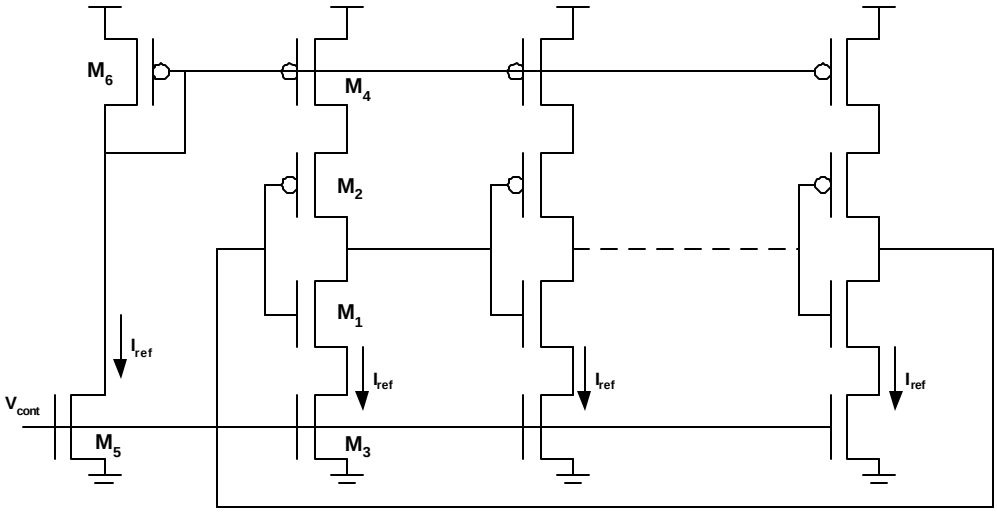


Figure 5: Current-Starved VCO

A single-ended VCO such as that in Figure 5 suffers from a large problem in that it is susceptible to common-mode noise. To alleviate this problem, many VCOs use a differential delay stage, as illustrated in Figure 6. Also note that a VCO using differential delay stages can have an even number of stages if the feedback lines are swapped.

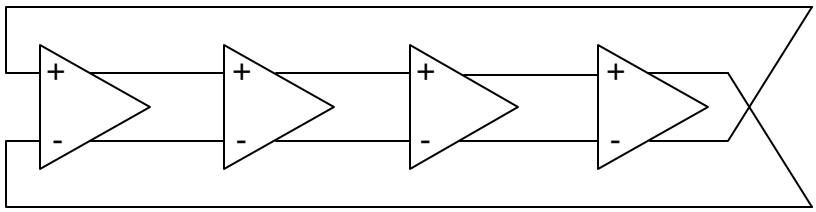


Figure 6: Ring Oscillator with Differential Delay Stages

A common topology for a differential ring oscillator involves a source-coupled pair driven by a current source and with a resistive load. An example of this circuit is shown in Figure 7. Assume that initially V_{in} is large and negative. This means that all of the current is flowing through M_2, so that there will be a voltage drop across the resistor, R_2. There is no current through M1, so there is no voltage drop across R_1. Therefore, V_{out} is positive. As V_{in} crosses zero in the positive direction, the current is switched from M_2 to M_1. The increased current through M_1 increases the voltage drop across the R_1, and the decreased current through M_2 decreases the voltage drop across R_2. As a result, V_{out} switches and becomes negative. Since V_{out} is connected to the input of the next stage, it switches also. As in the single-ended delay stage, if the feedback results in a DC inversion, and the gain of each stage is sufficient, the circuit will oscillate. To first order, the oscillation frequency of this ring oscillator is given in (3), where C_L is the

load seen at the output of a stage and V_{sw} is the peak to peak voltage swing of V_{in} and V_{out} [8]. Assuming the current fully switches, V_{sw} is equal to I_{SS}•R.

$$f = \frac{I_{SS}}{2N \cdot C_L V_{sw}} \tag{3}$$

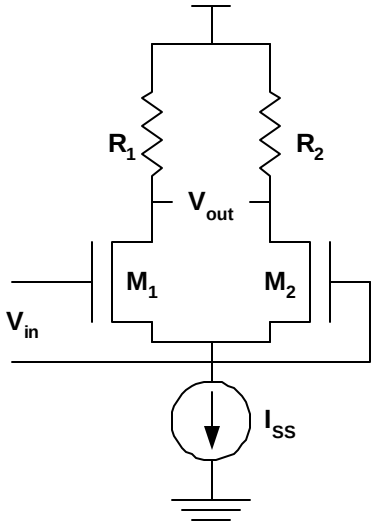


Figure 7: Differential delay stage

However, we would like to make the oscillation frequency voltage-controlled. The parameters that affect the frequency are given in (3). The number of stages and load capacitance are normally constant, which leaves I_{SS} and V_{sw} as possible variables. Note that if I_{SS} is increased, to first order, V_{sw} will increase proportionally and the frequency will remain constant. Also, it is often desirable to maintain a constant voltage swing during operation. It is problematic to have a variable swing because if the swing is small, the jitter will be increased, and if the swings are large, a higher supply voltage is needed for differential operation [16]. Therefore, a circuit is needed such that, if I_{SS} is varied, V_{sw} remains constant, and the frequency varies with I_{SS}. This can be accomplished with the circuit shown in Figure 8, which is based on [8] and [17].

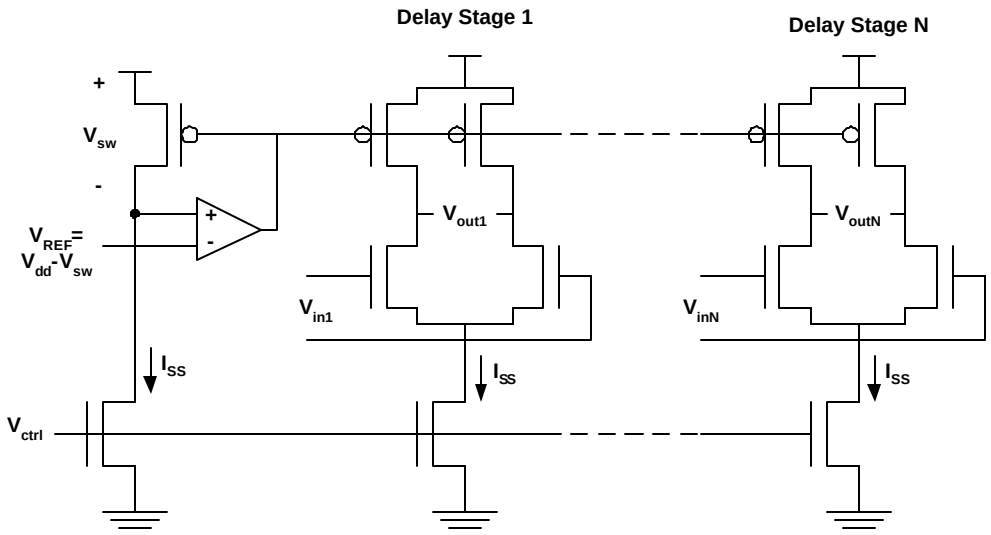


Figure 8: VCO with replica biasing

In the delay stage in Figure 8, the resistor is replaced with a PMOS transistor with a variable gate voltage, which acts similarly to a variable resistor. The resistance of a PMOS transistor operating in the linear region is given by (4). Note that the resistance can be changed by varying V_{gs}.

$$R = \frac{1}{\left[\mu_p C_{ox} \frac{W}{L}\left(\left|V_{gs}\right| - \left|V_{tp}\right| - \left|V_{ds}\right|\right)\right]} \tag{4}$$

The VCO works as follows. As shown in (3), the frequency will increase as the tail current increases. Therefore, to increase the frequency of the circuit in Figure 8, V_{ctrl} should be increased such that I_{SS} increases. However, this increased current through the linear PMOS load will increase the voltage swing. This will cause the non-inverting input of the opamp to drop, causing the output of the opamp to also drop. This will decrease the equivalent resistance of the PMOS load, reducing the swing. Due to the feedback loop, the opamp output voltage will decrease until the differential input voltage is zero. At this point, the PMOS bias voltage will be such that the voltage swing has returned to the desired level, set by V_{REF}. Therefore, the tail current increases and V_{sw} remains constant, meaning that the frequency will increase.

Another common method to control the frequency is through delay interpolation [18]. In this method, a fast path and a slow path are placed in parallel, and the total delay is a weighed sum of the two paths. The delay is changed with a differential control voltage, which increases the gain of one path and decreases the gain of the other. This is conceptually shown in Figure 9 [16]. A circuit based on this concept is shown in Figure 10 [7].

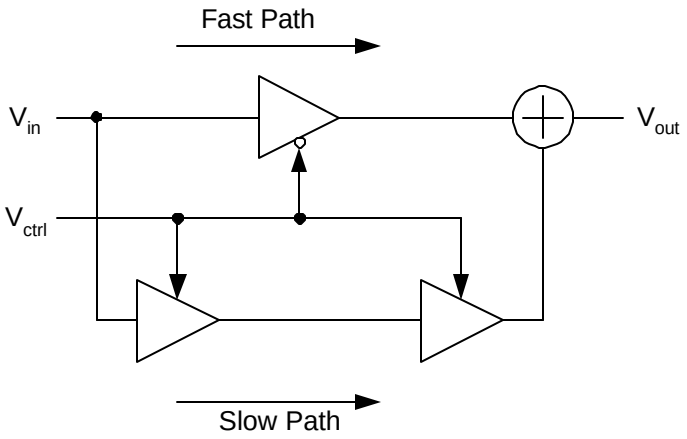


Figure 9: Delay Interpolation

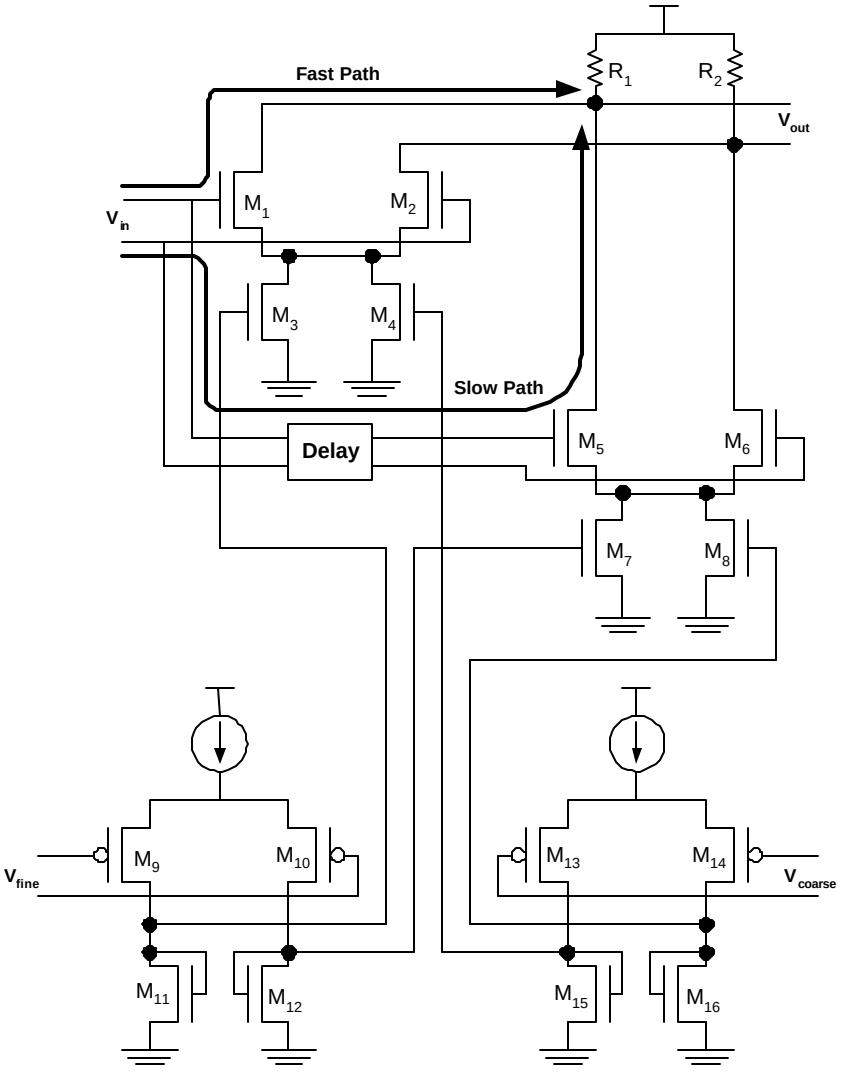


Figure 10: VCO with delay interpolation

Note that there are two control voltage in this circuit, V_{coarse} and V_{fine}. V_{coarse} will have a large VCO gain and its primary purpose is to make large adjustments to the frequency to account for process and temperature variations. V_{fine} will have a much smaller VCO gain and will be used to fine tune the VCO frequency once it has been set close to the desired value by V_{coarse}.

This circuit operates similarly to that of Figure 7, where M_1 and M_2 form the NMOS source-coupled pair with resistive loads R_1 and R_2. However, the delay of this circuit is controlled through delay interpolation. The fast path to the output is through M_1 and M_2 and the slow path is through the delay element and then M_5 and M_6. The gains of these two paths are controlled through V_{coarse} and V_{fine}. First, note that the gain of a resistively loaded source-coupled pair is g_mR [19]. Also note that g_m increases with increasing tail current, and therefore the gain of each stage can be controlled by controlling its tail current. The tail current through the fast path is mirrored from M_{11} and M_{15} and the tail current for the slow path is mirrored from M_{12} and M_{16}. If V_{coarse} increases, the current through M_4 will increase and increase the gain of the fast path. At the same time, the current through M_8 will decrease and decrease the gain of the slow path. Therefore, the oscillation frequency will increase.

2.3.2 LC Oscillators

LC Oscillators are based on the principle that for an ideal inductor and capacitor resonant tank, there exists a frequency at which the average energy stored in the inductor and capacitor are equal and the total losses in the circuit are zero. Under these conditions, the circuit can sustain oscillations. This can be shown for the parallel LC tank structure shown in Figure 11.

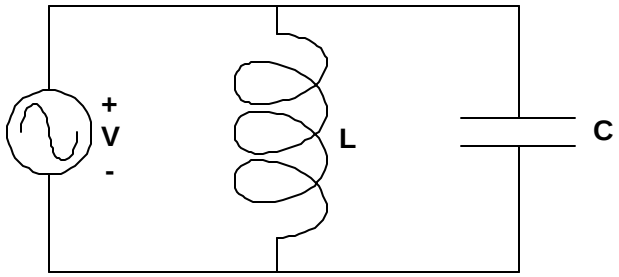


Figure 11: Parallel LC Circuit

The average magnetic energy stored in the inductor, W_m, is given by (5) and the average electric energy stored in the capacitor, W_e, is given by (6) [20].

$$W_m = \frac{1}{4}|V|^2 \frac{1}{\omega^2 L} \tag{5}$$

$$W_e = \frac{1}{4}|V|^2 C \tag{6}$$

Setting (5) and (6) equal and solving for ω gives (7), the oscillation frequency.

$$\omega = \frac{1}{\sqrt{LC}} \tag{7}$$

However, ideal inductors and capacitors are not physically realizable and thus there will always be a loss. This results in the equivalent circuit shown in Figure 12, where the loss is represented by the resistor, R. This loss will cause the oscillations to die out.

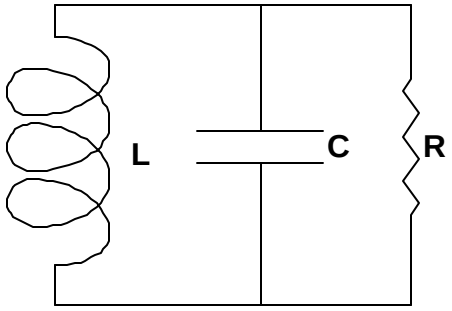


Figure 12: Parallel LC with losses

Therefore, an element with an equivalent negative resistance is needed to cancel out these losses so that oscillation can be sustained, as shown in Figure 13.

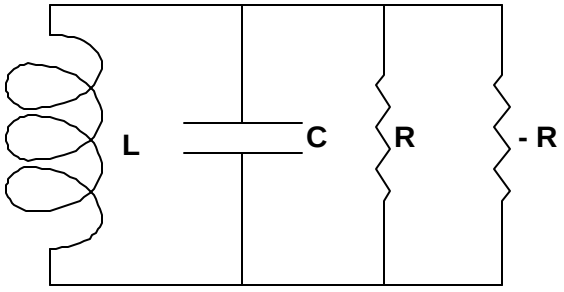


Figure 13: LC Oscillator with Negative resistance to cancel losses

In a monolithic LC oscillator, this negative resistance can be realized with the use of active devices. For example, the resistance seen between the two drains of a cross-coupled differential pair is -2/gm [13]. The circuit is shown in Figure 14. Note that the value of R should be less than $2/g_m$ to begin, and then sustain, oscillations.

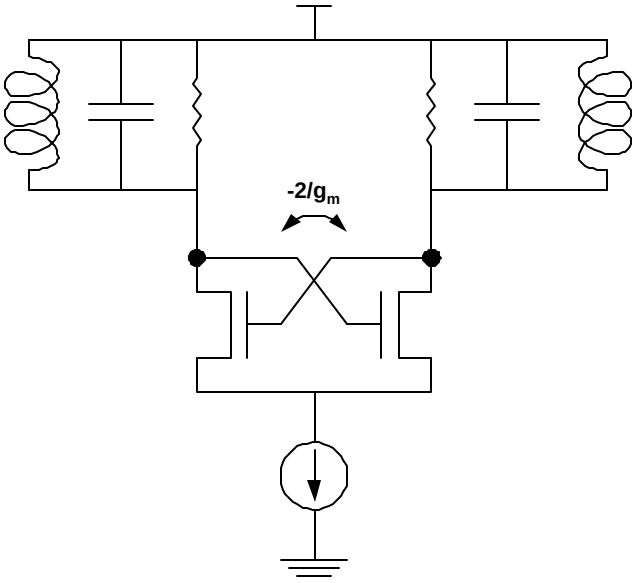


Figure 14: LC oscillator with active devices

Although this circuit will oscillate, to make it useful, the oscillation frequency must somehow be controlled. The frequency of oscillation is given by (7), where the only variables are L and C. The inductor will normally be implemented as a spiral inductor, and is not tunable. Therefore, a variable capacitance must be used. This can be implemented with a reverse biased pn-diode or a MOS varactor. In either case, the capacitance is varied by varying a voltage which varies the width of the space charge region, which varies the capacitance of the region. An LC tank VCO using a varactor is shown in Figure 15.

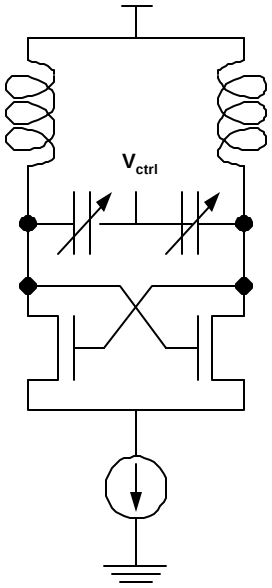


Figure 15: LC Tank VCO using varactors

2.4 Important VCO characteristics

When choosing a VCO architecture and topology, there are many important characteristics which must be taken into account. The relative importance of these characteristics usually depends on the target application. The characteristics can be placed into different categories. In the noise category, there are jitter and phase noise. In the frequency category, there are the tuning range, the maximum frequency and the predictability of the frequency over process and temperature variations. In the manufacturing category, there is the ease of integration with digital CMOS circuitry, and again, the effect of process variations.

2.4.1 Phase Noise and Jitter

One of the most important characteristics of a VCO is its phase noise in the frequency domain, which corresponds to jitter in the time domain. If the VCO is used in a wireless application, the phase noise can cause adjacent channels to be down-converted into the desired signal band. If the VCO is used to sample data, the jitter will affect the sample point and could degrade the signal-to-noise ratio (SNR).

The output of an ideal sinusoidal oscillator is of the form given in (8) where A is the amplitude, ω_0 is the oscillation frequency and ϕ is an arbitrary phase reference.

$$V_{out}(t) = A \cdot \cos(\omega_0 t + \phi) \tag{8}$$

However, the output of a practical oscillator will be of the form given in (9), where A(t) and $\phi(t)$ are now functions of time due to internal and external noise sources.

$$V_{out}(t) = A(t) \cdot \cos(\omega_0 t + \phi(t)) \tag{9}$$

The amplitude fluctuations will be significantly attenuated due to the amplitude limiting mechanism that is present is any practical stable oscillator, and can be neglected. This mechanism is particularly strong in ring oscillators [9]. Therefore, the only fluctuations are phase fluctuations, which correspond to the phase noise. A definition of phase noise, in dBc/Hz, is given in (10) and is illustrated in Figure 16. It is the ratio of the power in a 1 Hz bandwidth at an offset from the carrier of $\Delta\omega$, divided by the power of the carrier.

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1\ \text{Hz})}{P_{carrier}}\right] \tag{10}$$

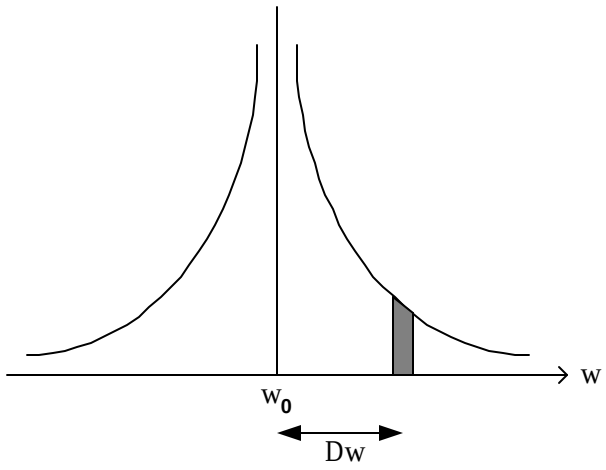


Figure 16: Illustration of Phase Noise

Phase noise can cause problems in wireless systems, as illustrated in Figure 17. It is desired to use a local oscillator (LO) to down-convert a signal. However, the LO is not ideal, and an adjacent channel is down-converted such that its skirts overlap the desired signal, causing significant interference.

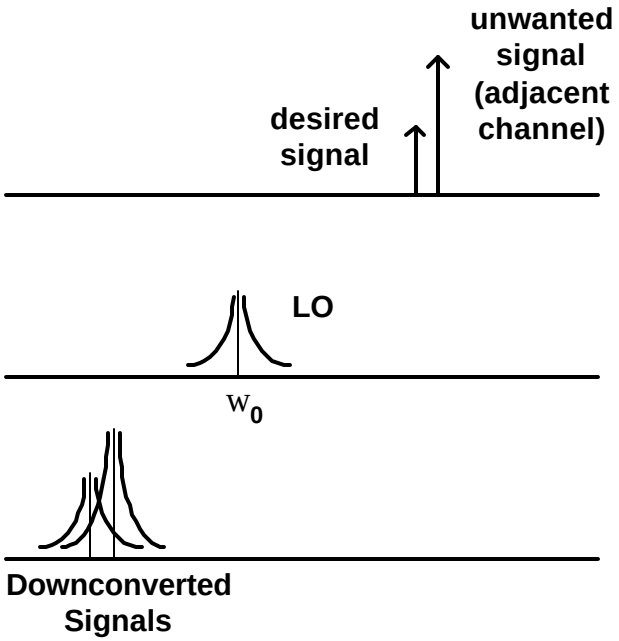


Figure 17: Effect of Phase Noise on Down Conversion

Phase noise in the frequency domain can be related to jitter in the time domain. Jitter is variations in the zero crossings of the signal, and is illustrated in Figure 18.

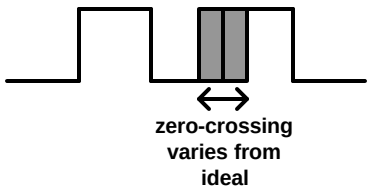


Figure 18: Jitter on a clock

One example of the effect of jitter is in a data recovery system, as illustrated in Figure 19. Jitter degrades the performance of this system in two ways. First, there will be jitter on the transmitter end, which is shown in the figure as data jitter. There will also be jitter on the sampling clock, which will be from the output of a VCO on the receiver end. The combined effect is that the sampling clock won't sample the data at the optimal point in the data eye, which will degrade the SNR, which will in turn degrade the BER.

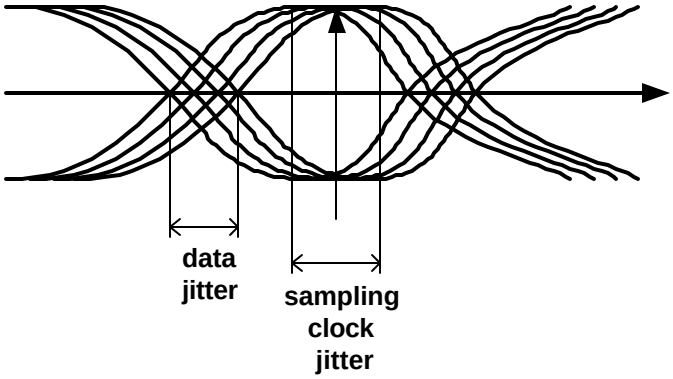


Figure 19: Effect of jitter on data recovery

2.4.2 Frequency Characteristics

The frequency related characteristics of a VCO are the tuning range, the maximum frequency and the predictability of the frequency over process and temperature variations. The tuning range of a VCO is the range that the oscillation frequency can be varied from its center frequency. For example, if a VCO with a center frequency of 1.9 GHz could be varied from 1.8 GHZ to 2.0 GHz, it would have a tuning range of 10.5%. The tuning range can be important for two reasons. The first is that if the VCO is to be used in a system which has a large possible range of incoming frequencies, the tuning range should encompass them. This might occur in a chip which is designed to work with multiple standards. The second reason tuning range is important is related to the predictability of the VCO. That is, how close the actual center frequency will be with respect to the designed center frequency, as it can vary substantially due to process

variations. Therefore, if the center frequency can vary substantially, a large tuning range is necessary so that the VCO will oscillate in the desired frequency range.

The maximum attainable frequency of a VCO architecture is also important in high speed systems. As internet traffic increases, it is desirable to increase the serial data rate. Therefore, high-speed VCOs are needed for data recovery circuits. The issue of VCO speed will be discussed further in section 2.5.2, comparing the maximum frequency of LC and ring oscillators.

2.4.3 Manufacturability

To reduce overall system cost and complexity, it in often desired to design an entire system, including analog and digital circuitry, on a single chip. Therefore, the ease with which the VCO can be integrated with other circuits is important. For example, the digital circuitry can create substrate and supply noise, so it is important that the VCO be able to reject this noise. Also, the physical size of the VCO is important, as a larger VCO will correspond to a larger die size, which will correspond to a higher cost.

2.5 Ring versus LC VCO

When choosing a VCO architecture, one must determine the specifications related to the VCO characteristics described above, and then decide whether a ring or LC VCO would better suit the application, as they each have their strengths and weaknesses.

2.5.1 Phase Noise

Phase noise is often the most important specification that must be met when choosing a VCO architecture. If excellent phase noise characteristics are required, an LC VCO will usually be necessary. Two of the main parameters related to phase noise are the attainable quality factor of the oscillator and the oscillator's ability to reject supply and substrate noise.

The quality factor, Q, of an oscillator is related to the loss of the circuit, and a common definition is given in (11).

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy dissipated per cycle}} \tag{11}$$

The relationship between Q and the phase noise is given in (12). This relationship shows that a higher Q reduces the phase noise.

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{2kT}{P_{sig}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{12}$$

An LC oscillator will have a higher Q than a ring oscillator. The reason can be seen by analyzing the energy storage and dissipation during a cycle. In an ideal LC oscillator, the energy will transfer between the inductive and capacitance elements with no loss, resulting in an infinite Q. In a practical LC oscillator, there are losses associated with each element, such as series resistance losses in the inductor, but energy still switches between the two reactive elements. However, in a ring oscillator, the energy is stored in the equivalent capacitance of the next stage, and the energy is fully charged and then discharged every cycle. As shown by the denominator of (11), this characteristic substantially reduces the Q. Typical Q values for a ring oscillator are about 1.3 to 1.4 [21]. The Q of an LC tank can be about an order of magnitude higher [22].

A second reason why ring oscillators have poor phase noise performance is seen by analyzing the oscillator as a time-varying system. The system is time-varying in that the effect of injected noise on phase depends on the point in the cycle at which the noise is injected [9]. This is shown in Figure 20 [9]. When the impulse is during the peak, there is an amplitude shift, but the phase remains the same. When the impulse is during the transition, there is a phase shift that persists over time. This is a problem in ring oscillators, because the device noise is the highest during transitions, which is the worst case scenario in terms of phase noise performance.

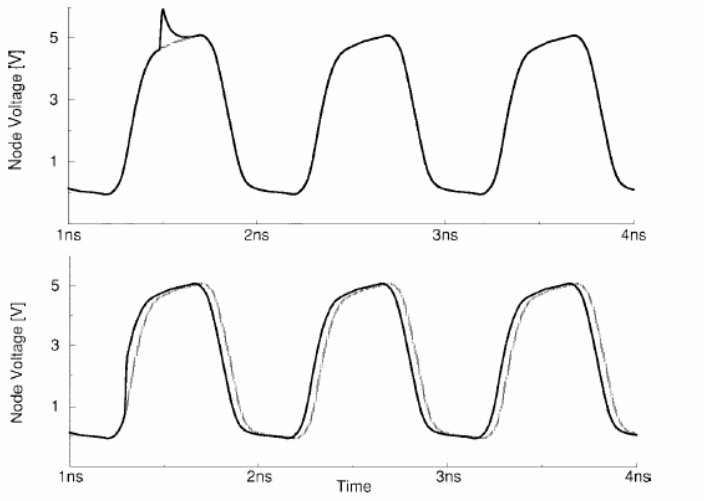


Figure 20: Effect of impulse during peak and transition

A third issue regarding phase noise is the oscillator's ability to reject supply and substrate noise. Differential ring oscillators have superior performance in this respect over LC tank oscillators. One reason for this superiority can be traced to the form of supply and substrate noise. Because these noise sources have a strong correlation, the noise will affect each stage of the ring oscillator similarly. As a result, only

noise in the vicinity of integer multiples of $N\omega_0$ affects the phase [26]. Also, in differential ring oscillators, the control voltage is usually made to be differential, rejecting common mode noise. However, in most LC tank oscillators, the control voltage is single ended, and therefore more susceptible to noise.

2.5.2 Maximum Frequency

A second specification is the maximum frequency of the VCO. An LC tank has a higher maximum attainable frequency than a ring oscillator. As shown in (7), the oscillation frequency of an LC tank is inversely proportional to the square root of L and C. The value of these elements can be made extremely low, and therefore the frequency of the tank very high. However, active devices are still needed to maintain oscillation, and can limit the frequency. An oscillation frequency of 50 GHz using an LC tank VCO was reported by [23]. The maximum frequency of a ring oscillator in CMOS is much lower. According to [7], the maximum frequency of a 3-stage ring oscillator driving a buffer in 0.18um CMOS is 7 GHz. An expression for the maximum frequency of a ring oscillator is derived in section 4.5 and suggests 9 GHz.

2.5.3 Tuning Range

As discussed previously, a high tuning range is often needed, whether to account for process variations or to work with multiple standards. If a high tuning range is needed, a ring oscillator should be used. As discussed in section 2.3.1, there are numerous parameters that can be varied to change the frequency of the ring oscillator, and many of these parameters can be varied over a wide range. The tuning range for ring oscillators can reach over 50% [7], [24]. However, typically, the only parameter varied in a monolithic LC tank is the capacitance of the varactor. This tends to result in a tuning range of less than 20% [25].

2.5.4 Manufacturability

There are two issues related to the manufacturability of the VCO. These are how easily the VCO can be integrated into a monolithic solution, and how much the center frequency will vary over process parameters.

A ring oscillator is preferred if die area is a large concern. Monolithic inductors can occupy a large area, which corresponds to higher cost. However, the center frequency of a ring oscillator can also vary by more than an LC tank due to process variations. Even with this larger variation, ring oscillators are still more likely to be able to be used at the desired frequency because of their wide tuning range.

2.5.5 Summary

Table 1 summarizes the relative strengths and weaknesses and ring and LC oscillators by marking an ‘X’ to show the oscillator with superior performance for each category.

Table 1: Summary of Ring vs. LC Oscillator

	Ring Oscillator	LC Oscillator
Phase Noise		X
Maximum Frequency		X
Tuning Range	X	
Manufacturability	X	

Chapter 3

Method

3.1 Introduction

Despite its widespread usage, the ring oscillator still poses difficulties when it comes to analysis and modeling [16]. The design of a voltage-controlled oscillator involves many trade-offs in terms of speed, power, area and application domain. For the designer to make informed decisions regarding these trade-offs, an accurate method to determine the frequency of oscillation of the VCO is necessary. One method to determine the frequency is with the use of an analytical equation, which can provide substantial insight. The designer can use the analytical equation to determine which circuit parameters have the largest effect on frequency, and which parameters need to be optimized to meet performance specifications. To achieve the same results with a numerical simulator, hundreds of simulations may need to be run, without the designer ever really understanding the effect of each circuit parameter. If the analytical equation contains process parameters, then the designer can determine the benefits or drawbacks of scaling. There are numerous CAD programs that can perform symbolic analysis of analog circuits, such as ISAAC (Interactive Symbolic Analysis of Analog Circuits) [27] and Analog Insydes [28]. These programs can produce analytical equations for many useful circuit characteristics such as the CMRR, PSRR and poles and zeros. However, these programs do not find an analytical expression for the frequency of oscillation of a circuit.

In this chapter, a novel method to derive an analytical equation for the oscillation frequency of a ring oscillator will be described. The chapter will also discuss existing equations and the methods in which they were obtained. The method proposed here will then be illustrated with an example. The example will then be expanded on to account for more parasitics and secondary effects in the next chapter.

3.2 Existing VCO Frequency Equations

As described in section 2.3.1, a ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a DC inversion. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the DC inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped. Examples of these two circuits are shown in Figure 21.

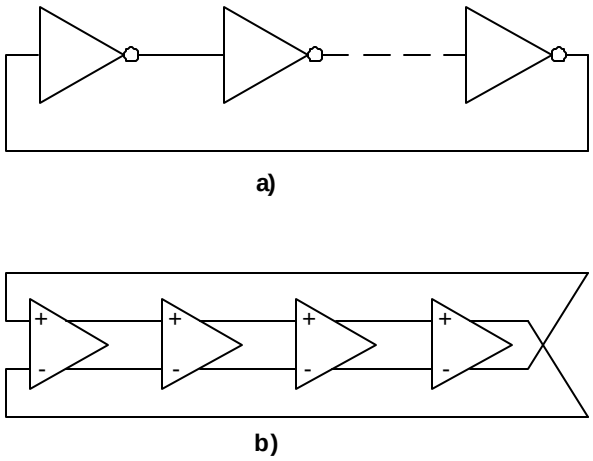


Figure 21: a) single-ended ring oscillator b) differential ring oscillator

The most common way to determine the frequency of oscillation of the ring is to assume each stage provides a delay of t_d. The signal must go through each of the N delay stages once to provide the first π phase shift in a time of $N \cdot t_d$. Then, the signal must go through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2N \cdot t_d$. Therefore, the frequency of oscillation, f, is

$$f = \frac{1}{2N \cdot t_d} \tag{13}$$

The difficulty in obtaining a value for the frequency arises when trying to determine t_d, mainly due to the non-linearities and parasitics of the circuit. The value also depends on the topology used for the delay stage. This paper will focus on differential delay stages, such as the one shown in Figure 22. Even with a circuit that appears as simple as this one, many assumptions and simplifications are necessary to obtain a value for t_d. Therefore, numerous equations exist for determining the oscillation frequency of a VCO, each derived with a separate set of assumptions and simplifications. Most of these derivations use a common set

of parameters, which are listed in Table 2. The following derivations are all for ring oscillators with differential delay stages, such as that in Figure 22.

Table 2: Delay Stage Parameters

I_{SS}	Tail current used in the delay stage
V_{sw}	Peak to peak amplitude of the voltage waveform
N	Number of delay stages in the VCO
t_d	Delay of each stage in the VCO
R_L	Load resistance of the delay stage
C_L	Load capacitance of the delay stage

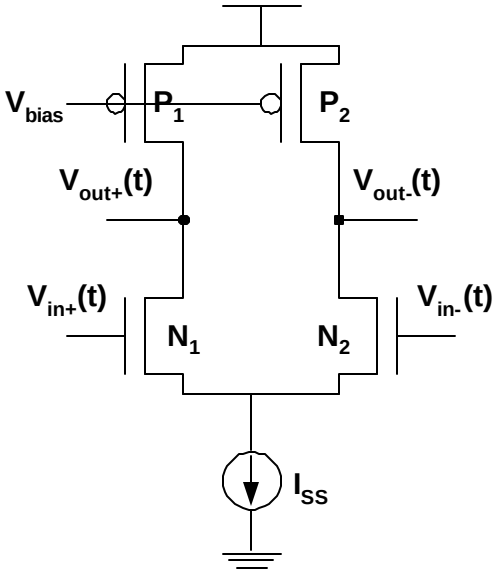


Figure 22: Type of delay stage assumed for equation derivations

Weigandt's derivation [8] assumes that each stage is separated by an ideal buffer. The ideal buffer switches when its differential input crosses zero, at which point it initiates switching of the next stage. This is illustrated in Figure 23. Based on this assumption, t_d is found by dividing the total change in the differential output voltage, V_{sw}, by the differential slew rate, I_{SS}/C_L, resulting in a delay per stage of $C_L V_{sw}/I_{SS}$. Using this definition and (13), the oscillation frequency is given by (14).

$$f = \frac{I_{SS}}{2N \cdot C_L V_{sw}} \tag{14}$$

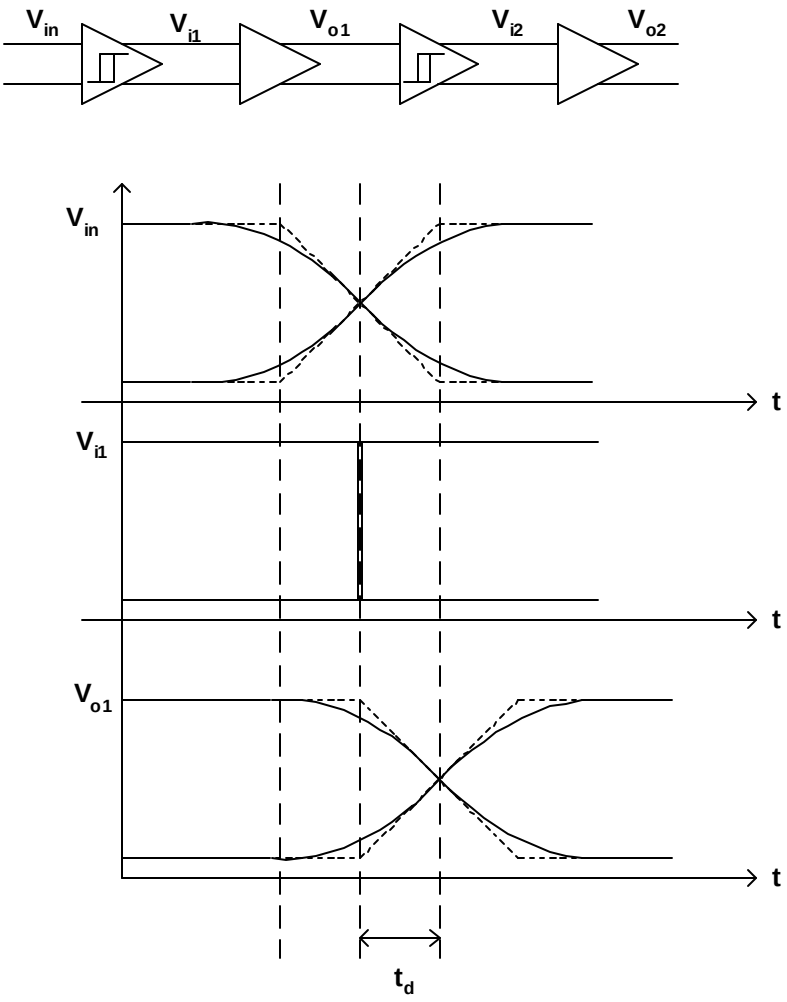


Figure 23: Timing diagram for Delay stages with ideal buffers between stages

A similar approach is taken in [9]. First, a relationship is found between the rise time and delay, as shown in Figure 24. The figure shows that t_d is equal to ηt_r, where t_r is the rise time and η is a proportionality constant. η is found to be about 0.9 for differential ring oscillators. Next, an expression must be found for t_r. t_r is defined as q_{max}/I_{SS}, and q_{max} is defined as $C_L V_{sw}$. Combining these expressions with (13) gives (15). This is equivalent to (14), except for the proportionality constant, η.

$$f = \frac{I_{SS}}{2\eta N \cdot C_L V_{sw}} \tag{15}$$

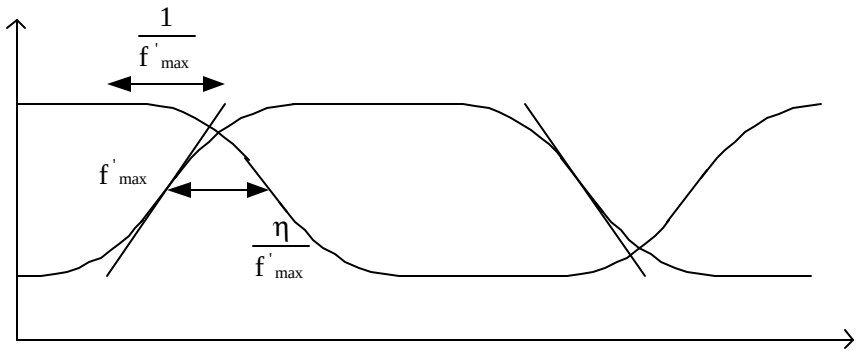


Figure 24: Relationship between rise time and delay

A different method is used in [10], which models the delay stage as an RC circuit. In this case, the PMOS load is assumed to be biased in the triode region, acting as a resistor. The delay time is defined as the time between zero crossings. Zero crossings occur at the midpoint of the voltage swing, which is at V_{DD}-V_{sw}/2. To calculate the time between zero crossings, it is assumed that the circuit can be treated as a first order RC circuit. Note that the output voltage of an RC circuit can be given by (16).

$$V_{out}(t) = V_{out}(\text{final}) + [V_{out}(\text{initial}) - V_{out}(\text{final})] \cdot e^{\frac{-t}{RC}} \tag{16}$$

In this case, V_{out}(initial) is V_{DD} and V_{out}(final) is V_{DD}-V_{sw}. We are interested in the zero crossing of the differential output voltage, and therefore set V_{out}(t) to V_{DD}-V_{sw}/2. Substituting these values into (16) and solving for t gives t_d as shown in (17).

$$t_d = R_L C_L \cdot \ln(2) \tag{17}$$

Substituting (17) into (13) gives the expression for the frequency, as shown in (18).

$$f = \frac{1}{2NR_L C_L \cdot \ln(2)} \tag{18}$$

Note that R_L is equal to V_{sw}/I_{SS}. Making this substitution results in the frequency equation shown in (19).

$$f = \frac{I_{SS}}{2NV_{sw} C_L \cdot \ln(2)} \tag{19}$$

Therefore this method results in an expression of the same form as the previous two methods, (14) and (15), with the only differences being a constant.

However, note that in this derivation, the delay time is defined as the time between zero crossings. To derive t_d, the time for the output to go from V_{DD} to V_{DD}-$V_{sw}/2$ is calculated. This assumes that for the zero crossing in the positive direction, the output switches to V_{DD} as soon as the differential voltage crosses zero. Since there is actually a delay, this method will overestimate the frequency.

A more accurate method would be to find the delay such that the input and output waveforms have equal rise times. This was attempted by [11], who approximated the input as a ramp function. Then, an expression for the ratio of the delay, t_d, to the RC time constant, τ, was found. This expression results in a nonlinear function, so a closed form solution was not found. Therefore, numerical fitting was used and it was found that $t_d = 0.8\tau$. This resulted in the frequency equation given in (20). C_{gdn} ad C_{dbn} correspond to transis tors N_1 and N_2 and C_{gdp} and C_{dbp} correspond to P_1 and P_2 in Figure 22. C_{in} is the input capacitance of the next stage.

$$f = \frac{1}{2N \cdot 0.8 \cdot R_L \left(C_{gdn} + C_{dbn} + C_{gdp} + C_{dbp} + C_{in}\right)} \tag{20}$$

Other frequency equations also exist. For example, [6] gives the frequency equation in (21) where θ is $\frac{N+1}{N} \cdot \pi$. However, a derivation or a source for this equation is not given.

$$f = \frac{\tan\theta}{2\pi RC} \tag{21}$$

These equations produce different frequency values for the same circuit and are not able to account for all effects that one may encounter in scaled geometries. The novel method introduced here can be used on a variety of ring oscillator topologies and can take into account many secondary and parasitic effects ignored by the derivations presented in this section.

3.3 Proposed Method

Although the derivations described in section 3.2 result in a variety of different equations for the oscillation frequency of a ring oscillator, they all share one major step in common. This commonality is that the derivations attempt to find an expression for t_d, and then substitute this value into (13). The method proposed here differs in that an expression for t_d is not found or required. Instead, equations are formed and equated that result in a final system with one equation and one unknown, where the unknown is the

frequency. The frequency can then be solved for in term of circuit and process parameters, resulting in an analytical expression for the frequency. The new method will be described here, and it will also be illustrated using an example.

The key assumption made in the new method is that the input and output voltage waveforms of a delay stage are sinusoidal, with frequency, f. Although the output of a ring oscillator will not be purely sinusoidal, the frequency domain representation of the output of a practical ring oscillator shows that it is a reasonable assumption [7], [21]. The actual error will be based on the voltage difference between an ideal sinusoid and the actual waveform. The accuracy of the results shown section 5.3 also show that this is a reasonable assumption. Once the input voltage has been defined, the output voltage can be found as a phase shifted version of the input voltage, where the phase shift is a function of the number of stages. Expressions for currents throughout the delay stage can then be found in terms of these voltages. These currents can then be equated using Kirchoff's Current Law (KCL), which states that the sum of currents entering a node is zero. This can reduce the system of equations to one equation with one unknown, the frequency. This equation can then be solved for the frequency, resulting in an equation in terms of circuit and process parameters. This process is outlined in Table 3.

Table 3: Outline of steps for proposed frequency derivation method

Step	
1	Define the input voltage as a sinusoid with unknown frequency, f.
2	Define the output voltage as a phase shifted version of the input voltage.
3	Determine expressions for currents flowing in and out of the output node in terms of the voltages defined in Steps 1 and 2.
4	Determine the capacitance seen between the output node of one stage and the input of the next. Define the current that charges (discharges) this capacitance.
5	Use KCL to create an expression for the current defined in step 4 in terms of the currents defined in Step 3.
6	Create an expression relating the change in voltage on the capacitance defined in Step 4 and the current charging (discharging) this capacitance, also defined in Step 4.
7	Determine valid time ranges for all expressions.
8	Substitute the expressions from Step 1 to 5 and 7 into the expression determined in Step 6 and solve for the frequency

These steps will now be explained in more detail through an example. The example will use the topology shown in Figure 25 for the delay stage. This topology has been chosen for the example because it is commonly used in practice [17], [29]. It is also convenient for comparison purposes, as this topology was used in the derivations in [8], [10] and [11] that were just described. A differential topology has been

chosen because it is used more often that single ended stages due to its ability to reject common mode noise.

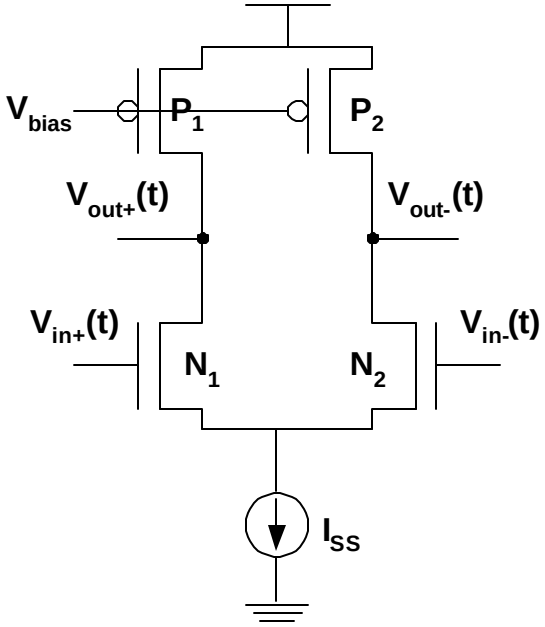


Figure 25: Delay Stage topology for example

3.3.1 First Order Example

In this example, assumptions will be made that will simplify the analysis and help to describe the method. Some of the assumptions will be removed in Chapter 4 to generate a more accurate equation.

Step 1: Define the input voltage as a sinusoid with unknown frequency, f.

For a source-coupled pair as shown in Figure 25, the tail current, I_{SS}, will switch between N_1 and N_2. When all the current is through N_2, $V_{out+}(t)$ will rise to V_{DD}, as there is no voltage drop across P_1. When all the current is through N_1, there will be a voltage drop of V_{sw} across P_1, and therefore $V_{out+}(t)$ will be V_{DD}-V_{sw}. This output voltage is the input voltage to the next stage. Based on these criteria, the input voltage waveforms, $V_{in+}(t)$ and $V_{in-}(t)$, are given in (22) and (23), in terms of the unknown frequency, f. $V_{in+}(t)$ and $V_{in-}(t)$ will be 180° out of phase. These voltages are shown in Figure 26.

$$V_{in+}(t) = V_{DD} - \frac{V_{sw}}{2}(1 - \sin(2\pi ft)) \tag{22}$$

$$V_{in-}(t) = V_{DD} - \frac{V_{sw}}{2}(1 + \sin(2\pi ft)) \tag{23}$$

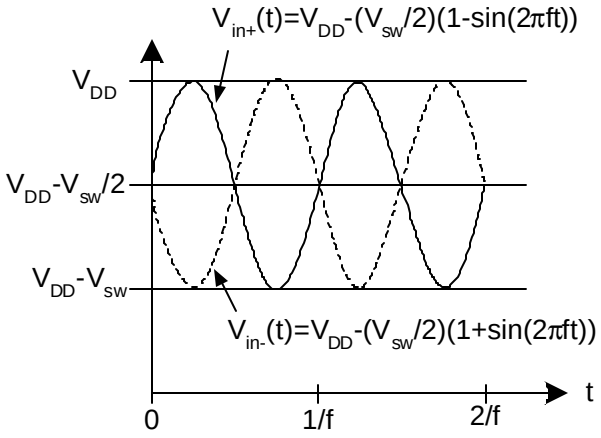


Figure 26: Input voltage waveforms

Step 2: Define the output voltage as a phase shifted version of the input voltage.

Because we are using a ring oscillator, we know the phase shift between stages. As stated in section 2.3.1, each stage of the ring must provide a phase shift of π/N radians. However, because $V_{out+}(t)$ is on the same half circuit as $V_{in+}(t)$, there is a also a DC inversion. Note that as $V_{in+}(t)$ increases, more current is steered through P_1, which acts as a resistor, and therefore $V_{out+}(t)$ drops. Therefore, the total phase shift from $V_{in+}(t)$ to $V_{out+}(t)$ is $\pi/N + \pi$, or $\pi(1+1/N)$ radians, resulting in the expression for $V_{out+}(t)$ in (24). The output voltage waveform is shown in Figure 27.

$$V_{out+}(t) = V_{DD} - \frac{V_{sw}}{2}\left(1+\sin\left(2\pi ft - \pi\left(1+\frac{1}{N}\right)\right)\right) \tag{24}$$

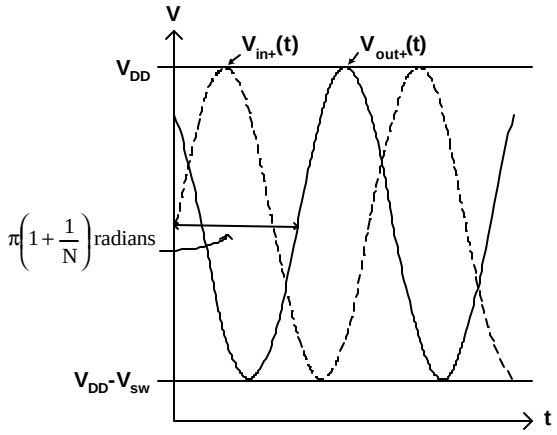


Figure 27: Output Voltage Waveform

Step 3: Determine expressions for currents flowing in and out of the output node in terms of the voltages defined in Steps 1 and 2.

By defining the input and output voltages in steps 1 and 2, expressions for the currents flowing in and out of the output node can be found. For this derivation, we are only concerned with the half circuit, as the circuit is symmetric. Therefore, the output node is at $V_{out+}(t)$. The currents related to this node are shown in Figure 28. The currents shown here are for a first order analysis.

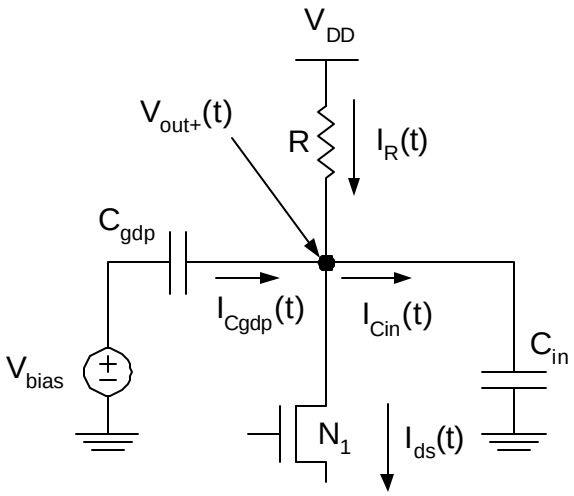


Figure 28: Currents for KCL

First, we must see how we went from the circuit in Figure 25 to the circuit elements and currents of Figure 28. As mentioned previously, we are only concerned with the half circuit, due to symmetry. The PMOS load transistor, P_1, has been replaced with a resistor, R, and capacitance, C_{gdp}. P_1 is biased in the linear region, and therefore the resistance is relatively constant with changes in V_{ds}. This resistance is modeled in Figure 28 as R. This assumption is removed in section 4.2, and this resistance is made to be time-varying. Also, because P_1 is in the linear region, there is a gate-drain capacitance. The capacitance is called C_{gdp} and is equal to $\frac{1}{2}WLC_{ox}$ of P_1. There is no gate to source capacitance because both nodes are at small signal ground. N_1 is not replaced with any models, but the current source is removed and is accounted for by the expression for the current through N_1, which is a function of I_{SS}. The capacitance between the output node and the input of the next stage is called C_{in}.

Now, an expression for the currents related to these circuit elements must be determined. The expression for $I_R(t)$ is given in (25).

$$I_R(t) = \frac{V_{DD} - V_{out+}(t)}{R} \tag{25}$$

The current necessary to charge (discharge) C_{gdp}, $I_{Cgdp}(t)$ is given in (26).

$$I_{Cgdp}(t) = C_{gdp} \cdot \frac{d}{dt}\left(V_{bias} - V_{out+}(t)\right) \tag{26}$$

Some difficulty arises in determining the drain current in the differential pair transistors, $I_{ds}(t)$. The current through N_1 is a function of the tail current, I_{SS}, and the differential input voltage, $V_{id}(t)$, where $V_{id}(t)=V_{in+}(t)-V_{in-}(t)$. Therefore, as derived in [19], the drain current, $I_{ds}(t)$ is

$$I_{ds}(t) = \frac{I_{SS}}{2} + \frac{\mu_n C_{ox} \frac{W}{L} V_{id}(t)}{4} \sqrt{\frac{4 \cdot I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - V_{id}^2(t)} \tag{27}$$

It is very important to note that (27) is only valid for certain values of $V_{id}(t)$. The differential input voltage steers current between N_1 and N_2. However, as $V_{id}(t)$ increases, the maximum current that can flow through N_1 is I_{SS}. Also, as $V_{id}(t)$ decreases and the current is steered through N_2, the minimum amount of current that can flow through N_1 is 0. The relationship between $V_{id}(t)$ and I_{ds} is shown in Figure 29.

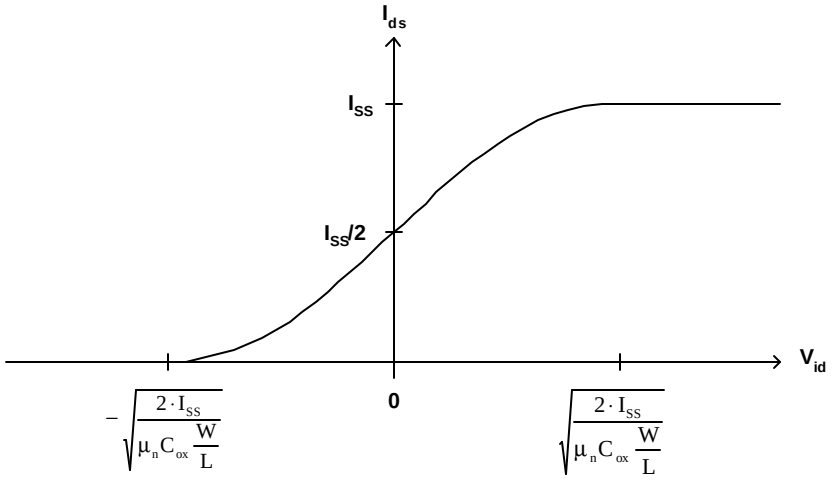


Figure 29: I_{ds} vs. V_{id} for a differential pair

The range for which (27) is valid is given in (28).

$$-\sqrt{\frac{2\cdot I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} \le V_{id} \le \sqrt{\frac{2\cdot I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} \tag{28}$$

If V_{id} is below the left side of this relation, I_{ds} is equal 0, as all the current is flowing through N_2. If V_{id} is higher than the right side of this relation, I_{ds} is equal to I_{SS}, as all the current is flowing through N_1. This range will become important in subsequent steps. This range can be easier to visualize using Figure 30. Note the voltage lines showing where V_{id} crosses over the ranges defined in (28). On the right side of the diagram, the value for I_{ds} through N_1 is shown for each region.

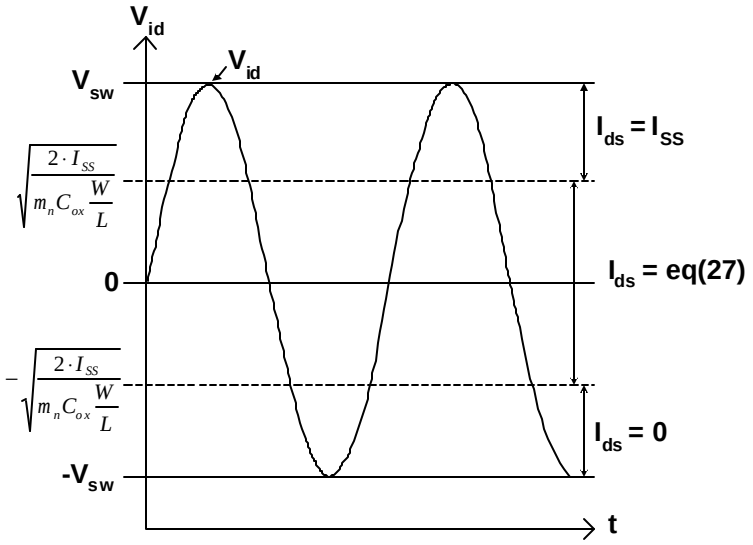


Figure 30: The expression for I_{ds} is a dependant upon V_{id}

Expressions for all currents shown in Figure 28 have been determined, except for $I_{Cin}(t)$. This is because it is the current charging up the capacitance between the output of one stage and the input of the next. This current will be defined in Step 4.

Step 4: Determine the capacitance seen between the output node of one stage and the input of the next. Define the current that charges (discharges) this capacitance.

For the delay stage used in this example, the capacitance seen at the output node looking into the input of the next delay stage is defined as C_{in}. The current charging (discharging) this capacitance is defined as $I_{Cin}(t)$, as shown in Figure 28. C_{in} is the gate capacitance of the source-coupled transistor of the next stage and is approximately $(2/3)WLC_{ox}$.

Step 5: Use KCL to create an expression for the current defined in step 4 in terms of the currents defined in Step 3.

In Step 3, expressions were found for all currents flowing in and out of the output node, except for the current charging up the capacitance associated with the next stage. This current was defined is Step 4. Using KCL and Figure 28, an expression can be formed which relates these currents. The expression is given in (29).

$$I_{Cin}(t) = I_R(t) + I_{Cgdp}(t) - I_{ds}(t) \tag{29}$$

Step 6: Create an expression relating the change in voltage on the capacitance defined in Step 4 and the current charging (discharging) this capacitance, also defined in Step 4.

The voltage and current can be related using the charge-voltage relationship for a capacitor, Q=CV. In this case, the charge, Q, is the integral of $I_{Cin}(t)$ with respect to time. The capacitance is C_{in}. The voltage is the voltage change over the time of integration. Substituting these values into Q=CV results in (30).

$$\int_{t_n}^{t_{n+1}} I_{Cin}(t)\,dt = C_{in} \cdot \left(V_{out+}(t_{n+1}) - V_{out+}(t_n)\right) \tag{30}$$

Step 7: Determine valid time ranges for all expressions.

There are two separate time ranges that need to be determined. The first is the limits of integration for (30). The second is the time ranges in which the current expressions determined in Step 3 are valid.

To determine the oscillation frequency, the integration in (30) should be performed over one full period of $V_{out+}(t)$[1]. However, if this was done in one step, the resulting expression would be 0=0, as both sides contain periodic functions. Therefore, the integration must be separated into sections where $V_{out+}(t)$ is monotonic. Therefore, the period will be divided into 4 sections, each corresponding to a quarter of the period. The overall frequency expression will be found by averaging the expressions from each equally weighted section. The times that the first section begins and ends will be defined as t_0 and t_1, respectively. t_0 is the time at which $V_{out+}(t)$ crosses the mid-swing point in the positive direction. This can be determined by equating (24) to the mid-swing value, $V_{DD}-V_{sw}/2$. As this function is periodic, there are an infinite number of solutions. We desire the first solution that corresponds to a positive crossing of the mid-swing point. This solution for t_0 is given in (31).

[1] A half period is actually sufficient, as will be explained later

$$t_0 = \frac{N+1}{2Nf} \tag{31}$$

Once t_0 has been determined, each subsequent time of interest must be ¼ of a period later. Since the period is equal to 1/f, an expression for subsequent integration limits is given in (32). Note that the magnitude of the voltage change during each of these time periods is $V_{sw}/2$.

$$t_n = t_{n-1} + \frac{1}{4f}, \quad n = 1,2,3,4 \tag{32}$$

The second time range of importance is related to the time ranges for which the current expressions determined in Step 3 are valid. For this case, $I_R(t)$ and $I_{Cgdp}(t)$ are valid at all times. As discussed previously, the range for which the general expression for $I_{ds}(t)$ is valid is given in (28). Therefore, the times at which V_{id} crosses these limits during a full period must be determined. To simplify the process, refer to Figure 31. In this figure, t_0 to t_4, are labeled to show the full period of the output voltage, V_{out+}, of interest. Within this period, the points at which V_{id} crosses the ranges defined in (28) are also marked. These times are labeled as t_{1a}, t_{1b}, t_{3a} and t_{3b}. Determining these times will enable a piecewise expression for $I_{ds}(t)$ to be used in (30), remembering that $I_{Cin}(t)$ is a function of $I_{ds}(t)$. To determine these times, V_{id} should be set to the right side of the relation in (28). Noting that V_{id} is equal to $V_{sw} \cdot \sin(2\pi ft)$ results in (33), where the time that V_{id} crosses this limit is called t_{sat}.

$$V_{sw} \sin\left(2\pi f t_{sat}\right) = \sqrt{\frac{2 \cdot I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \tag{33}$$

Solving this expression for t_{sat} gives (34).

$$t_{sat} = \frac{1}{2\pi f} a\sin\left(\frac{1}{V_{sw}} \sqrt{\frac{2 \cdot I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \right) \tag{34}$$

It can be shown that the time at which V_{id} crosses the limits of the relation in (28) can be given by the expression in (35), where m refers to the m^{th} V_{id} zero crossing.

$$t_{cross} = \frac{m}{2f} \pm t_{sat}, \quad m = 1,2,3... \tag{35}$$

For this case, the times at which V_{id} crosses are near the 2nd and 3rd zero crossing, and therefore m =2,3. The times for t_{1a} and t_{1b} are given in (36) and the times for t_{3a} and t_{3b} are given in (37).

$$\begin{aligned} t_{1a} &= \frac{1}{f} - t_{sat} \\ t_{1b} &= \frac{1}{f} + t_{sat} \end{aligned} \tag{36}$$

$$\begin{aligned} t_{3a} &= \frac{3}{2f} - t_{sat} \\ t_{3b} &= \frac{3}{2f} + t_{sat} \end{aligned} \tag{37}$$

All times of importance with regards to the limits of integration and the ranges for the expression for $I_{ds}(t)$ are shown in Figure 31.

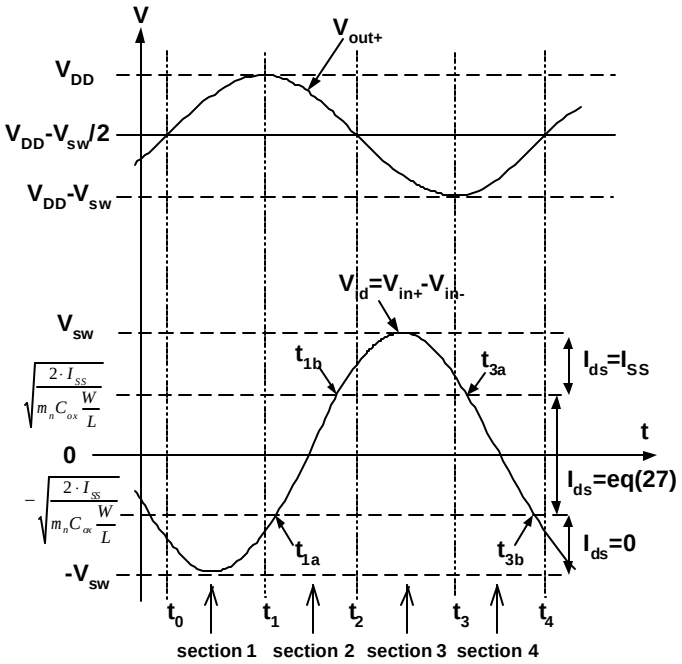


Figure 31: Figure to determine limits of integration

Step 8: Substitute the expressions from Step 1 to 5 and 7 into the expression determined in Step 6 and solve for the frequency.

This step must be performed for each of the four sections labeled in Figure 31. The limits of integration are determined by (31) and (32). $I_{Cin}(t)$ can be replaced by the expression in (29). After this replacement, expressions for the currents can be found from (25), (26) and (27), remembering that the expression for $I_{ds}(t)$ is piecewise. The current expressions contain $V_{id}(t)$ and $V_{out+}(t)$ terms. $V_{id}(t)$ is equal to $V_{in+}(t)$-$V_{in-}(t)$, which corresponds to (22) and (23) respectively. $V_{out+}(t)$ can be replaced by (24). These substitutions can be easily performed by using a symbolic math tool such as mathcad. There are really only a few fundamental equations developed which are then related to each other with some substitutions, and this can be achieved easily and clearly with such a tool.

To demonstrate this process, equations for the first two sections will be shown. For section 1, the lower limit of the integration is t_0 and the upper limit is t_1. The change in $V_{out+}(t)$ during this period is $V_{sw}/2$. After substituting for $I_{Cin}(t)$ based on the KCL equation, (29), (38) is generated.

$$\int_{t_0}^{t_1}\left(I_R(t)+I_{Cgdp}(t)-I_{ds}(t)\right)dt = C_{in}\cdot\frac{V_{sw}}{2} \tag{38}$$

In Step 7, expressions for the currents were determined. The only expression that was piecewise was $I_{ds}(t)$. Note that for section 1, V_{id} is always below the bottom threshold line in Figure 31, and therefore there is no current flowing through N1, so $I_{ds}=0$. Making this substitution gives (39).

$$\int_{t_0}^{t_1}\left(I_R(t)+I_{Cgdp}(t)\right)dt = C_{in}\cdot\frac{V_{sw}}{2} \tag{39}$$

After making the remaining substitutions, the equation will contain only one unknown, the frequency, f. Therefore, solve for the frequency. Again, using mathcad or an equivalent tool simplifies this process, as it can symbolically solve for a variable. Solving for the frequency for section 1 gives

$$f_1 = \frac{1}{4}\cdot\frac{\pi-2}{\pi\cdot R\left(C_{in}+C_{gdp}\right)} \tag{40}$$

We have completed section 1 and now move on to section 2. For section 2, there are two additional times labeled between t_1 and t_2. These times, t_{1a} and t_{1b}, correspond to times when V_{id} crosses the threshold values corresponding to a new range in the relation given in (28). These threshold crossings mean that the equation giving $I_{ds}(t)$ becomes piecewise. From time t_1 to t_{1a}, V_{id} is below the left side of the relation, and

therefore I_{ds}=0. From time t_{1a} to t_{1b}, I_{ds} is given by (27). From time t_{1b} to t_2, V_{id} is greater than the right side of the relation, and therefore $I_{ds} = I_{SS}$. Again, $I_R(t)$ and $I_{Cgdp}(t)$ have the same expression throughout the time period. Next, substitute the KCL relation for $I_{Cin}(t)$ from (29) into (30), accounting for the piecewise nature of $I_{ds}(t)$. Then, note that the change in $V_{out+}(t)$ for section 2 is $-V_{sw}/2$. These substitutions result in (41).

$$\int_{t_1}^{t_2}\left(I_R(t)+I_{Cgdp}(t)\right)dt+\int_{t_1}^{t_{1a}}(0)dt+\int_{t_{1a}}^{t_{1b}}I_{ds}(t)dt+\int_{t_{1b}}^{t_2}(I_{SS})dt=C_{in}\cdot\frac{-V_{sw}}{2} \tag{41}$$

The expressions for t_1 and t_2 can be found from (31) and (32). The expressions for t_{1a} and t_{1b} can be found from (36). The current equations can be found from (25), (26) and (27). After completing all substitutions, the only unknown becomes the frequency, f. Solving for the frequency results in (42).

$$f_2=\frac{1}{4}\cdot\frac{NV_{sw}(2-\pi)+4\pi I_{SS}R}{\pi NV_{sw}R(C_{in}+C_{gdp})} \tag{42}$$

The same method can be used for sections 3 and 4 to determine f_3 and f_4, respectively. Once the four frequency expressions have been determined, which together represent one complete period of oscillation, the overall frequency expression can be determined by averaging the four expressions. The final frequency expression for the VCO is given in (43).

$$f=\frac{I_{SS}}{2NV_{sw}(C_{in}+C_{gdp})} \tag{43}$$

Note that this equation is equivalent to (14), the frequency equation derived by [8], suggesting some validity to this method. Experimental results and a more accurate equation derived in Chapter 4 also reinforce the validity of the method proposed here.

It should also be noted that the process of determining the overall frequency expression can be simplified. Due to the symmetry of the differential delay stage, (43) can be found by averaging only f_1 and f_2, corresponding to the first half of the period, instead of f_1 to f_4.

As discussed previously, the importance of an analytical equation is that it can show the designer how circuit and process parameters affect the behavior of the circuit. Eq. (43) shows that the frequency is directly proportional to the tail current and is inversely proportional to the number of delay stages, the voltage swing and to the parasitic and load capacitances. A more accurate equation will be derived in the following chapter.

Chapter 4

Secondary Effects

4.1 Introduction

The frequency equation derived in Chapter 3 is based on several simplifying assumptions. One of the benefits of the proposed method is that the designer can determine which parasitic and secondary effects should be included in the frequency derivation. Parasitics can be included by adding these elements to the model and including the corresponding currents in the KCL expression. Expressions for elements can also be made time-varying, since an integration over time is performed. In this chapter, we will remove some previous assumptions to develop a more accurate expression for the oscillation frequency. Parasitic capacitances such as junction, side-wall and overlap capacitances will be included. Expressions for element values will be made time-varying, such as the PMOS load resistance. The gate resistance, which has an effect at high-frequencies, will also be included. The equations derived here, as well as (43), will also be used to show how an expression for the maximum oscillation frequency of a ring oscillator can be derived.

4.2 Time-varying resistance

The additional effects will be included one at a time to more easily see the effect they have on the final frequency expression. The first additional effect will be to make the expression for the PMOS load resistance time-varying. In section 3.3.1, it was assumed that this value was constant. In reality this resistance is a function of V_{ds}. Since V_{ds} is a function of time, this resistance is also a function of time. The expression for the resistance of a PMOS transistor in the linear region is given by (44).

$$R = \frac{1}{\left[\mu_p C_{ox} \frac{W}{L}\left(\left|V_{gs}\right| - \left|V_{tp}\right| - \left|V_{ds}\right|\right)\right]} \tag{44}$$

For the circuit in Figure 25, $|V_{gs}| = V_{DD} - V_{bias}$ and $|V_{ds}| = V_{DD} - V_{out+}(t)$. Making these substitutions in (44) gives (45), an expression for the PMOS load resistance as a function of time.

$$R(t) = \frac{1}{\left[\mu_p C_{ox} \frac{W}{L}\left(V_{DD} - V_{bias} - \left|V_{tp}\right| - \left(V_{DD} - V_{out+}(t)\right)\right)\right]} \tag{45}$$

The process described in section 3.3 can be repeated, with the only change being that R in (25), the expression for $I_R(t)$, is replaced by R(t), given in (45). This is shown in (46).

$$I_R(t) = \frac{V_{DD} - V_{out+}(t)}{R(t)} \tag{46}$$

If the method is repeated for the first half of the cycle, the expressions for f_1 and f_2 result, as shown in (47) and (48) respectively.

$$f_1 = \frac{\mu_p C_{ox} \frac{W}{L}\left[\frac{1}{2\pi}\left(V_{dd} - V_t - V_{bias} - V_{sw}\right) - \frac{1}{4}\left(V_{dd} - V_t - V_{bias} - \frac{3}{4}V_{sw}\right)\right]}{C_{in} + C_{gdp}} \tag{47}$$

$$f_2 = \frac{\mu_p C_{ox} \frac{W}{L}\left[\frac{1}{4}\left(V_{dd} - V_t - V_{bias} - \frac{3}{4}V_{sw}\right) - \frac{1}{2\pi}\left(V_{dd} - V_t - V_{bias} - V_{sw}\right)\right] + \frac{I_{SS}}{NV_{sw}}}{C_{in} + C_{gdp}} \tag{48}$$

Averaging f_1 and f_2 gives (49), the oscillation frequency with a time-varying resistive load.

$$f = \frac{I_{SS}}{2NV_{sw}\left(C_{in} + C_{gdp}\right)} \tag{49}$$

Note that this equation is identical to (43). Therefore, including the time-varying nature of the equivalent resistance of the PMOS load has no effect on the frequency.

4.3 Parasitic Capacitances

For the derivation of (43), the only capacitances included were the input capacitance of the delay stage, C_{in}, and the gate-drain capacitance of the PMOS load, C_{gdp}. However, there are numerous other parasitic capacitances which can affect the oscillation frequency. There is a junction and a sidewall capacitance associated with each transistor. This is a time-varying capacitance. There is also a gate-drain overlap capacitance for the NMOS transistors.

The expressions for the parasitics introduced in this section use some hspice parameters, which are shown in Table 4. The equations use an 'n' or 'p' following these parameters to refer to the NMOS or PMOS parameter, respectively. For example, Cj_p refers to the zero-bias area junction capacitance of a PMOS transistor.

Table 4: hspice parameters for parasitic capacitances

Cj	Zero-bias area junction capacitance
Cjsw	Zero-bias sidewall junction capacitance
Cgdo	Gate-drain overlap capacitance
Pb	p-n junction potential
Pbsw	p-n junction sidewall potential
Mj	Area junction grading coefficient
Mjsw	Sidewall junction grading coefficient
Ad	Drain area
Pd	Drain perimeter

In the derivation of (43), we ignored the drain to bulk capacitances of all four transistors shown in Figure 25. These capacitances are due to the reverse biased p-n-junctions between the respective drains and bulk. These capacitances are a function of the drain voltage. Since the drain voltage varies with time, these capacitances are also a function of time. This expression for this capacitance [30] is given in (50).

$$C_{db}(t) = \frac{Cj \cdot Ad}{\left(1 + \frac{V_{db}(t)}{pb}\right)^{mj}} + \frac{Cjsw \cdot Pd}{\left(1 + \frac{V_{db}(t)}{pbsw}\right)^{mjsw}} \tag{50}$$

For the NMOS differential pair, the drain voltage is $V_{out+}(t)$ and the bulk voltage is ground, meaning that $V_{db}(t)$ is equal to $V_{out+}(t)$. Substituting this value into (50) gives (51), the time-varying drain-bulk capacitance of the differential pair transistors.

$$C_{dbn}(t) = \frac{Cj_n \cdot Ad_n}{\left(1 + \frac{V_{out+}(t)}{pb_n}\right)^{mj_n}} + \frac{Cjsw_n \cdot Pd_n}{\left(1 + \frac{V_{out+}(t)}{pbsw_n}\right)^{mjsw_n}} \tag{51}$$

For the PMOS load, the drain voltage is $V_{out+}(t)$ and the bulk voltage is V_{DD}, meaning that $V_{db}(t)$ is equal to $V_{out+}(t)$-V_{DD}. Substituting this value into (50) gives (52), the time-varying drain-bulk capacitance of the PMOS load transistors.

$$C_{dbp}(t) = \frac{Cj_p \cdot Ad_p}{\left(1 + \frac{V_{out+}(t) - V_{DD}}{pb_p}\right)^{mj_p}} + \frac{Cjswp \cdot Pdp}{\left(1 + \frac{V_{out+}(t) - V_{DD}}{pbsw_p}\right)^{mjsw_p}} \tag{52}$$

Another simplification made in the derivation of (43) is that the gate-drain overlap capacitance of the differential pair transistors was ignored. This capacitance is given in (53).

$$C_{gdovn} = W_n \cdot Cgdo_n \tag{53}$$

The voltages on both nodes of this capacitance are time-varying, with the gate voltage being $V_{in+}(t)$ and the drain voltage being $V_{out+}(t)$. Since both node voltages are time-varying, the contribution of this capacitance with respect to the oscillation frequency becomes difficult to determine. Since these voltages are predefined as $V_{in+}(t)$ and $V_{out+}(t)$, the proposed method is able to determine their contribution.

At this point we have removed three of the assumptions made in the derivation of (43), the first-order oscillation frequency equation. We have made the equivalent resistance of the PMOS load a time-varying function of V_{ds}. We have included the drain-bulk capacitances of all four transistors shown in Figure 25. Moreover, these capacitances are made time-varying. Furthermore, we have also included the gate-drain overlap capacitance of the differential pair transistors. These three additional effects and the related currents are shown in Figure 32.

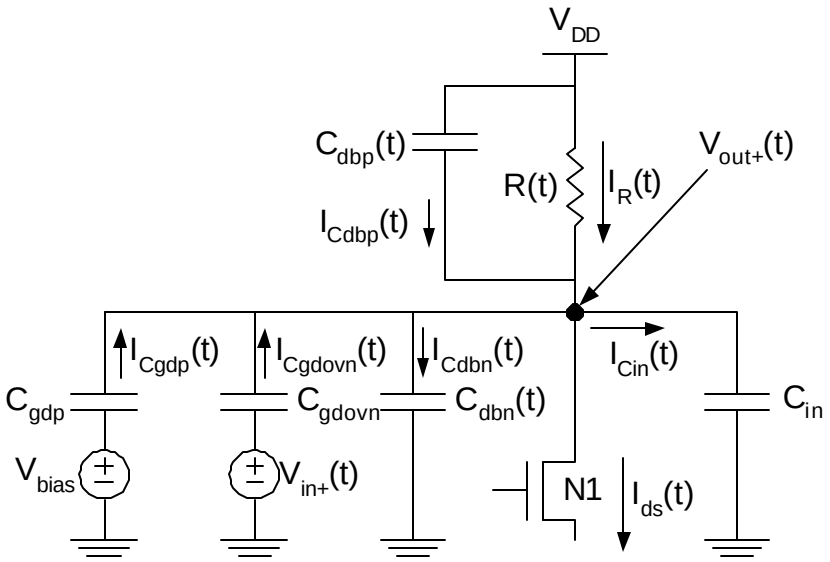


Figure 32: KCL including additional effects

The next step is to find expressions for these currents. The expressions for $I_{Cgdp}(t)$, $I_{ds}(t)$ and $I_R(t)$ were found previously and are given in (26), (27) and (46), respectively. The expression for $I_{Cgdon}(t)$ is given in (54).

$$I_{Cgdovn}(t) = C_{gdovn} \cdot \frac{d\left(V_{in+}(t) - V_{out+}(t)\right)}{dt} \tag{54}$$

To determine the expressions for the current charging $C_{dbn}(t)$ and $C_{dbp}(t)$, it is important to note that these capacitances are time-varying, and therefore the relation I(t)=C(dV/dt) does not hold. To derive the correct expression, begin with the standard charge-voltage relationship for a capacitor, Q=CV, where both C and V are functions of time. Differentiating both sides with respect to time and noting that dQ/dt is current gives (55). Note that if the capacitance is not a function of time, dC(t)/dt =0, and (55) reduces to I=C(dV/dt).

$$I(t) = C(t) \cdot \frac{dV(t)}{dt} + \frac{dC(t)}{dt} \cdot V(t) \tag{55}$$

Eq. (55) can now be used to find expressions for $I_{Cdbn}(t)$ and $I_{Cdbp}(t)$, as given in (56) and (57), respectively.

$$I_{Cdbn}(t) = C_{dbn}(t) \cdot \frac{dV_{out+}(t)}{dt} + \frac{dC_{dbn}(t)}{dt} V_{out+}(t) \tag{56}$$

$$I_{Cdbp}(t) = C_{dbp}(t) \cdot \frac{d(V_{DD} - V_{out+}(t))}{dt} + \frac{dC_{dbp}(t)}{dt}(V_{DD} - V_{out+}(t)) \tag{57}$$

We now have expressions for the resistance, the parasitic capacitances, and the related currents, all of which are time-varying. However, the proposed method can still result in a closed form expression for the frequency of oscillation. To solve for the frequency, the method is identical to that described in section 3.3. In terms of specific values, the KCL equation in step 4 must include the currents added in this section. Similarly, the new time-varying equations for all currents and parasitics must be substituted. Including these additional currents, the new KCL equation becomes the one shown in (58).

$$I_{Cin}(t) = I_R(t) + I_{Cgdp}(t) + I_{Cgdovn}(t) - I_{Cdbn}(t) + I_{Cdbp}(t) - I_{ds}(t) \tag{58}$$

Following the steps outlined in section 3.3, and using some simplifications, the resulting equation for the oscillation frequency is given in (59). The simplification of the gate-drain overlap term involves ignoring smaller terms, and is detailed in Appendix A. The simplification of the drain-bulk capacitance effects, which corresponds to the Cjun and Cjunsw terms, involves using the binomial expansion to simplify the expression. This simplification is detailed in Appendix B.

$$f = \frac{I_{SS}}{2NV_{sw}\left(C_{in} + Cgd_p + Cjun_n + Cjunsw_n + Cgdov_n + Cjun_p + Cjunsw_p\right)} \tag{59}$$

Where:

$$C_{in} = \frac{2}{3} W_n L_n C_{ox} \tag{60}$$

$$C_{gdp} = \frac{1}{2} W_p L_p C_{ox} \tag{61}$$

$$Cjun_n = \frac{Cj_n Ad_n}{\left(1 + \frac{V_{dd}}{pb_n}\right)^{mj_n}} \left[2 - mj_n \left(1 - \frac{1}{\left(1 + \frac{V_{dd}}{pb_n}\right)} \right) \right] \tag{62}$$

$$Cjunsw_n = \frac{Cjsw_n Pd_n}{\left(1+\frac{V_{dd}}{pbsw_n}\right)^{mjsw_n}}\left[2-mjsw_n\left(1-\frac{1}{\left(1+\frac{V_{dd}}{pbsw_n}\right)}\right)\right] \tag{63}$$

$$Cgdov_n = \left(1+\cos\left(\frac{\pi}{N}\right)\right)W_n Cgdo_n \tag{64}$$

$$Cjun_p = 2Cj_p Ad_p \tag{65}$$

$$Cjunsw_p = 2Cjsw_p Pd_p \tag{66}$$

Eq. (59) shows the contribution of the time-varying parasitics. The drain-bulk capacitances of the PMOS and NMOS transistors add to the denominator, and decrease the frequency. Increasing V_{sw} increases the weight of these components. The weighting of the drain-bulk capacitance terms is higher than in other equations. Other equations use the average value of these time-varying terms, but this method suggests the actual weighting is about twice that value. Moreover, the gate-drain overlap capacitance is multiplied by a factor of $1+\cos(\pi/N)$. This factor is equivalent to showing the effect of the Miller capacitance at this node because the voltages at both nodes of the capacitor, $V_{in+}(t)$ and $V_{out+}(t)$, are moving in opposite directions. As N increases, the phase difference of these voltages approaches π, and the value of $1+\cos(\pi/N)$ approaches 2, resulting in a doubling of the gate-drain overlap capacitance.

At this point, we have shown that the proposed method, which results in (59), is able to incorporate additional parasitics and secondary effects. These time-varying parameters are easily included in the frequency equation.

4.4 RF effects

Due to aggressive scaling of CMOS, it has become a viable technology for RF applications. However, simulating RF circuits with models intended for low frequency applications can create inaccurate results. The two main effects not included in low frequency compact models that affect high frequency operation are additional parasitics, such as the gate resistance, and nonquasi-static (NQS) effects.

4.4.1 Parasitics

One of the most commonly used compact models is BSIM3v3. However, the standard BSIM3v3 model does not take into account parasitics that affect the high frequency behavior of the MOS transistor. It is generally agreed that at least a gate resistance and a substrate coupling network should be added to the standard model [31]-[33], as shown in Figure 33.

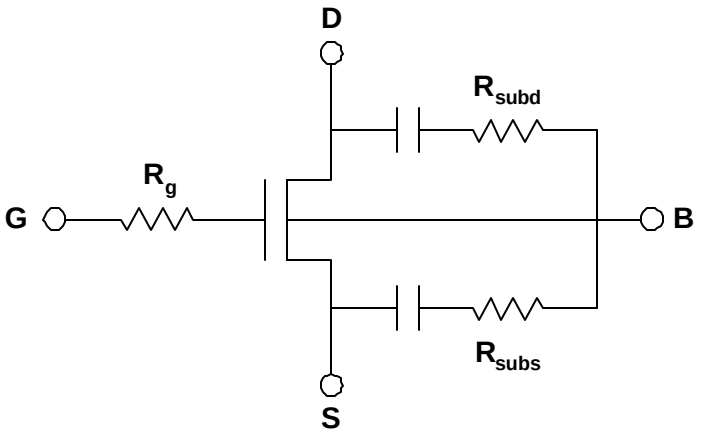


Figure 33: Additional parasitics with existing model

The gate resistance, R_g, consists of two parts: the physical gate resistance and the part due to the NQS effects. The physical gate resistance is due to the poly sheet resistance. The NQS component will be discussed in the following section, but is related to the finite time for the charge under the gate to react to the applied voltage. The substrate resistances, R_{subd} and R_{subs}, are the resistances between the drain/ source junctions and the substrate contacts. These resistances are a function of the layout.

4.4.2 Nonquasi-static Effects

There is a finite time necessary for the charge in the channel to respond to changes in the bias conditions. At low frequencies and/or short channel lengths, this time can be ignored, and the charge can be made a function of the current bias conditions (quasi-static). However, at high frequencies and/or long channel lengths, the charge is a function of both the bias conditions and the history. To model this finite response time, a nonquasi-static approach must be taken. This finite response time is related to the distributed effect of the channel resistance [34]. This resistance in turn increases the effective gate resistance, and thus the gate resistance is a function of both the physical gate resistance and the NQS effects [35]. This distributed channel and gate resistances are shown in Figure 34. R_{eltd} is the gate electrode sheet resistance and R_{ch} is the channel resistance.

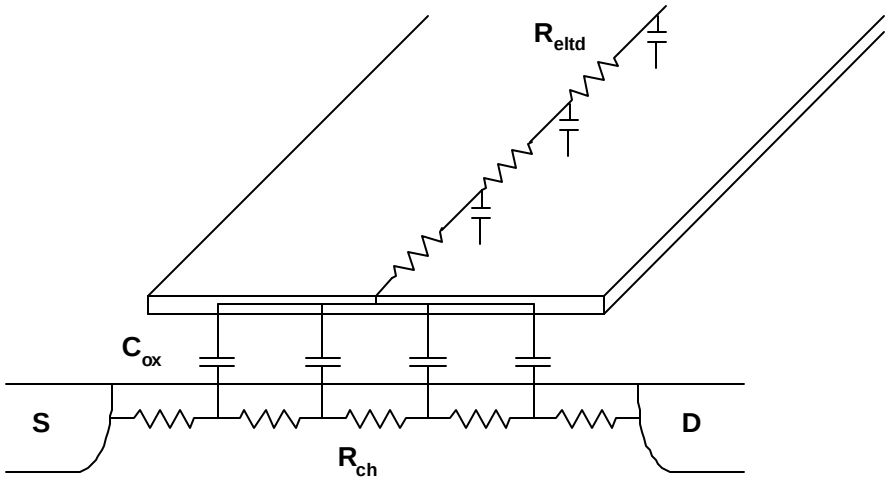


Figure 34: Distributed gate and channel resistance [35]

There are many more complex models to account for all RF effects [33], [36], [37], but a simple model is sufficient for the purposes of deriving an analytical equation.

4.4.3 Gate Resistance

As discussed in section 4.4.1 and section 4.4.2, extra parasitics and NQS effects should be included as part of the MOS model to obtain accurate simulation results at high frequencies. Since VCOs are often used in high frequency applications, it is important that RF effects be included in the oscillation frequency equation derived here. As mentioned previously, the purpose of the analytical equation is for the designer to be able to easily see the effect of parameters on the oscillation frequency. A complex RF model will result in an extremely complex equation. Therefore, only the dominant effects will be included. It can be shown that a strict minimum for an RF model is to include a gate resistance [33], and that is what will be done here. The delay stage with gate resistance is shown in Figure 35.

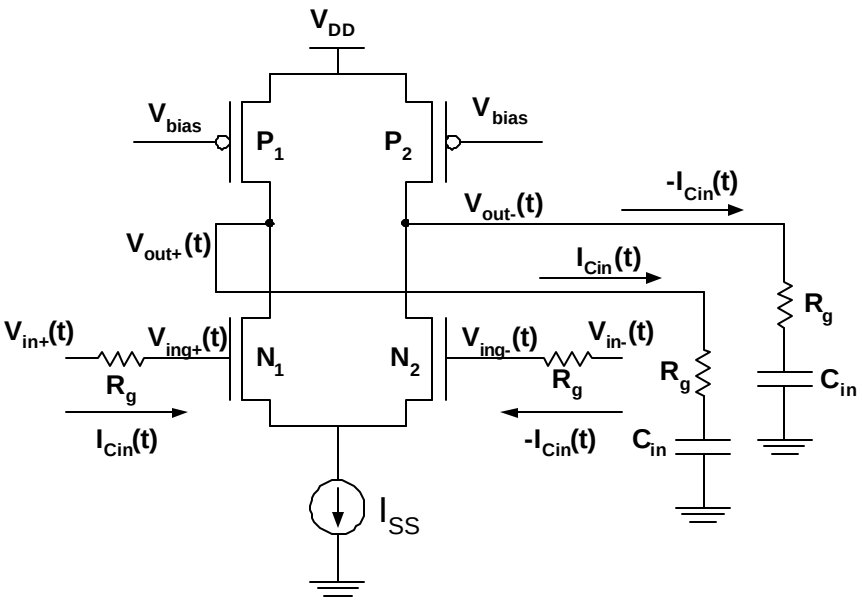


Figure 35: Delay stage with gate resistance, R_g.

Notice that the gate resistance affects the circuit in two ways. The first is on the input as the gate resistance affects the differential input voltage of the source-coupled pair, N_1 and N_2. The second is at the output. Remember that the important times when deriving the oscillation frequency correspond to when the voltage on C_{in} crosses the mid-swing point, and then every quarter period thereafter. With no gate resistance, this voltage is equal to $V_{out+}(t)$. However, with the gate resistance, the voltage on C_{in} no longer equals $V_{out+}(t)$, and the time that the voltage crosses the mid-swing point will shift slightly. This shift must be determined as it will shift the integration limits. To see the effect of the gate resistance on the oscillation frequency, the effect on the differential input voltage and on the time shift at the output will be dealt with separately, and then combined. Also, detailed calculations not shown in this section can be found in Appendix C.

The time shift due to the gate resistance will be determined first. Therefore, the time that the voltage on C_{in} crosses the mid-swing point, V_{dd}-V_{sw}/2, must be determined. The voltage on C_{in} is $V_{out+}(t)$-$I_{Cin}(t)R_g$. The time that this voltage crosses the mid-swing point can be found by solving (67) for t_0.

$$V_{out+}(t_0) - I_{Cin}(t_0)R_g = V_{dd} - \frac{V_{sw}}{2} \tag{67}$$

where $V_{out+}(t)$ is given in (24) and $I_{Cin}(t)$ is found through KCL as before. Solving for t_0 gives (68), where C_{par} is a sum of all the parasitic capacitances as defined in (69). The details of determining this time shift can be found in Appendix C.

$$t_0 = \frac{N+1}{2Nf} - R_g C_{par} \tag{68}$$

.

$$C_{par} = Cgd_p + Cjun_n + Cjunsw_n + Cgdov_n + Cjun_p + Cjunsw_p \tag{69}$$

Note that if R_g is set to 0, (68) reduces to the previous expression for t_0 given in (31). With this time shift, the new expression for the oscillation frequency becomes

$$f = \frac{I_{SS}}{2NV_{sw}(C_{in} + C_{par})} \cdot \left(1 - \frac{I_{SS} R_g C_{par}}{V_{sw}(C_{in} + C_{par})}\left(2 - N\left(\frac{1}{2} - \frac{1}{\pi}\right)\right)\right) \tag{70}$$

Again, if R_g is set to zero, (70)reduces to (59), the frequency equation derived in the previous section. The form of (70) is the previous frequency equation without gate resistance, times a factor if 1-x, where x is small. The larger is x, the more the R_g term reduces the oscillation frequency. Also, as I_{SS} increases or V_{sw} decreases, both of which correspond to an increased frequency, the weighting of this term increases.

Next, the effect of the gate resistance on the differential voltage must be accounted for. It was previously assumed that the differential voltage was $V_{in+}(t)$-$V_{in-}(t)$. This is no longer the case. Now, the inputs to the gates of the N_1 and N_2, $V_{ing+}(t)$ and $V_{ing-}(t)$, are given by (71) and (72).

$$V_{ing+}(t) = V_{in+}(t) - I_{cin}(t) R_g \tag{71}$$

$$V_{ing-}(t) = V_{in-}(t) + I_{cin}(t) R_g \tag{72}$$

A difficulty arises in that $I_{Cin}(t)$ is a function of $V_{id+}(t)$, resulting in an equation that is difficult to solve. To solve this problem, first note that the phase of the current into a capacitor has a $\pi/2$ phase shift from the voltage. Since the voltage is a sine wave, the current will be a cosine. Also, the amplitude of the current can be represented as a fraction of the total tail current, I_{SS}. This fraction is fairly constant, although it is a weak function of I_{SS}, V_{sw} and N. This fraction will be called I_{frac}, which simulations show to be about 0.2. Therefore, (71) and (72) can be rewritten as (73) and (74).

$$V_{ing+}(t) = V_{in+}(t) - I_{frac} I_{SS} \cos(2\pi f t) R_g \tag{73}$$

$$V_{ing-}(t) = V_{in-}(t) + I_{frac} I_{SS} \cos(2\pi f t) R_g \tag{74}$$

Therefore, the current through R_g is no longer a function of $V_{in+}(t)$. Without gate resistance, the differential input voltage, $V_{id}(t)$, was given by $V_{in+}(t)$-$V_{in-}(t)$. With gate resistance, the differential input voltage is now found as $V_{ing+}(t)$-$V_{ing-}(t)$, which is shown in (75).

$$V_{idg}(t) = V_{id}(t) - 2I_{frac} I_{SS} \cos(2\pi ft) R_g \tag{75}$$

Now that the differential input voltage includes R_g, the oscillation frequency can be derived again. The oscillation frequency is now given as (76).

$$f = \frac{I_{SS}}{2NV_{sw}(C_{in} + C_{par})} \cdot \left(1 - \frac{2\sqrt{2}NI_{frac} I_{SS} R_g}{\pi V_{sw}}\right) \tag{76}$$

The form of (76) is similar to (70), the equation taking into account the time shift due to R_g. They both multiply the frequency equation without R_g by a 1-x term, where x is small. Again, the weighting of this term is increased if I_{SS} increases or V_{sw} decreases.

To combine the terms, the two factors derived here will be multiplied. This gives (77), the final oscillation frequency equation accounting for time-varying parasitic capacitances and a gate resistance, where C_{par} corresponds to all parasitic capacitances as defined in (69).

$$f = \frac{I_{SS}}{2NV_{sw}(C_{in} + C_{par})} \cdot \left[1 - \frac{I_{SS} R_g}{V_{sw}} \left(\left(\frac{C_{par}}{C_{in} + C_{par}}\right)\left(2 - N\left(\frac{1}{2} - \frac{1}{\pi}\right)\right) + \frac{2\sqrt{2}NI_{frac}}{\pi}\right)\right] \tag{77}$$

The validity of this expression will be verified in section 5.3. Eq (77) gives the designer a lot of information when designing a ring oscillator. Increasing I_{SS} and decreasing V_{sw} will increase the frequency, as expected. However, some of the benefits are lost due to the gate resistance. The parasitic capacitances play an extremely large role in determining the oscillation frequency, and need to be minimized if a high oscillation frequency is required, as it impacts the oscillation frequency in two ways. It adds to the input capacitance and decreases the oscillation frequency. It also increases the weighting of R_g. Eq (77) also emphasizes and quantifies the importance of reducing the gate resistance, as it is highly layout dependant.

4.5 Maximum Frequency

One benefit of finding an analytical frequency equation is that it can be used to determine the theoretical maximum frequency of oscillation. A frequency limit for the delay stage illustrated in Figure 25 is given in [8], and is shown here in (78).

$$f_{max} = \frac{1}{2N} \cdot \frac{\mu}{K_L \cdot L^2} \cdot \left[\left(V_{GS} - V_{TP} \right) - \frac{V_{sw}}{2} \right] \tag{78}$$

where K_L is made up of the contributions of each of the capacitances at the output. This equation shows the limits of the architecture in terms of process parameters and circuit parameters. For example, a designer may see how the maximum frequency is dependent upon a circuit parameter such as N. Alternatively, the designer can see how the maximum frequency is limited by a process parameter, such as the mobility, μ. Similarly, one may also examine how the frequency is modified with technology scaling.

However, (78) does not take into account the required gain per stage to maintain oscillations. The gain around the loop must be 1 at the oscillation frequency, meaning that the DC gain of each stage must usually be greater than 1. A new equation will be derived here which takes in to account the required gain per stage. Eq. (43), derived in section 3.3.1, is used for this derivation. Furthermore, the maximum frequency based on (77), which includes additional parasitics, is also given.

To begin the derivation of the maximum frequency, let us assume that the tail current for each delay stage has a value of I_{SS}. The first requirement is that N_1 and N_2 in Figure 25 be wide enough to have I_{SS} flow through them. Assuming a square current law, the minimum width of the NMOS transistor is given as (79).

$$W_n = \frac{I_{SS} \cdot L}{\frac{1}{2} \mu_n C_{ox} \left(V_{gs} - V_t \right)^2} \tag{79}$$

Once I_{SS} and W_n are known, the transconductance of N_1 and N_2 can be determined. A general equation for transconductance is given in (80). At the midpoint of the swing, I_{SS} is evenly distributed between N_1 and N_2. Therefore, I_D can be set to $I_{SS}/2$ and W can be set to W_n. These substitutions give (81).

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}} \tag{80}$$

$$g_m = \sqrt{I_{SS}\mu_n C_{ox}\frac{W_n}{L}} \tag{81}$$

Next, a minimum value for the gain of the delay stage must be assumed. Let us call this value a_v. The a_v must be at least unity to maintain oscillation in the ring. Normally this value is designed to be higher than unity to provide some robustness. The gain of the delay stage is g_mR, where R is the equivalent resistance of the PMOS load. We determined g_m in (81) and the designer sets a value for a_v. Then, the load resistance can be given by (82).

$$R = \frac{a_v}{g_m} \tag{82}$$

Making the assumption that the tail current fully switches, the voltage swing is given by (83).

$$V_{sw} = I_{SS}R \tag{83}$$

We need to determine the width of the PMOS transistor since it contributes a capacitive load that reduces the frequency. A general equation for the resistance of a MOS transistor in the linear region is given in (84).

$$R = \frac{1}{\mu C_{ox}\frac{W}{L}\left(|V_{gs}| - |V_{tp}| - |V_{ds}|\right)} \tag{84}$$

In (84), $|V_{gs}|$ can be set to V_{DD}-V_{bias}. $|V_{ds}|$ varies between 0 and V_{sw}, so the average value can be taken by setting $|V_{ds}|$ to $V_{sw}/2$. Solving (34) for W_p gives us the width of the PMOS load transistor in (85).

$$W_p = \frac{L}{\mu_p C_{ox} R\left(V_{DD} - V_{bias} - |V_{tp}| - \frac{V_{sw}}{2}\right)} \tag{85}$$

We now have expressions for all the terms in (43), the simplified equation for the frequency. Remember that C_{in} is given as $(2/3)W_nLC_{oxn}$ and C_{gdp} is equal to $(1/2)W_pLC_{oxp}$. After making these substitutions, substitute (85) for W_p. Substitute (83) for V_{sw}, and then (82) for R to take into account the gain per stage requirement. Next, substitute (81) for g_m. Finally, substitute (79) for W_n to have the expression in terms of only circuit and process parameters. The result gives an expression for the maximum possible frequency of

a ring oscillator using the delay stage shown in Figure 25. The expression for the maximum frequency is shown in (86).

$$f_{max} = \frac{3\mu_n\left(V_{gs} - V_{tn}\right)}{4NL^2} \cdot \frac{\dfrac{4\left(V_{DD} - V_{bias} - \left|V_{tp}\right|\right)}{\left(V_{gs} - V_{tn}\right)} - \sqrt{2}\cdot a_v}{\dfrac{4\sqrt{2}\cdot a_v\left(V_{DD} - V_{bias} - \left|V_{tp}\right|\right)}{\left(V_{gs} - V_{tn}\right)} - 2\cdot a_v^2 + 3\dfrac{\mu_n}{\mu_p}} \tag{86}$$

To maximize the frequency, the number of stages, N, must be minimized. For the delay stage used in this example, the minimum number of stages is three. If only two stages are used, each stage must provide 90° of phase shift. However, because each stage contributes only one pole, this requirement cannot be met [4]. Hence, setting N=3, and substituting typical values for a 1.8V, 0.18µm CMOS process into (86), results in a maximum frequency value of approximately 25 GHz. This number is much higher than what is reported in literature. However, this value was obtained using the first order frequency equation. A more accurate value can be obtained by using (77), as will be shown later.

Eq. (86) can still give some insight in the frequency limits of a ring oscillator in terms of process and circuit parameters. As expected, f_{max} is inversely proportional to N, which is consistent with most existing frequency equations. In general, frequency is proportional to I_{SS}. However, in (86), I_{SS} doesn't appear. This is because, as I_{SS} is increased, the minimum value for the width of N_1 and N_2 increase proportionally. The increased width results in extra capacitance which offsets the benefit of the increased current. At the same time, f_{max} is also inversely proportional to L^2. This suggests that f_{max} should increase substantially with technology scaling. However, the square relationship is due to the assumption that there is no velocity saturation. Including velocity saturation would most likely change this relationship from an inverse square to a simple inverse relationship. In technologies where velocity saturation is not an issue, f_t and f_{max} have been shown to have an inverse square relationship with L [8]. However, f_t becomes inversely proportional to L as technology scales [19]. Since f_t and f_{max} track with respect to L [38], it is logical to assume that f_{max} also has an inversely proportional relationship with L. Eq. (86) also shows that increasing a_v, the gain of the delay stage, decreases f_{max}. Therefore, increased robustness limits the maximum performance. Eq (86) shows that increasing electron mobility, μ_n, can increase f_{max}. However, mobility is decreasing with technology scaling due to increasing vertical electric field. The relationship between f_{max} and the overdrive voltage, V_{gs}-V_{tn}, is also important. Increasing the overdrive voltage can increase the maximum frequency. However, voltages are decreasing with technology scaling, reducing the benefit of scaling on the maximum frequency. Plotting (86) with respect to any of its parameters can demonstrate some very interesting relationships.

A more accurate value for the maximum frequency can be obtained by using the method just described, but by substituting the values into (77), instead of (43). Eq. (77) takes into account numerous

parasitic effects. The resulting equation is very large, but once obtained, it can be plotted with respect to any parameter to see how the parameter affects the maximum frequency. Again, using typical values for a 0.18-μm CMOS process, a maximum value for the oscillation frequency of about 9 GHz is obtained.

Chapter 5

Verification

5.1 Introduction

An equation for the oscillation frequency of a ring oscillator has been derived. The result is an analytical equation based on circuit and process parameters. The purpose of the equation is to allow the designer to predict the oscillation frequency and to see the trade-offs between different parameters. It can also show the trends in the frequency as parameters vary. However, for the equation to be useful, it must accurately predict the frequency and the trends. Therefore, a test chip was fabricated to verify the proposed method and the resulting equation. The test chip was fabricated in a 1.8V, 0.18µm CMOS process. In this chapter, the test chip will be described and the measurement results will be compared to the frequency values predicted by the highest-order equation derived here, (77). Comparisons will also be made with existing equations.

5.2 Test Chip

The oscillation frequency equation contains circuit parameters such as N, I_{SS} and V_{sw}. Therefore, the test chip must contain oscillators that can vary these parameters. It is possible to vary I_{SS} and V_{sw} for a ring oscillator, but the number of stages, N, cannot be easily varied. Therefore, numerous oscillators with different numbers of stages will be needed.

5.2.1 Parameter Variation

The test chip contains 6 different ring oscillators, 5 of which are intended for verifying the method and equations, and one which is intended to obtain a high oscillation frequency. The 5 intended for verification

will be discussed here. To maintain consistency between measurements, the dimensions of the transistors in the delay stage are the same for each oscillator, and the different oscillators vary only in the number of stages. The numbers of stages used are 3, 4, 5, 6 and 8.

To vary I_{SS} and V_{sw}, external controls are used. To vary I_{SS}, the circuit shown in Figure 36 is used. The resistor R is an external 1K potentiometer. Varying this value changes I_{in}, which is mirrored in the delay stages. Simulations show that I_{SS} can be varied from 1.0 mA to 5.0 mA over process corners. It is important that only one parameter be varied at a time. Since varying I_{SS} will vary the swing, it is necessary to be able to vary the resistance of the PMOS load to keep the swing constant. Therefore, there is an external bias voltage, V_{bias}, that can vary the resistance of the PMOS load to keep the swing constant.

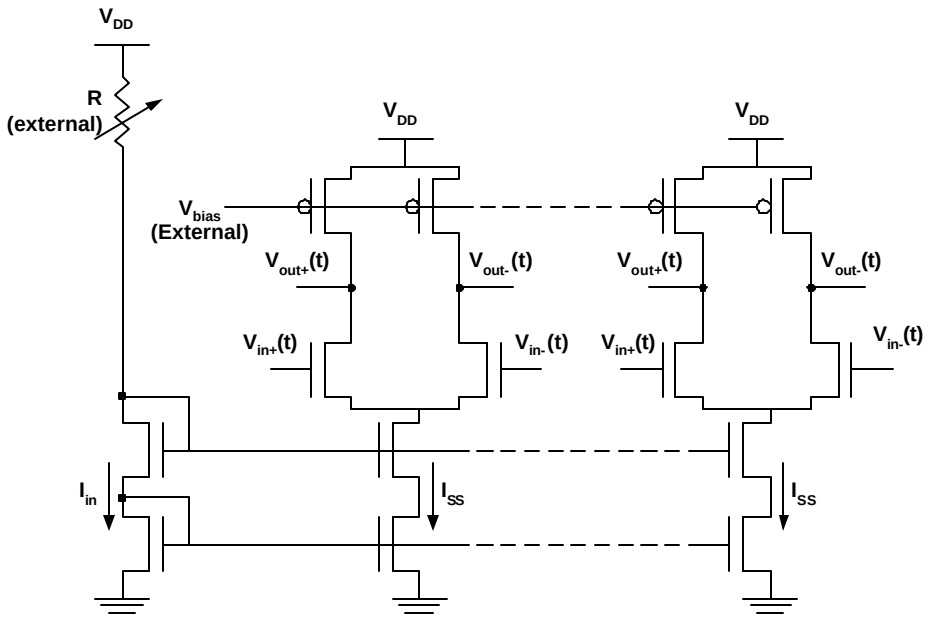


Figure 36: Control Circuit for I_{SS}

The third parameter to vary is V_{sw}. V_{bias} is also used for this purpose. The only difference is that I_{SS} will be kept constant as V_{sw} is varied.

5.2.2 Delay Stage Layout

Each delay stage consists of the source-coupled pair, the PMOS load and the current mirror. A schematic of the delay stage with dimensions is shown in Figure 37. All dimensions are in microns.

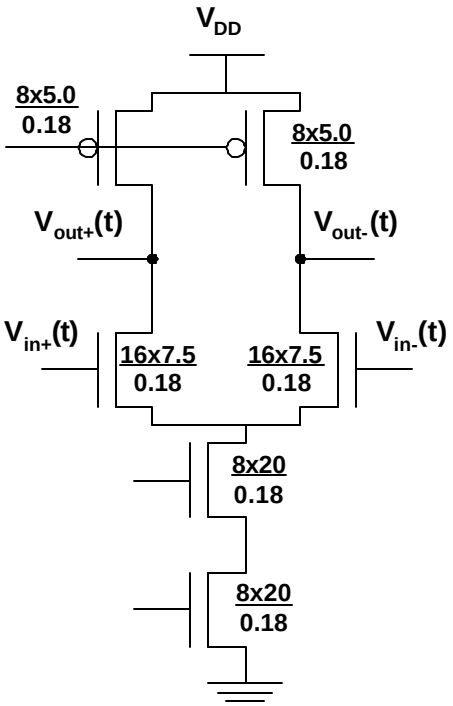


Figure 37: Delay stage with dimensions

The layout of the differential pair was done with reduction of mismatch and parasitics considered at all times. To reduce parasitics, the transistor is folded into 16 fingers. This was considered an optimum number because, although a larger number of fingers would reduce the gate resistance and drain-bulk capacitances, it would have caused issues with regards to the aspect ratio of the delay stage. To reduce mismatch, a common-centroid geometry was used, as illustrated in Figure 38, where A and B correspond to fingers of the two source-coupled transistors. Care was also taken to ensure that the two transistors see the same parasitics. The value for the gate resistance, R_g, that is to be used in (77) is layout dependent. It is based on the sheet resistance of the gates of the source-couples pair transistors. This value for this layout was calculated to be 11.9 Ω.

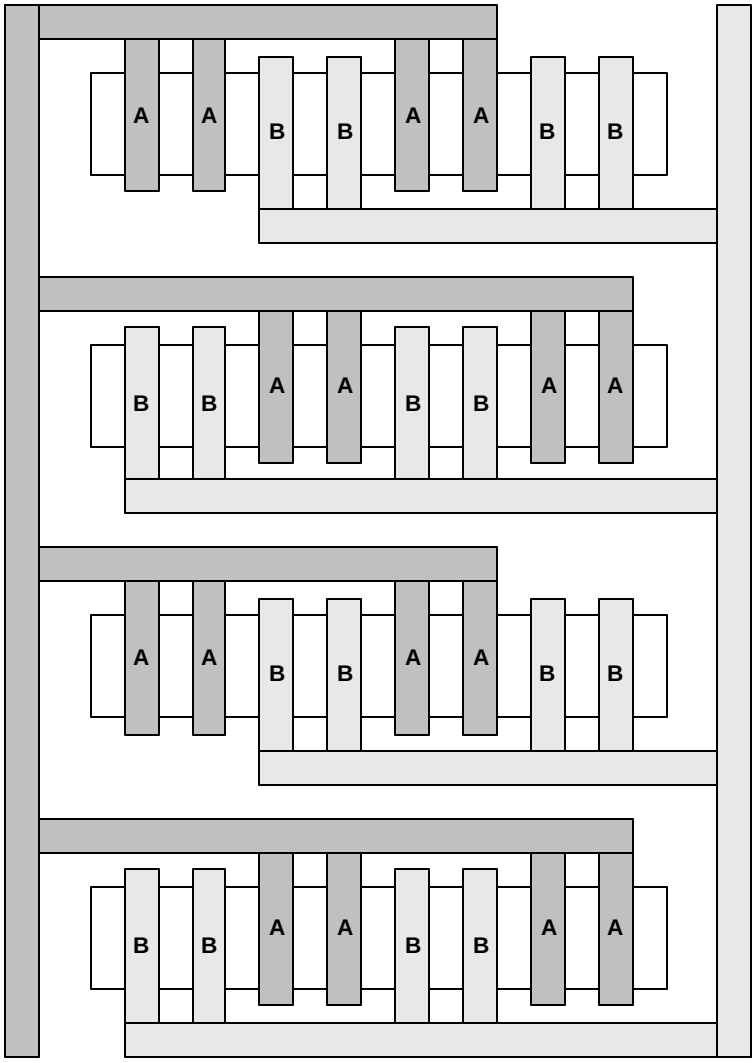


Figure 38: Common-Centroid Layout of source-coupled pair

The layout of the PMOS load transistors was done in a similar fashion. It is also common-centroid, but contains only two rows as each transistor is folded into 8 fingers. The layout for the entire delay stage is shown in Figure 39.

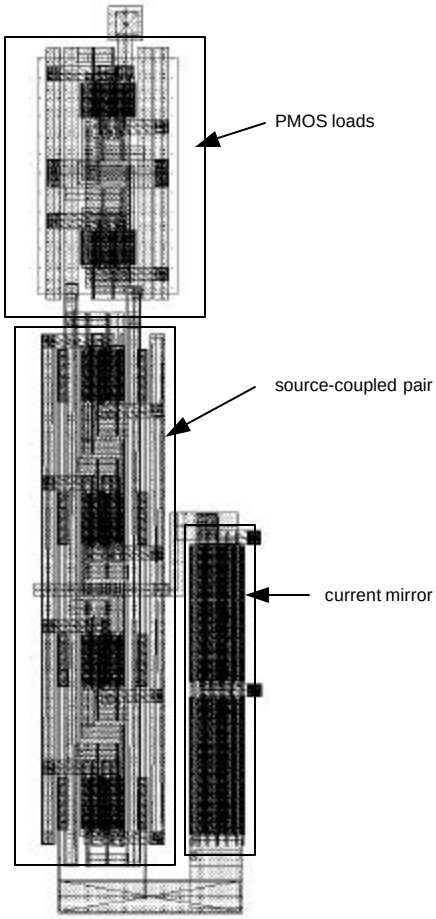


Figure 39: Layout of Delay Stage

5.2.3 Test Chip Layout

The chip contains 6 ring oscillators; 2 with 3 stages, and 1 of each with 4, 5, 6 and 8 stages. Due to pad limitations, many inputs and outputs need to be shared. Therefore, the sharing is done in such a way that only one VCO will be on at a time. This is done using external row and column select signals, as shown in Figure 40.

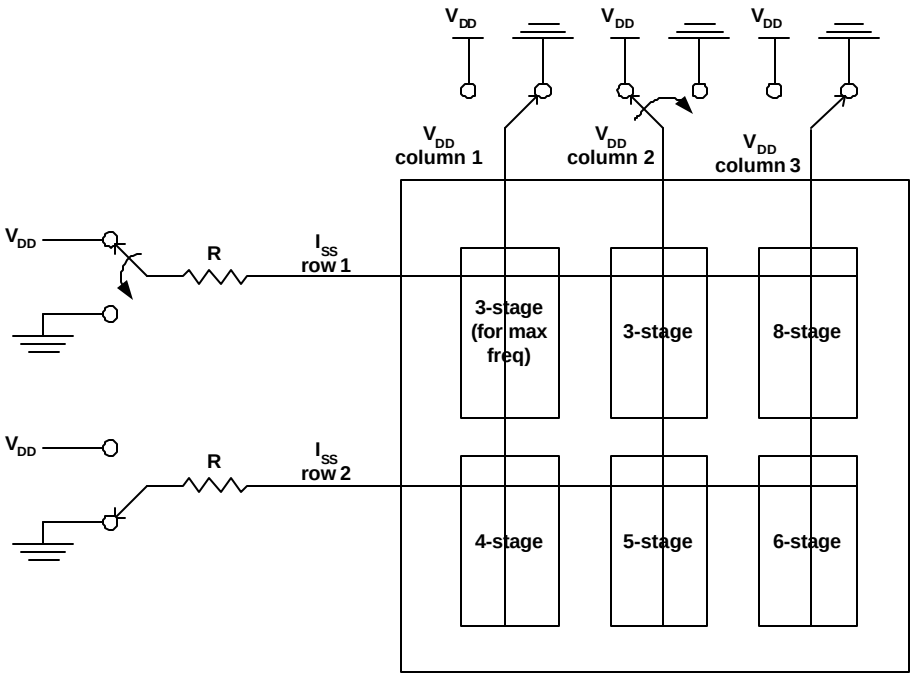


Figure 40: Layout of chip and how row and column are selected

The row is selected by connecting the resistor of the current source of one row to V_{DD} and the other to ground. Therefore, only the ring oscillators of one row will have a tail current. The oscillators in the row without the tail current will not be able to oscillate. The column is selected by connecting the V_{DD} inputs of the delay stage of only one column to V_{DD}, and connecting the other two to ground. Therefore, only one ring oscillator will have both power to the delay stage and a tail current, and therefore only one ring oscillator will be on. In Figure 40, the 1st row and the 2nd column are selected, meaning that the 3-stage VCO is on and the remaining 5 are off.

Other inputs and outputs are also shared. There is one PMOS load bias signal for each row. There is also one "swing out" output for each row. The purpose of "swing_out" is to determine the voltage swing of the VCO. Therefore, a replica of the delay stage with the same tail current and PMOS load is used so that the maximum swing is known. The circuit to generate "swing_out" is shown in Figure 41.

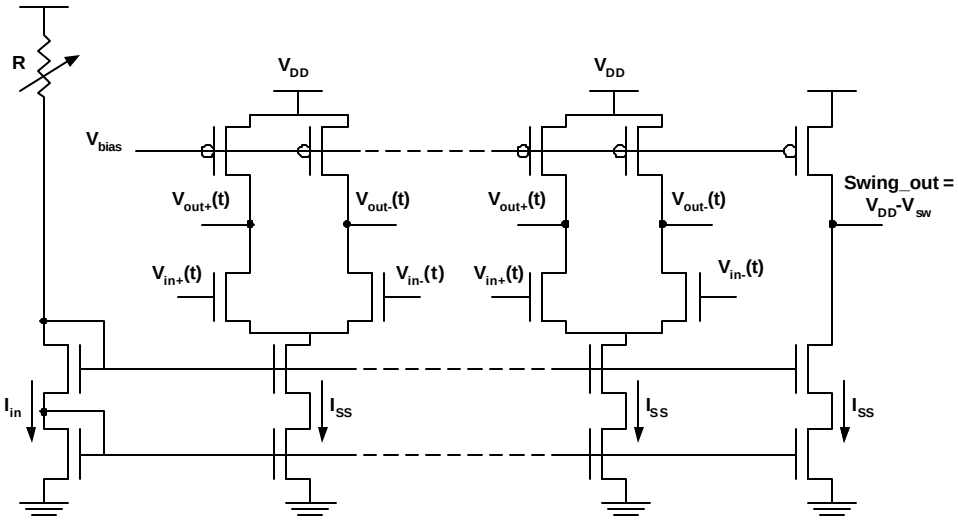


Figure 41: "Swing Out" is generated using a replica stage

A micrograph for the test chip is shown in Figure 42. The test chip is 1000µm x 1000µm.

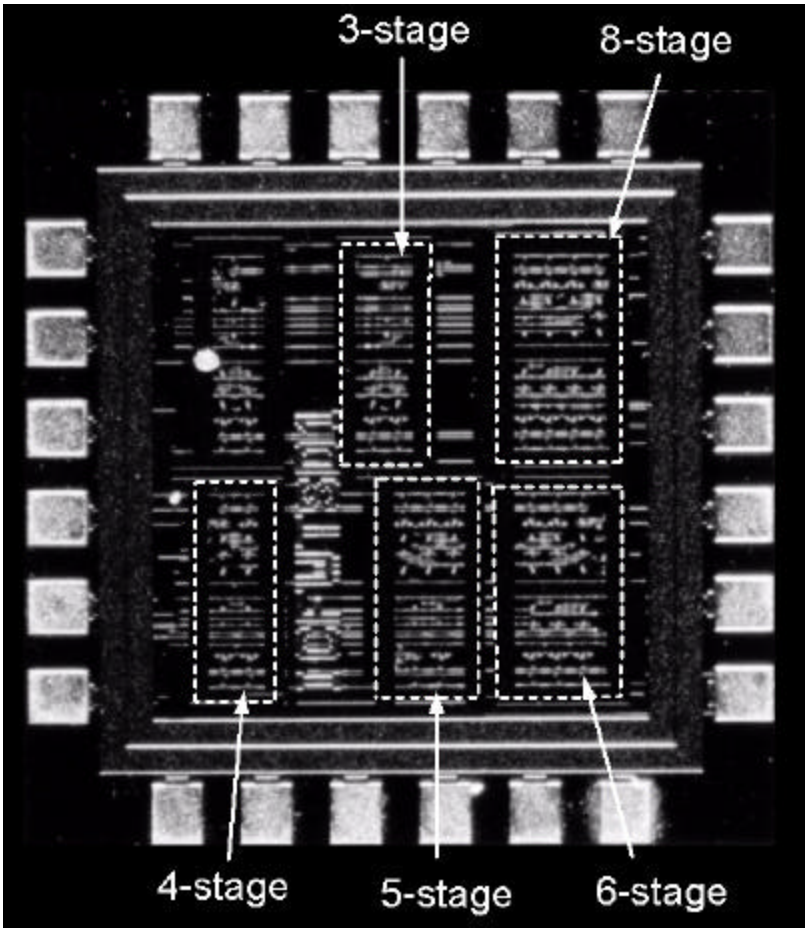


Figure 42: Micrograph of Test Chip

The test board is shown in Figure 43. The test chip has been packaged in a 28-pin Quad Flatpack No lead (QFN) package.

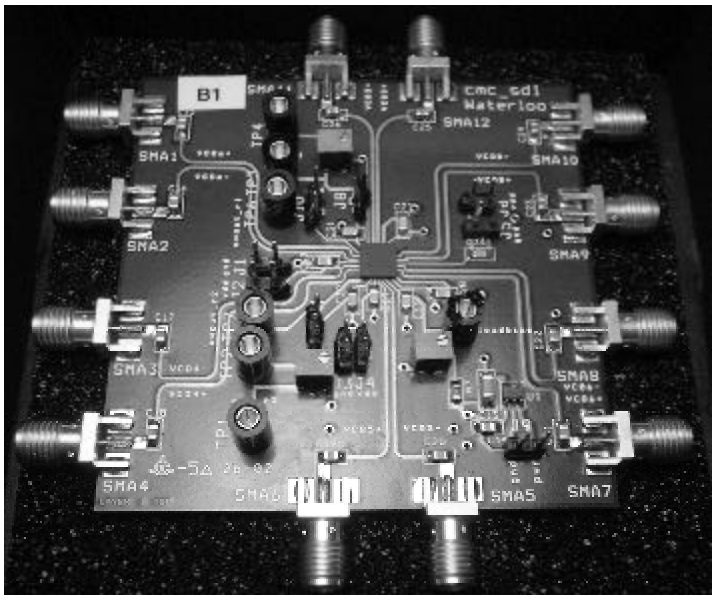


Figure 43: Test Board

5.3 Results

The experimental results show that the oscillation frequency is in good agreement with the values predicted by (77), the final oscillation frequency equation. The experimental results presented here are average values of measurements from four test chips. The error bars show the minimum and maximum measured frequency for each data point. The average error while varying N from 3 to 8, I_{SS} from 2mA to 5mA and V_{sw} from 250mV to 500mV is 8.2%. A range of the measured data is plotted with the predicted values in Figure 44 to Figure 46. Figure 44 shows the relationship between frequency and I_{SS} for V_{sw}=350mV and N=4, 6 and 8. Figure 45 shows the relationship between frequency and V_{sw} for I_{SS}=3.5mA and N=4, 6 and 8. Figure 46 shows the relationship between frequency and N for I_{SS}=3.5mA and V_{sw}=300mV and 500mV.

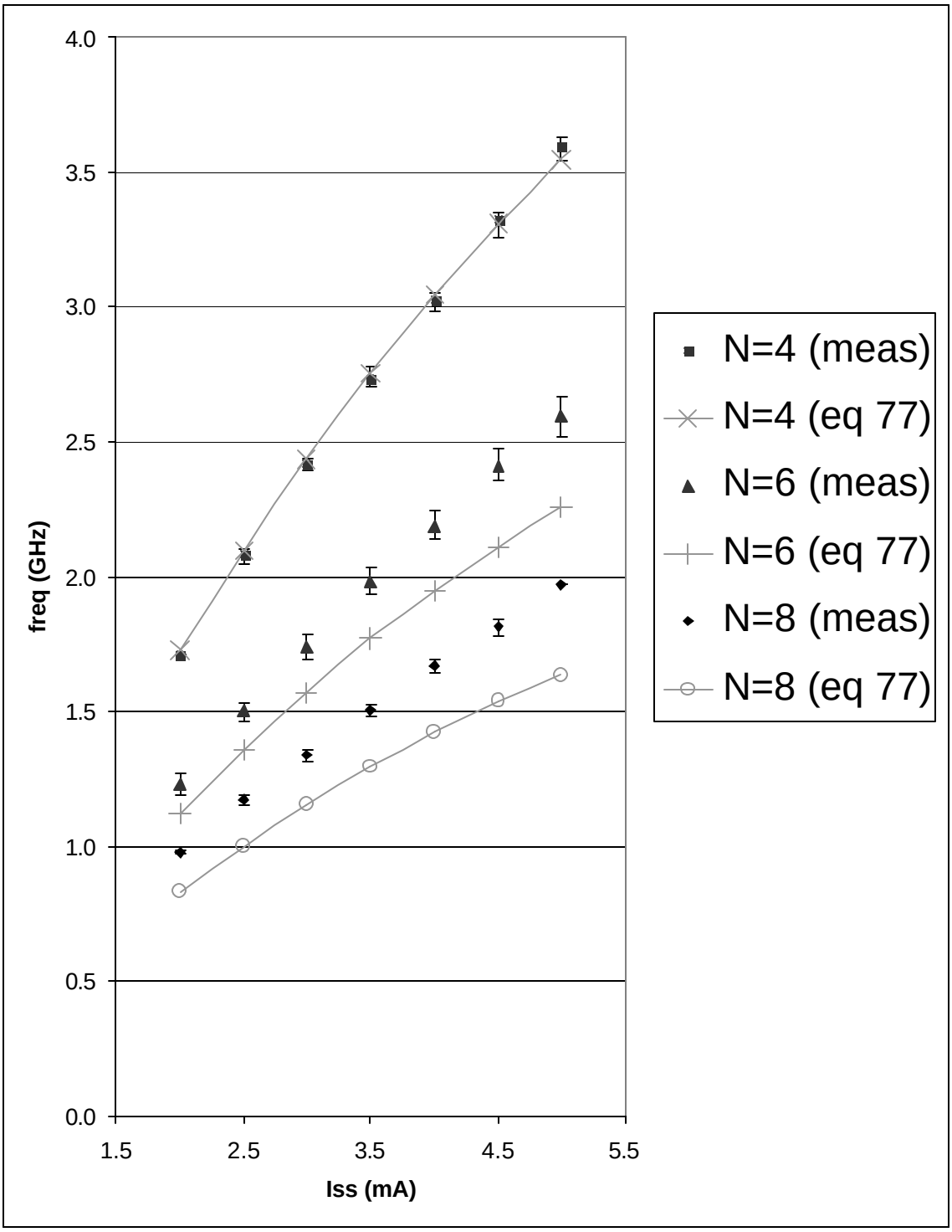


Figure 44: Experimental and calculated results for frequency versus I_{SS}

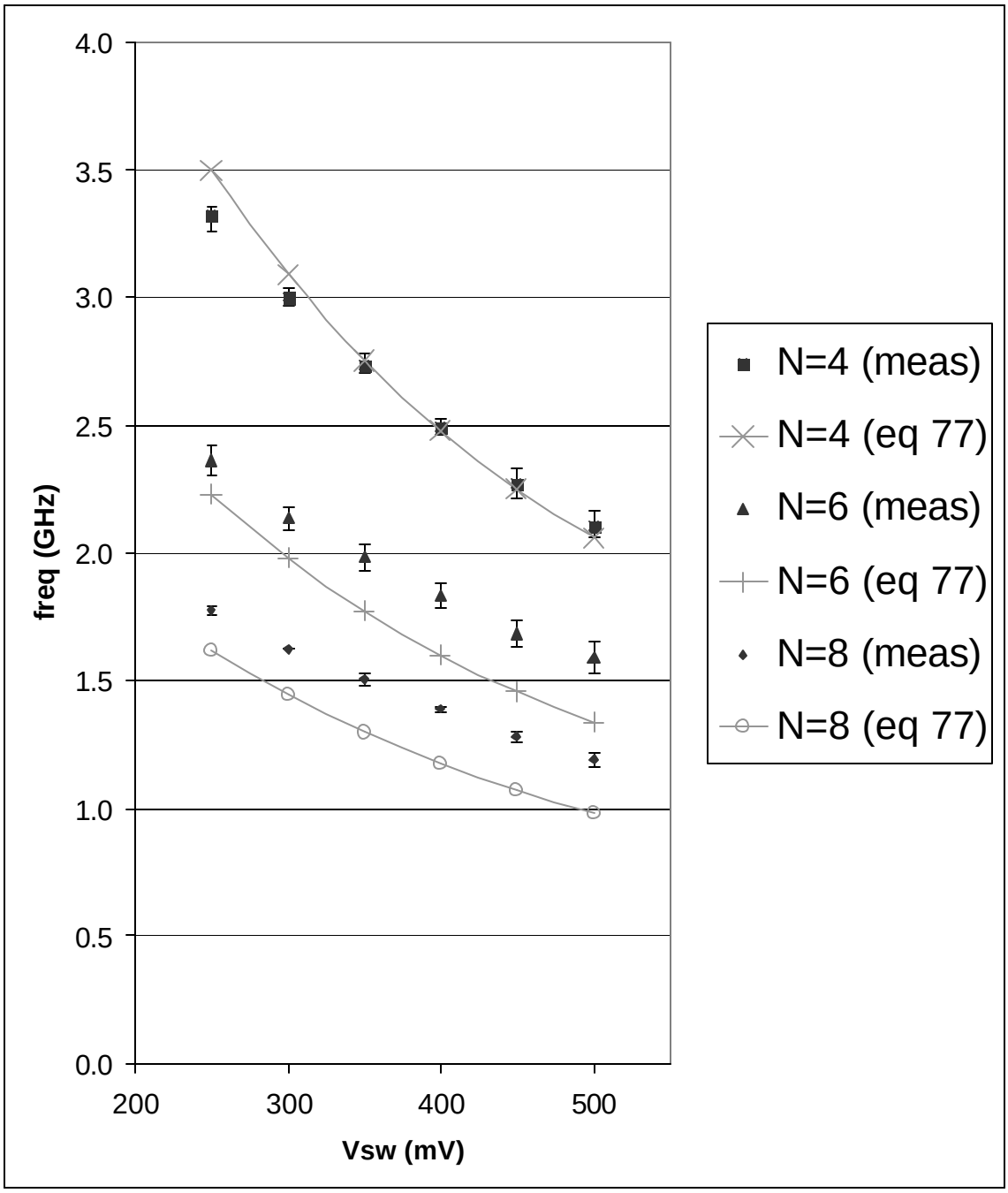


Figure 45: Experimental and calculated results for frequency versus V_{sw}

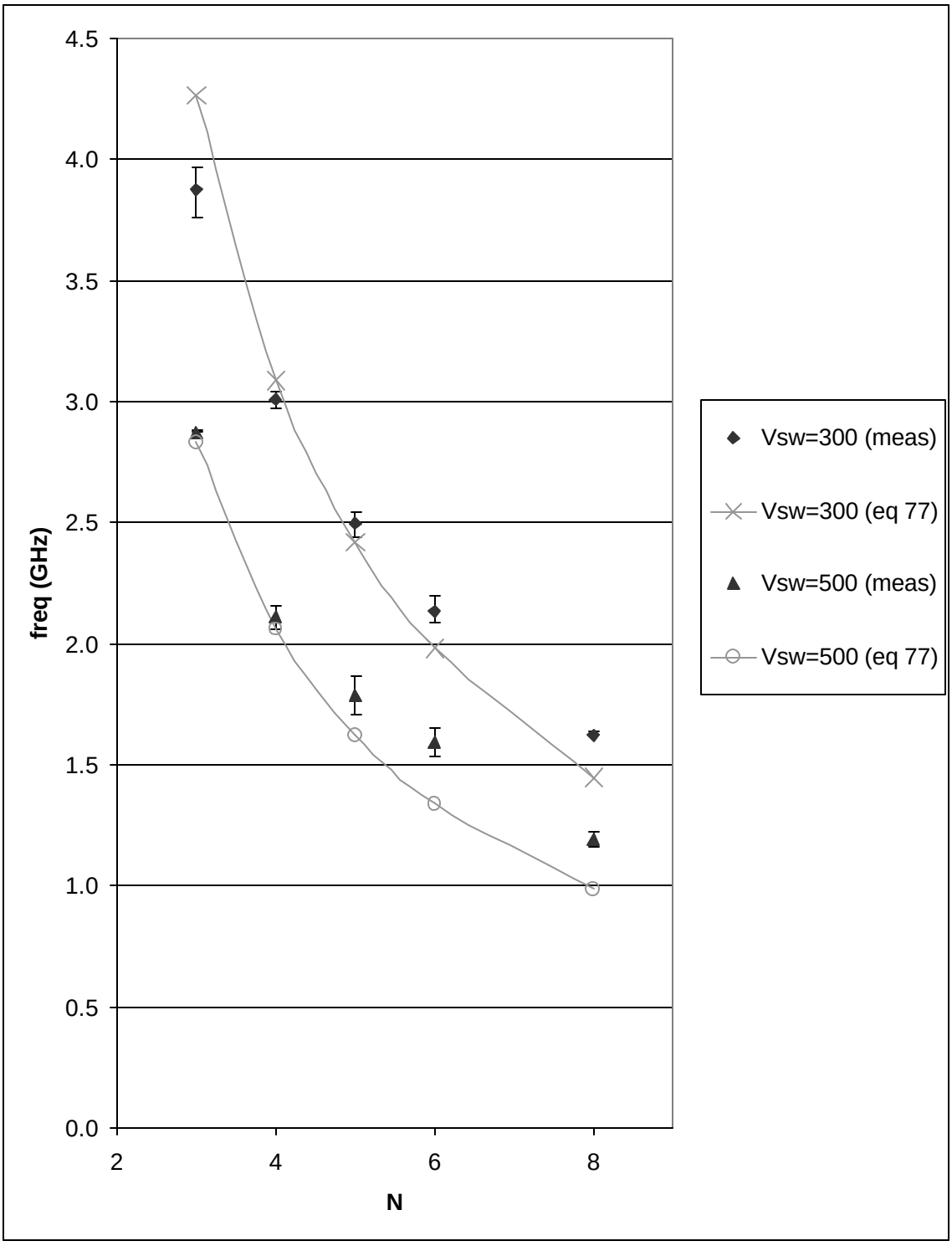


Figure 46: Experimental and calculated results for frequency versus N

These figures show that the frequency equation derived here is able to accurately predict the value of the oscillation frequency over a wide range of I_{SS}, V_{sw} and N values. These figures also show that including the gate resistance is important to obtain an accurate prediction, especially at high frequencies. Without including the gate resistance, the equation derived here, (59), and existing equations such as (14), (18) and (20), suggest that the frequency should increase linearly with the tail current and inversely with the voltage swing. However, simulations and measurements show that at high frequencies, this relationship does not hold. High oscillation frequencies correspond to a high I_{SS} and/or a low V_{sw}.

As the tail current increases, the gains in frequency are not proportional. Notice that in Figure 44, the frequency does not increase linearly with I_{SS}. Since increasing the tail current increases the power, this suggests a diminishing return with increased I_{SS}. However, Eq (77) predicts the trend with respect to increasing I_{SS} very accurately, as demonstrated in Figure 47. In Figure 47, the frequency is normalized to the frequency corresponding to the lowest I_{SS} value for both the experimental and predicted results. Without a gate resistance, other equations suggest that the frequency should have a linear relationship with I_{SS}. This is shown by the simple model line in Figure 47, which begins at 1 and linearly increases to 2.5. This corresponds to a 2.5 times increase in I_{SS}. However, the experimental results show that actual increase in frequency for a 2.5 times increase in current is just over 2. Eq (77), which includes the effect of the gate resistance, very accurately predicts this actual non-linearity in the frequency-I_{SS} relationship.

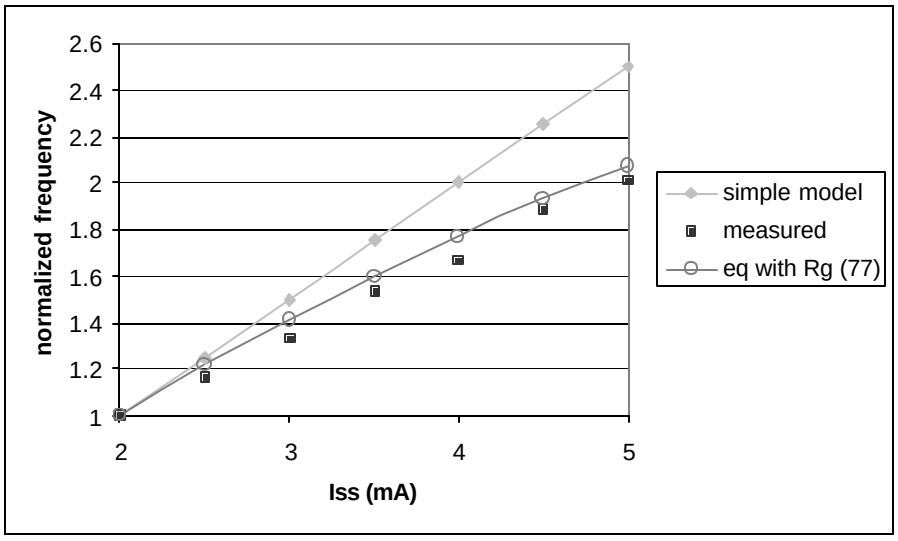


Figure 47: Normalized frequency vs. I_{SS}

A similar trend can be found with V_{sw}. Without the gate resistance, existing equations suggest that decreasing the voltage swing should have an inverse increase in the frequency. However, as V_{sw} gets low, which corresponds to higher frequencies, this relationship doesn't hold. This trend is shown in Figure 48. In Figure 48, the frequency is again normalized and plotted against the inverse of the voltage swing. In this

case, V_{sw} starts at 0.5V ($1/V_{sw}$=2). V_{sw} then decreases by a factor of 2, to 0.25V ($1/V_{sw}$=4). Since the V_{sw} was halved, a simple model would expect the frequency to double, as shown by the straight line in Figure 48. However, the model with gate resistance predicts, with some error, that the actual increase in frequency is much less.

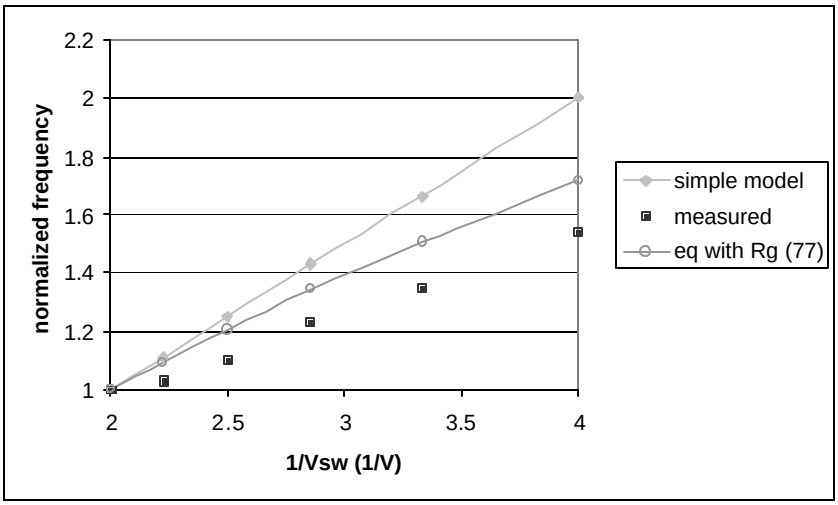
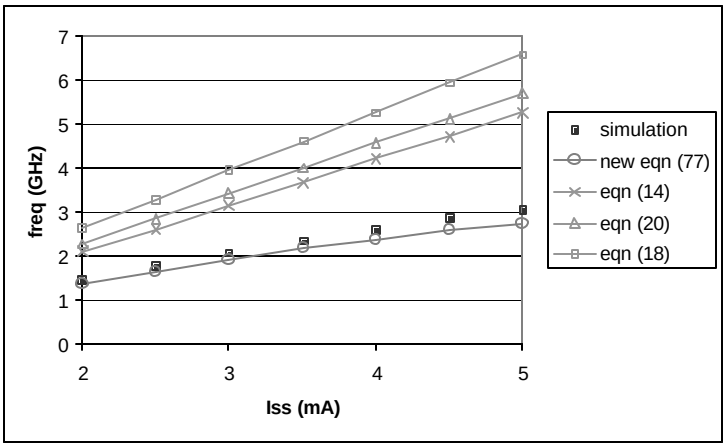


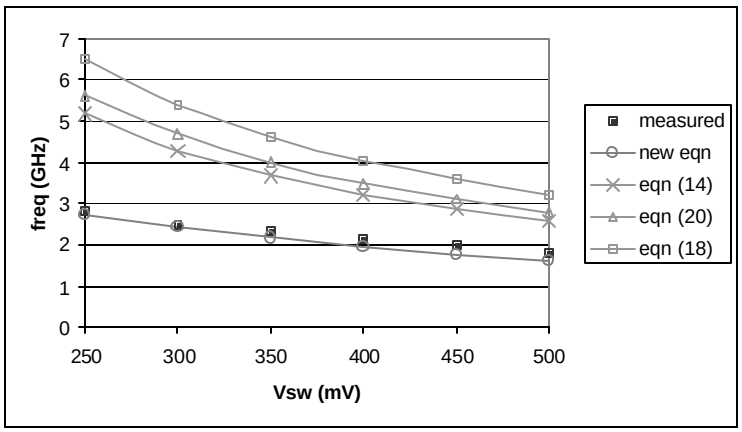
Figure 48: Normalized frequency vs. V_{sw}.

5.3.1 Comparison

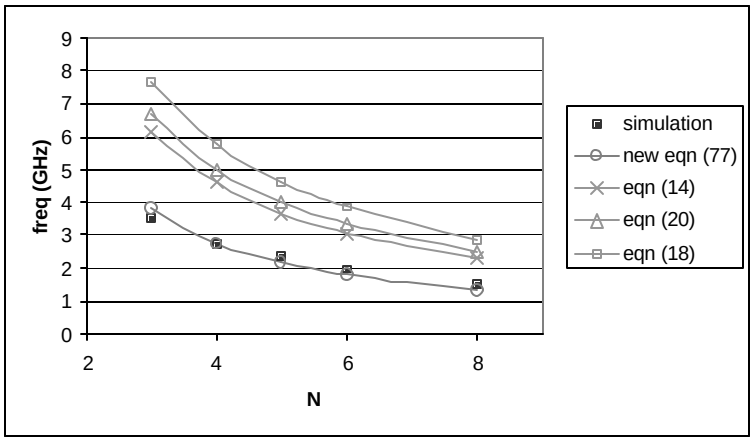
As discussed in section 3.2, there are numerous existing equations available to predict the oscillation frequency. In this section, the final equation derived using the proposed method will be compared with these other equations. The comparisons are made in Figure 49. Figure 49a) shows frequency vs. I_{SS} for N=5 and V_{sw}=350mV. Figure 49b) shows frequency vs. V_{sw} for N=5 and I_{SS}=3.5mA. Figure 49c) shows frequency vs. N for I_{SS}=3.5mA and V_{sw}=350mV. The results show that the equation derived here, (77), provides the most accurate results. The differences are due to varying assumptions made in the equations' derivations. First, all other equations ignored the gate resistance, which has a large effect at high frequencies. Also, the difference between (77) and (14) is that (14) does not take into account the gate-drain overlap capacitance. Moreover, (14) does not let the designer know what values to use for the drain-bulk capacitances. Eq. (18) has similar issues as (14). This equation also overestimates the frequency due to the ln(2) factor that arises from the assumptions made in the equation's derivation. Eq. (20) contains similar parasitic capacitance values as (77). The differences are the Miller effect on the gate-drain overlap capacitance and the weighting of the drain-bulk capacitances. Moreover, (20) also contains a 0.8 factor related to the equation's derivation and seems to overestimate the frequency.



a) frequency vs. I_{SS}



b) frequency vs. V_{sw}



c) frequency vs. N

Figure 49: Equation Comparison for a) frequency vs. I_{SS} b) frequency vs. V_{sw} c) frequency vs. N

Chapter 6

Conclusions

Ring oscillators are commonly studied due to their use in communications circuits such as PLLs and clock and data recovery circuits (CDRs). When designing a ring oscillator, an accurate analytical equation for the oscillation frequency is important. First, the equation can be used to predict the oscillation frequency. Second, the analytical equation can be used to show the designer the tradeoffs between the circuit parameters. Also, the process parameters can show the designer the limitations of the circuit and how these will change with scaling. There are currently numerous equations to predict the oscillation frequency of a ring oscillator. These equations attempt to find an expression for the delay of one stage, and use this to predict the frequency. In this thesis, a new method is proposed which, instead of finding an expression for the delay, assumes a sinusoidal voltage waveform and uses this to create a system of equations which can be reduced and then solved for the oscillation frequency.

The main contributions of this thesis have been:

1. A new method to derive an analytical equation for the oscillation frequency of a ring oscillator. The method is able to take into account many parasitics and secondary effects. The parasitics can be time-varying, such as the drain-bulk capacitance. The gate resistance can also be included as it becomes important at high frequencies.
2. An analytical equation for the oscillation frequency of a ring oscillator based on a common topology has been derived using the proposed method. The final equation for the oscillation frequency of this topology is given in (77). A test setup that varies the relevant parameters over a wide range results in an average error of 8.2% between the predicted and measured frequency values. The results also show the importance of including the gate resistance in the model for ring oscillators with high frequencies of oscillation. The final equation also shows that the frequency reduction due to the gate-drain overlap and drain-bulk capacitances is higher than previously reported. The predicted frequencies are more accurate than those of existing equations.

3. A test chip in a 0.18μm CMOS process to validate the proposed method and derived oscillation frequency equation.

Appendix A

Simplification of gate-drain overlap term

This appendix explains the simplification performed when determining the multiplier of the gate-drain overlap term. In section 4.3, the gate-drain overlap capacitance is included in the derivation of the oscillation frequency equation. The weighting of this term is found to be $(1+\cos(\pi/N))\bullet C_{gdov}$. Some simplification is necessary to result in this simple expression. To more easily show the simplifications, unrelated terms will be removed from the frequency equation.

If the method is followed as outlined in section 4.3, but with the only additional parasitic capacitance included being the gate-drain overlap capacitance, f_1 and f_2, as shown in (87) and (88) will be found.

$$f_1 = \frac{1}{4}\cdot\frac{\pi-2}{\pi R\left(C_{in}+C_{gdp}+W_n Cgdo_n\left(1+\cos\left(\frac{\pi}{N}\right)-\sin\left(\frac{\pi}{N}\right)\right)\right)} \tag{87}$$

$$f_2 = \frac{1}{4}\cdot\frac{(2-\pi)NV_{sw}+4\pi I_{SS}R}{\pi NV_{sw}R\left(C_{in}+C_{gdp}+W_n Cgdo_n\left(1+\cos\left(\frac{\pi}{N}\right)+\sin\left(\frac{\pi}{N}\right)\right)\right)} \tag{88}$$

To obtain an expression for the overall frequency, these expressions must be averaged. Ideally, the final expression will not contain an excessive number of terms so that the effect of each component can be easily seen by the designer. However, if these two relatively simple expressions are averaged, the resulting expression will contain many terms. This is because of a small difference in the denominator. The denominator for f_1 contains a $\left(1+\cos\left(\frac{\pi}{N}\right)-\sin\left(\frac{\pi}{N}\right)\right)$ term whereas the expression for f_2 contains a

$\left(1+\cos\left(\frac{\pi}{N}\right)+\sin\left(\frac{\pi}{N}\right)\right)$ term. The sign difference for the sin(π/N) term causes the problem. If the average of f_1 and f_2 is taken without any simplification, (89) results.

$$f=\frac{I_{SS}}{2NV_{sw}}\cdot\frac{1+\frac{W_nCgdo_n}{C_{in}+C_{gdp}}\left(1+\cos\left(\frac{\pi}{N}\right)+\sin\left(\frac{\pi}{N}\right)\right)\left(N\left(\frac{1}{2}-\frac{1}{\pi}\right)-1\right)}{\left(C_{in}+C_{gdp}+\frac{2W_nCgdo_n}{C_{in}+Cgdo_p}\left(C_{in}+C_{gdp}+W_nCgdo_n\cos\left(\frac{\pi}{N}\right)\right)\right)} \tag{89}$$

To simplify the expression, it is desirable to make the denominator of f_1 and f_2 of the same form. To do this, the following simplifications will be made:

$$\left(1+\cos\left(\frac{\pi}{N}\right)-\sin\left(\frac{\pi}{N}\right)\right)\rightarrow\left(1+\cos\left(\frac{\pi}{N}\right)\right) \tag{90}$$

$$\left(1+\cos\left(\frac{\pi}{N}\right)+\sin\left(\frac{\pi}{N}\right)\right)\rightarrow\left(1+\cos\left(\frac{\pi}{N}\right)\right) \tag{91}$$

Therefore, the sin(π/N) term has been removed, making the denominators of the same form. This will first be qualitatively, and then quantitatively justified. To qualitatively justify this simplification, note that the ring oscillator in the example, N must be 3 or greater. As N gets larger, the sin(•) term will decrease and the cos(•) term will increase, and 1+cos(π/N) will be much greater than sin(π/N). The relative magnitudes of these terms are shown in Figure 50.

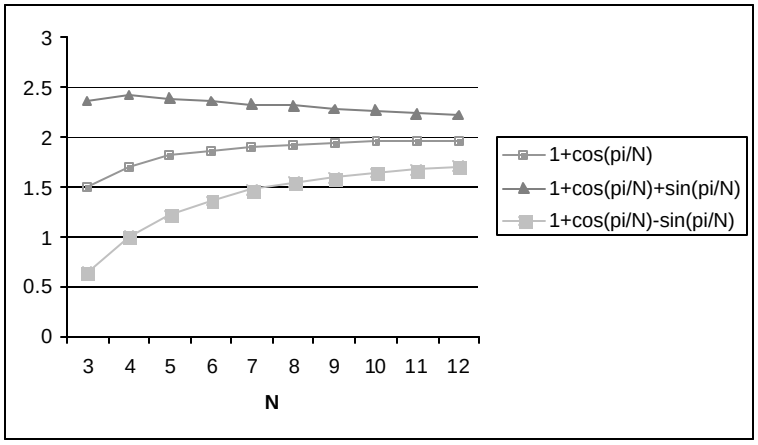


Figure 50: Effect of ignoring the sin(p/N) term

For small N's, this difference can be substantial, but as N increases, the error will approach zero. Also, because the signs of the sin(•) terms are different, some of the terms will cancel themselves, or reduce when the expressions are combined. With this simplification, f_1 and f_2 become:

$$f_1 = \frac{1}{4} \cdot \frac{\pi - 2}{\pi R\left(C_{in} + C_{gdp} + W_n Cgdo_n \left(1 + \cos\left(\frac{\pi}{N} \right) \right) \right)} \tag{92}$$

$$f_2 = \frac{1}{4} \cdot \frac{(2-\pi) N V_{sw} + 4\pi I_{SS} R}{\pi N V_{sw} R\left(C_{in} + C_{gdp} + W_n Cgdo_n \left(1 + \cos\left(\frac{\pi}{N} \right) \right) \right)} \tag{93}$$

Using these expressions, the new frequency expression becomes:

$$f = \frac{I_{SS}}{2NV_{sw}\left(C_{in} + C_{gdp} + \left(1 + \cos\left(\frac{\pi}{N} \right) \right) W_n Cgdo_n \right)} \tag{94}$$

This expression is much simpler than (89), and the effect of the gate-drain overlap capacitance can be easily seen. To quantify the error, the error between the predicted frequency using (89) and (94) has been plotted with respect to N for typical capacitance values.

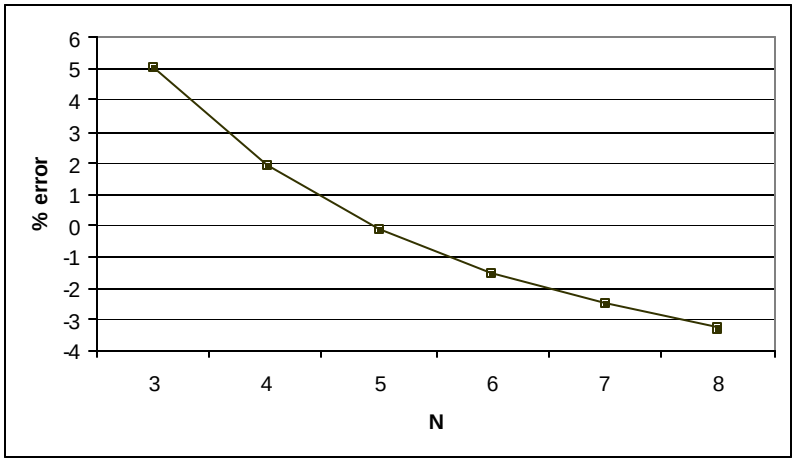


Figure 51: % error due to gate-drain overlap simplification

Figure 51 shows that the error due to the simplification is less than 5% for practical values of N, meaning that removing the sin(π/N) terms does not cause a large error, but does substantially simplify the analytical expression for the oscillation frequency, enabling the designer to easily see the contribution of the gate-drain overlap capacitance.

Appendix B

Simplification of the junction and sidewall capacitance terms

This appendix explains the simplification performed for the junction and sidewall capacitance components of the oscillation frequency equation derived in section 4.3. The weightings of the parasitic capacitance terms are repeated here for convenience.

$$Cjun_n = \frac{Cj_n Ad_n}{\left(1+\frac{V_{DD}}{pb_n}\right)^{mj_n}}\left[2 - mj_n\left(1-\frac{1}{\left(1+\frac{V_{DD}}{pb_n}\right)}\right)\right] \tag{95}$$

$$Cjunsw_n = \frac{Cjsw_n Pd_n}{\left(1+\frac{V_{DD}}{pbsw_n}\right)^{mjsw_n}}\left[2 - mjsw_n\left(1-\frac{1}{\left(1+\frac{V_{DD}}{pbsw_n}\right)}\right)\right] \tag{96}$$

$$Cjun_p = 2Cj_p Ad_p \tag{97}$$

$$Cjunsw_p = 2Cjsw_p Pd_p \tag{98}$$

where $Cjun_n$ is the area junction capacitance of N_1 and N_2, $Cjunsw_n$ is the sidewall capacitance of N_1 and N_2, $Cjun_p$ is the area junction capacitance of P_1 and P_2 and $Cjunsw_n$ is the sidewall capacitance of P_1 and P_2.

However, some simplification is needed to get the junction and sidewall capacitance terms of the forms in (95)-(98). Again, the main reason for the simplification is to create an analytical equation that the designer can use to easily see the effects of these parasitics.

To explain the simplification, only the relevant terms will be discussed, and not the whole equation. To begin, the term corresponding to the junction capacitance of the NMOS differential pair will be discussed. Without simplification, the junction capacitance results in the term shown in (99) in the denominator of the frequency equation.

$$\frac{2Cj_n Ad_n}{1-mj_n}\left[\frac{pb_n+(2-mj_n)V_{dd}}{\left(\frac{pb_n+V_{dd}}{pb_n}\right)^{mj_n}}-\frac{pb_n+(2-mj_n)V_{dd}-\frac{2-mj_n}{2}V_{sw}}{\left(\frac{pb_n+V_{dd}-\frac{V_{sw}}{2}}{pb_n}\right)^{mj_n}}\right] \tag{99}$$

This term shows how the junction capacitance is related to parameters such as the voltage swing, V_{sw}, and the area junction grading coefficient, mj_n. However, the form of the equation makes the effects of these parameters difficult for the designer to see. Therefore, some simplification is needed. Algebraic manipulation can result in the from shown in (100)

$$\frac{2Cj_n Ad_n (pb_n)^{mj_n}}{1-mj_n}\left[(2-mj_n)(pb_n+V_{DD})^{1-mj_n}\left[1-\left(1-\frac{V_{sw}}{2(pb_n+V_{DD})}\right)^{1-mj_n}\right]-\frac{pb_n(1-mj_n)}{(pb_n+V_{DD})^{mj_n}}\left[1-\left(1-\frac{V_{sw}}{2(pb_n+V_{DD})}\right)^{-mj_n}\right]\right] \tag{100}$$

This form is useful because the binomial expansion can be used to simplify it. The binomial expansion for $(1\pm x)^n$ is shown in (101).

$$(1\pm x)^n = 1\pm nx+\frac{n(n-1)}{2!}x^2\pm\frac{n(n-1)(n-2)}{3!}x^3+\ldots \tag{101}$$

If $x << 1$, then (101) can be simplified to (102).

$$(1\pm x)^n \approx 1\pm nx \tag{102}$$

There are two terms in (100) than can be simplified using the binomial expansion. The simplifications are shown in (103) and (104).

$$\left(1-\frac{V_{sw}}{2(pb_n+V_{DD})}\right)^{1-mj_n} \approx 1-(1-mj_n)\frac{V_{sw}}{2(pb_n+V_{DD})} \tag{103}$$

$$\left(1-\frac{V_{sw}}{2(pb_n+V_{DD})}\right)^{-mj_n} \approx 1-(-mj_n)\frac{V_{sw}}{2(pb_n+V_{DD})} \tag{104}$$

This simplification is valid because $V_{sw}/2(pb_n+V_{DD})$ will be about an order of magnitude smaller than 1 for typical values. Making these substitutions into (100) and some algebraic manipulation results in (105).

$$Cj_n Ad_n V_{sw}\left(\frac{pb_n}{pb_n+V_{dd}}\right)^{mj_n}\frac{1}{(pb_n+V_{dd})^{1-mj_n}}\left[(2-mj_n)(pb_n+V_{dd})^{1-mj_n}+\frac{mj_n pb_b}{(pb_n+V_{dd})}\right] \tag{105}$$

Further algebraic manipulation results in the final simplified expression for the effect of the junction capacitance of the NMOS differential pair, given in (106).

$$Cj_n Ad_n V_{sw}\frac{1}{\left(1+\frac{V_{dd}}{pb_n}\right)^{mj_n}}\left[2-mj_n\left(1-\frac{1}{\left(1+\frac{V_{dd}}{pb_n}\right)}\right)\right] \tag{106}$$

This is the final form used in the oscillation frequency equation.

To perform the simplification of the sidewall capacitance term, it can be noted that the sidewall term is of the same form as the junction term. The only difference is that Cj must be replaced by Cjsw, mj by mjsw, pb by pbsw and Ad by Pd. The sidewall capacitance term as it is derived in the denominator is given in (107), and with simplification in (108).

$$\frac{2Cjsw_n Pd_n}{1-mjsw_n}\left[\frac{pbsw_n+(2-mjsw_n)V_{DD}}{\left(\frac{pbsw_n+V_{DD}}{pbsw_n}\right)^{mjsw_n}}-\frac{pbsw_n+(2-mjsw_n)V_{DD}-\frac{2-mjsw_n}{2}V_{sw}}{\left(\frac{pbsw_n+V_{DD}-\frac{V_{sw}}{2}}{pbsw_n}\right)^{mjsw_n}}\right] \tag{107}$$

$$Cjsw_n Pd_n V_{sw} \frac{1}{\left(1+\frac{V_{DD}}{pbsw_n}\right)^{mjsw_n}} \left[2 - mjsw_n \left(1 - \frac{1}{\left(1+\frac{V_{DD}}{pbsw_n}\right)}\right)\right] \tag{108}$$

The error in the NMOS sidewall and junction capacitance terms due to this simplification is shown in Figure 52 as a function of V_{sw} using typical values for a 1.8V, 0.18µm CMOS process. The error in the junction and sidewall capacitance term is less than 2% for typical V_{sw} values. Also, since these capacitances are only a fraction of the total capacitances, the error in the frequency will be substantially less than 1%.

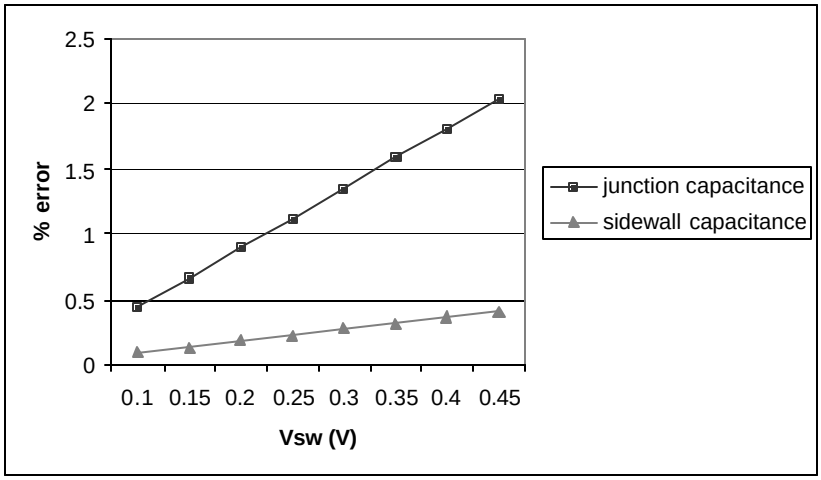


Figure 52: % error in capacitance values due to simplification of junction and sidewall capacitance terms for the NMOS transistors

A similar method can be used to simplify the junction and sidewall capacitance terms for the PMOS load transistors. With simplification, the junction capacitance term appears in the denominator of the frequency equation as shown in (109).

$$\frac{2Cj_p Ad_p}{1 - mj_p}\left[pb_p - \frac{pb_p - (2 - mj_p)V_{sw}}{\left(\frac{pb_p - \frac{V_{sw}}{2}}{pb_p}\right)^{mj_p}}\right] \tag{109}$$

Again, the form of this equation does not make it easy for the designer to see how the parameters affect the weighting of the junction capacitance term. Therefore, simplification is necessary. Algebraic manipulation can be used on (109) to obtain (110).

$$\frac{2Cj_p Ad_p pb_p}{1-mj_p}\left[1-\left(2-mj_p\right)\left(1-\frac{V_{sw}}{2pb_p}\right)^{1-mj_p}+\left(1-mj_p\right)\left(1-\frac{V_{sw}}{2pb_p}\right)^{-mj_p}\right] \tag{110}$$

Eq (110) is in a form that can be simplified using the binomial expansion. Note that $V_{sw}/2pb_p$ will be almost an order of magnitude less than 1, and therefore the binomial expansion simplification shown in (102) applies. The two terms in (110) that can be simplified are shown in (111) and (112).

$$\left(1-\frac{V_{sw}}{2pb_p}\right)^{1-mj_p}\approx 1-\left(1-mj_p\right)\frac{V_{sw}}{2pb_p} \tag{111}$$

$$\left(1-\frac{V_{sw}}{2pb_p}\right)^{-mj_p}\approx 1-\left(-mj_p\right)\frac{V_{sw}}{2pb_p} \tag{112}$$

Using these simplification in (110) results in (113).

$$\frac{2Cj_p Ad_p pb_p}{1-mj_p}\left[1-\left(2-mj_p\right)\left(1-\left(1-mj_p\right)\frac{V_{sw}}{2pb_p}\right)+\left(1-mj_p\right)\left(1-\left(-mj_p\right)\frac{V_{sw}}{2pb_p}\right)\right] \tag{113}$$

Algebraic manipulation if (113) results in (114), a simplified expression for the weighting of the junction capacitance of the PMOS load transistor.

$$2Cj_p Ad_p V_{sw} \tag{114}$$

To perform the simplification of the sidewall capacitance term for the PMOS load transistor, it can be noted that the sidewall capacitance term is of the same form as the junction capacitance term. The only difference is that Cj must be replaced by Cjsw, mj by mjsw, pb by pbsw and Ad by Pd. The sidewall capacitance term as it is derived in the denominator is given in (115), and with simplification in (116).

$$\frac{2Cjsw_p Pd_p}{1-mjsw_p}\left[pbsw_p - \frac{pbsw_p - (2-mjsw_p)V_{sw}}{\left(\frac{pbsw_p - \frac{V_{sw}}{2}}{pbsw_p}\right)^{mj_p}}\right] \tag{115}$$

$$2Cjsw_p Pd_p V_{sw} \tag{116}$$

The error in the PMOS sidewall and junction capacitance terms due to this simplification is shown in Figure 53 as a function of V_{sw} for typical values in a 1.8V, 0.18µm CMOS process. The error in the junction and sidewall capacitance term is less than 10% for typical V_{sw} values. Also, since these capacitances are only a fraction of the total capacitances, the error in the frequency will generally be less than 1%.

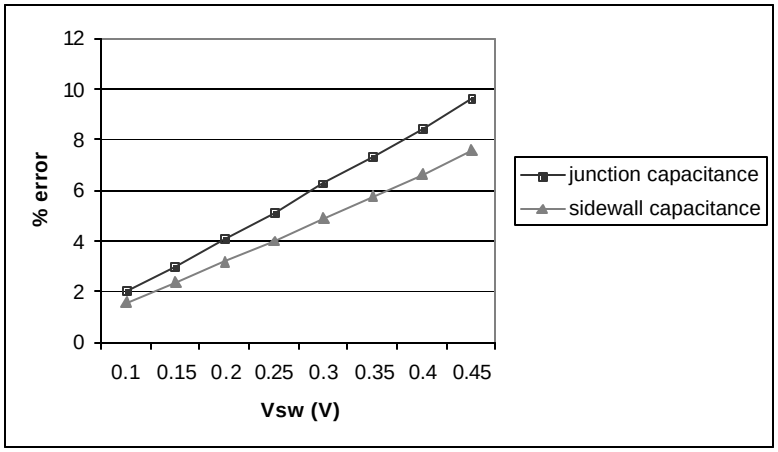


Figure 53: % error in capacitance values due to simplification of junction and sidewall capacitance terms for the PMOS transistors

Appendix C

Simplification of the gate resistance term

This appendix explains the simplification performed for the gate resistance components of the oscillation frequency equation derived in section 4.4.3. With simplification, the oscillation frequency, including the gate resistance, is shown in (117).

$$f = \frac{I_{SS}}{2NV_{sw}\left(C_{in}+C_{par}\right)}\cdot\left[1-\frac{I_{SS}R_g}{V_{sw}}\left(\left(\frac{C_{par}}{C_{in}+C_{par}}\right)\left(2-N\left(\frac{1}{2}-\frac{1}{\pi}\right)\right)+\frac{2\sqrt{2}NI_{frac}}{\pi}\right)\right] \qquad (117)$$

As discussed in section 4.4.3, the effect of the gate resistance is determined from both the effect of the time shift in the period of the voltage waveform on C_{in} and on the differential input voltage. The two effects are shown in Figure 54. The simplification regarding the time shift due to R_g will be discussed first.

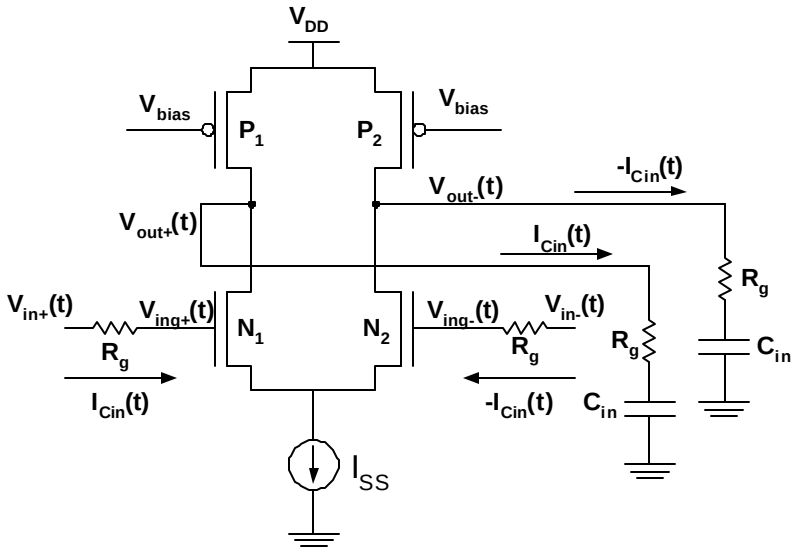


Figure 54: Effects of gate resistance

With no gate resistance, the voltage on the capacitor C_{in} is equal to $V_{out+}(t)$. However, with the gate resistance, the voltage on C_{in} no longer equals $V_{out+}(t)$, and time that the voltage crosses the mid-swing point will shift slightly. This is important because it affects the limits of integration when integrating the current. Therefore, the time that the voltage at C_{in} crosses the mid-swing point, V_{dd}-V_{sw}/2, must be determined. This can be done by solving (118) for t_0.

$$V_{out+}(t_0) - I_{Cin}(t_0)R_g = V_{DD} - \frac{V_{sw}}{2} \tag{118}$$

where $V_{out+}(t)$ is given in (24) and $I_{Cin}(t)$ is found through KCL as before. To simplify the expressions, all the parasitic capacitances will be lumped into a term called C_{par} as defined in (69). Making the substitutions into (118) gives (119).

$$\sin\left(\pi\frac{2ft_0N - N - 1}{N}\right) + 2\pi fR_gC_{par}\cos\left(\pi\frac{2ft_0N - N - 1}{N}\right) = 0 \tag{119}$$

Solving (119) for t_0 gives (120).

$$t_0 = \frac{\pi N + \pi - a\tan(2\pi f \cdot R_gC_{par})N}{2\pi fN} \tag{120}$$

The argument of atan, $2\pi fR_gC_{par}$, is much less than 1. If θ is small, then atan(θ) ~ θ. Therefore, (120) can be simplified to

$$t_0 = \frac{\pi N + \pi - 2\pi f \cdot R_gC_{par}N}{2\pi fN} \tag{121}$$

Eq. (121) can be further reduced to (122), which gives the time that the voltage on C_{in} crosses the mid-swing point. This is the time to be used as the lower limit on the integration of the current.

$$t_0 = \frac{N+1}{2Nf} - R_gC_{par} \tag{122}$$

Note that if R_g is set to 0, (122) reduces to the previous expression for t_0 given in (31). The subsequent times to be used in the integration are still separated by a quarter period.

Using the new integration limits, step 8 of the proposed method can be used to determine f_1. After substitution and integration, (123) is obtained.

$$\frac{1}{2}C_{in} = \frac{\pi + 2 + 4\pi f_1 R_p C_{par} + (4 - 8\pi f_1 R_p C_{par})\sin(\theta)\cos(\theta) - (4 + 8\pi f_1 R_p C_{par})\cos^2(\theta)}{8\pi f_1 R_p} \quad (123)$$

where $\theta=\pi f_1 R_g C_{par}$ and R_p is the equivalent resistance of the PMOS load. Since $\theta<<1$, $\sin(\theta)$ is << 1, and these terms become negligible. Also, since $\theta<<1$, $\cos(\theta) \sim 1$. Making these substitutions results in (124)

$$\frac{1}{2}C_{in} = \frac{\pi + 2 + 4\pi f_1 R_p C_{par} - (4 + 8\pi f_1 R_p C_{par})}{8\pi f_1 R_p} \quad (124)$$

Solving (124) for f_1 gives

$$f_1 = \frac{\pi - 2}{4\pi R_p (C_{in} + C_{par})} \quad (125)$$

The same steps can be repeated to determine f_2. The result is given in (126).

$$f_2 = \frac{4\pi I_{SS} R_p + N V_{sw}(2 - \pi)}{4\pi N(V_{sw}(C_{in} + C_{par}) + 2 I_{SS} R_g C_{par})} \quad (126)$$

Averaging f_1 and f_2 gives the overall frequency equation

$$f = \frac{I_{SS}}{2N V_{sw}(C_{in} + C_{par})}\left[\frac{1 + \frac{I_{SS} N R_g}{V_{sw}} \cdot \frac{C_{par}}{C_{in} + C_{par}}\left(\frac{1}{2} - \frac{1}{\pi}\right)}{1 + \frac{2 I_{SS} R_g}{V_{sw}} \cdot \frac{C_{par}}{C_{in} + C_{par}}}\right] \quad (127)$$

Eq. (127) is of the form (1+a)/(1+b) where a,b << 1. Therefore, (1+a)/(1+b) ~ 1-(b-a). Using this simplification, (127) reduces to

$$f = \frac{I_{SS}}{2N V_{sw}(C_{in} + C_{par})} \cdot \left(1 - \frac{I_{SS} R_g C_{par}}{V_{sw}(C_{in} + C_{par})}\left(2 - N\left(\frac{1}{2} - \frac{1}{\pi}\right)\right)\right) \quad (128)$$

This is the equation used in section 4.4.3.

Next, the simplification necessary to derive the effect of the gate resistance on the differential input voltage will be explained. As shown in Figure 54, the gate resistance affects the value of the differential input voltage. It was previously assumed that the differential input voltage was $V_{in+}(t)$-$V_{in-}(t)$. This is no longer the case. Now, the inputs to the gates of N_1 and N_2, $V_{ing+}(t)$ and $V_{ing-}(t)$, are given by (129) and (130), and the differential input voltage is now $V_{ing+}(t)$-$V_{ing-}(t)$.

$$V_{ing+}(t) = V_{in+}(t) - I_{cin}(t)R_g \tag{129}$$

$$V_{ing-}(t) = V_{in-}(t) + I_{cin}(t)R_g \tag{130}$$

A difficulty arises in that $I_{Cin}(t)$ is a function of $V_{id+}(t)$, resulting in an equation that is difficult to solve. To solve this problem, first note that the phase of the current into a capacitor has a $\pi/2$ phase shift from the voltage. Since the voltage is a sine wave, the current will be a cosine. Also, the amplitude of the current can be represented as a fraction of the total tail current, I_{SS}. This fraction is fairly constant, although it is a weak function of I_{SS}, V_{sw} and N. This fraction will be called I_{frac}, which simulations show to be about 0.2. Therefore, (129)and (130) can be rewritten as (131) and (132).

$$V_{ing+}(t) = V_{in+}(t) - I_{frac}I_{SS}\cos(2\pi ft)R_g \tag{131}$$

$$V_{ing-}(t) = V_{in-}(t) + I_{frac}I_{SS}\cos(2\pi ft)R_g \tag{132}$$

Therefore, the current through R_g is no longer a function of $V_{in+}(t)$. The current through N_1, $I_{ds}(t)$ is a function of the differential voltage across N_1 and N_2. This voltage is now found as $V_{ing+}(t)$-$V_{ing-}(t)$, which is shown in (133).

$$V_{idg}(t) = V_{id}(t) - 2I_{frac}I_{SS}\cos(2\pi ft)R_g \tag{133}$$

The expression for $I_{ds}(t)$ can now be rewritten as

$$I_{ds}(t) = \frac{I_{SS}}{2} + \frac{\mu_n C_{ox}\frac{W}{L}V_{idg}(t)}{4}\sqrt{\frac{4\cdot I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - V_{idg}^2(t)} \tag{134}$$

Now that the differential input voltage includes R_g, the oscillation frequency can be derived again, following the steps laid out in section 3.3. As with the example in section 3.3.1, the differential voltage for the first section is such that there is no current flowing through N1. Therefore, f_1 will be the same as in the example. It is repeated here for convenience.

$$f_1 = \frac{1}{4} \cdot \frac{\pi - 2}{\pi \cdot R\left(C_{in} + C_{par}\right)} \tag{135}$$

For the second section, there is current through N_1, and therefore f_2 must be recalculated with the gate resistance. After substitution into (30), as part of step 8, (136) is obtained

$$-\frac{V_{sw}}{2} C_{in} = \frac{I_{SS}\left(1 - \frac{2}{\pi} - \frac{4}{N} + \frac{4}{\pi} a\sin\left(\frac{1}{V_{sw}}\left(\frac{2I_{SS}}{\mu C_{ox}\frac{W_n}{L}}\right)\right)\right) + 2f\left(2V_{sw}C_{par} + \int_{t_{1a}}^{t_{1b}} X \cdot dt\right)}{8f} \tag{136}$$

where

$$X = -2I_{SS} - YV_{sw}\sin\left(2\pi ft\right) + 2YR_g I_{frac} I_{SS}\cos\left(2\pi ft\right) \tag{137}$$

and where

$$Y = \mu_n C_{ox}\frac{W_n}{L}\left(\frac{4I_{ss}}{\mu_n C_{ox}\frac{W_n}{L}} - \sin^2\left(2\pi ft\right) + 4V_{sw}R_g I_{frac} I_{SS}\sin\left(2\pi ft\right)\cos\left(2\pi ft\right) + \left(2R_g I_{frac} I_{SS}\cos\left(2\pi ft\right)\right)^2\right)^{\frac{1}{2}} \tag{138}$$

Eq. (136) is difficult to solve for f. However, this can be simplified if the remaining integral term, X, can be simplified. X in turn can be simplified if Y can be simplified. Note that in Y, the last term is much less than the terms it is added to, and can be ignored. With this simplification, Y is now given as

$$Y = \mu_n C_{ox}\frac{W_n}{L}\left(\frac{4I_{ss}}{\mu_n C_{ox}\frac{W_n}{L}} - \sin^2\left(2\pi ft\right) + 4V_{sw}R_g I_{frac} I_{SS}\sin\left(2\pi ft\right)\cos\left(2\pi ft\right)\right)^{\frac{1}{2}} \tag{139}$$

Substituting (139) into (137), and (137) into (136), (136) simplifies to

$$-\frac{V_{sw}}{2}C_{in} = \frac{I_{SS}\left(1-\frac{2}{\pi}-\frac{4}{N}+\frac{4YR_gI_{frac}}{\pi V_{sw}}\sqrt{\frac{2I_{SS}}{\mu C_{ox}\frac{W_n}{L}}}\right)+4fV_{sw}C_{par}}{8f} \tag{140}$$

This can be further simplified by noting another difference in the magnitudes of the terms making up Y in (139). The last two terms in the parenthesis are less than the first, meaning that Y can be simplified to

$$Y = \left(4I_{SS}\mu_n C_{ox}\frac{W_n}{L}\right)^{\frac{1}{2}} \tag{141}$$

Substituting (141) into (140) gives

$$-\frac{V_{sw}}{2}C_{in} = \frac{I_{SS}\left(1-\frac{2}{\pi}-\frac{4}{N}+\frac{8\sqrt{2}R_gI_{frac}I_{SS}}{\pi V_{sw}}\right)+4fV_{sw}C_{par}}{8f} \tag{142}$$

Solving (142) for f gives f_2.

$$f_2 = \frac{1}{4}\cdot\frac{NV_{sw}(2-\pi)+4\pi V_{sw}-8\sqrt{2}NR_gI_{frac}I_{SS}}{\pi NV_{sw}R(C_{in}+C_{par})} \tag{143}$$

Averaging f_1 and f_2 gives the overall frequency taking into account the effect if R_g on V_{id}, as shown in (144). This is equivalent to (76) derived in section 4.4.3.

$$f = \frac{I_{SS}}{2NV_{sw}(C_{in}+C_{par})}\cdot\left(1-\frac{2\sqrt{2}NI_{frac}I_{SS}R_g}{\pi V_{sw}}\right) \tag{144}$$

To obtain the final frequency equation taking into account the gate resistance, the 1-x factors from (128) and (144) will be multiplied to result in a single term accounting for R_g. This term is then combined

with the oscillation frequency equation without the gate resistance. This gives (145), the final oscillation frequency equation accounting for time-varying parasitic capacitances and a gate resistance.

$$f = \frac{I_{SS}}{2NV_{sw}\left(C_{in} + C_{par}\right)} \cdot \left[1 - \frac{I_{SS}R_g}{V_{sw}}\left(\left(\frac{C_{par}}{C_{in} + C_{par}}\right)\left(2 - N\left(\frac{1}{2} - \frac{1}{\pi}\right)\right) + \frac{2\sqrt{2}NI_{frac}}{\pi}\right)\right] \qquad (145)$$

where C_{par} corresponds to all parasitic capacitances as defined in (69).

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