A DFT Technique for High Performance Circuit Testing

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Abstract

Testing of high performance integrated circuits is becoming increasingly a challenging task owing to high clock frequencies. Often testers are not able to test such devices due to their limited high frequency capabilities. In this article we outline a DFT strategy such that high performance devices can be tested on relatively low performance testers. In addition, various implementations aspects of this technique are also addressed.

1. Introduction

The clock speed of advance CMOS VLSI devices have surpassed 1 GHz barrier. The Semiconductor Industry Association (SIA) roadmap for semiconductors 1997, expects even more aggressive increase in clock frequencies for future CMOS VLSI generations. High speed processors are enabling applications in many diverse fields. However, at the same time, testing and reliability of such devices is identified as one of the most critical challenges for VLSI testing [1].

Historically, testers had a timing accuracy of 5X over the state of the art ICs. As a result, performance testing was a non-issue. Since then, IC clock frequencies have improved on an average 30% per year while tester accuracy has improved only on an average 12% per year. If this trend continues, in coming few years, tester timing accuracies will approach the cycle time of the state of the art devices. Long before such a situation arises, yield loss due to insufficient accuracy of the tester will become unacceptably high [1,2]. Fig.1 which plots the SIA roadmap 97 data, further illustrates the point. According to these numbers inadequate tester resolution is causing undesirable yield loss in the state of the art, high performance VLSI.

Cost of a state of the art tester has risen significantly and it costs approximately $4-5 Million. Its cost is expected to increase further in years to come. In less than a decade, a state of the art tester may cost more than $20 Million. SIA roadmap predicts that cost of testing a die will surpass its manufacturing cost in the near future. The clock frequency of the device under test (DUT) plays a strong role in determining the overall test cost. Test cost can be reduced if DUT can be tested at substantially lower clock frequency than its nominal frequency while ensuring its high frequency behavior.

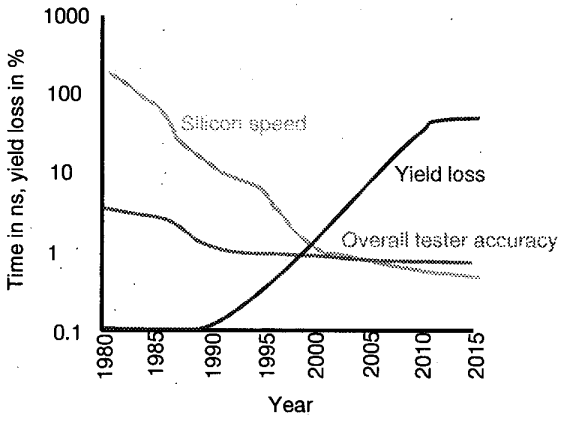

Fig.1: Trends in silicon clock period and overall tester accuracy [1,2].

2. Review and Motivation

Manufacturing defects are often segregated into catastrophic and non-catastrophic categories. Catastrophic defects influence IC topology significantly such that their influence is noticeable even at lower clock frequency. The impact of non-catastrophic or parametric defects is subtle and often means such as I_{DDQ}, burn-in, and performance testing are employed to uncover them. There is a general consensus among experts that large number of such defects lead to reliability failures in the field. Although I_{DDQ} testing and burn-in are very effective, their limitations are becoming prominent as we march into deep sub-micron

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regime [3,4,5].

A number of recent studies show concerns about new failure mechanisms in scaled geometries that may be harder to detect with conventional means. Recently Nigh et. al. [6] reported significantly large number of timing only failures. These failures did not influence the circuit's steady state logic functionality. Hence, these defects were not detected by slow speed SA based or functional tests. Similarly, for Intel's manufacturing processes, Needham et. al. [7] reported an increasing shift towards soft defects as technology moved from 0.35 to 0.25 micron. These defects do not always cause failures at all temperature and voltage conditions. According to authors, there is a correlation between soft defects and long term device reliability.

Some of these defects can be detected by I_{DDQ} testing provided background leakages are kept under control and ICs are designed to be I_{DDQ} testable. In high performance ICs often dynamic circuit techniques, low transistors threshold (V_T) technologies are utilized. These techniques lead to either insufficient I_{DDQ} coverage or make devices I_{DDQ} untestable. For such ICs performance testing, burn-in are routinely utilized to ensure long term device reliability. As cost of high performance testing is becoming expensive, researchers exploited innovative techniques to evaluate high frequency DUT response without a high frequency tester. Agrawal and Chakraborty [8] segregated them into indirect and direct test methods.

2.1. Indirect test methods

The indirect methods include correlation techniques to alleviate the need for high performance testing. Ring oscillators are often used for this purpose. A ring oscillator is put on a DUT and its free running frequency provides correlation to DUT high performance behavior. Bruls [9] used 11 stage on-chip ring oscillator as a performance indicator. The output of the ring oscillator was fed to 10 stage counter to reduce the oscillation frequency from 200 MHz to 200 kHz. Free running frequency of the counter provided correlation for DUT performance. Keshvarzi et. al. [5] reported a strong correlation between the I_{DDQ} and the maximum operating frequency for a 32 bit microprocessor. They argued that these two parameters were fundamentally related as both are functions of the channel length. This information can be used as a mechanism for high performance binning.

CMOS digital circuits exhibit increasingly large switching delay as supply voltage is reduced. In the limiting case, circuits work at VDD greater than the V_T. If the VDD is further reduced below V_T circuits do not switch. Therefore, reduced supply voltage testing may be carried out to lower the DUT operational frequency. Wagner and McCluskey [10] and Ho and McCluskey [11] found an empirical relationship between propagation delay at reduced supply voltage and nominal supply voltage.

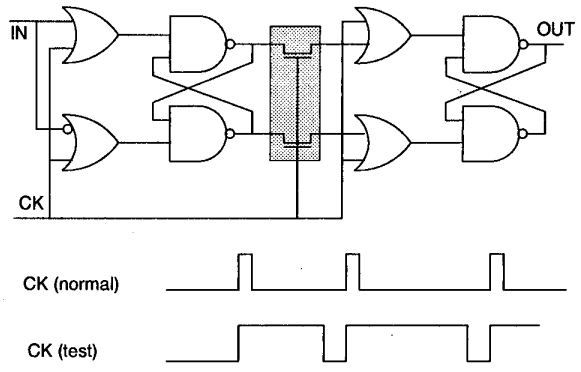


Fig. 2: Pulse triggered flip-flop and its clock waveform in normal and test modes [8].

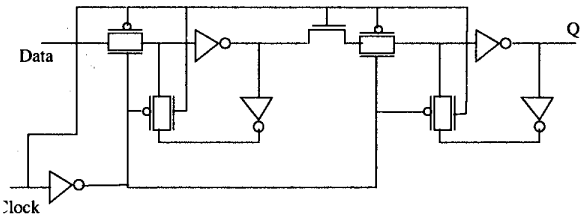


Fig. 3: CMOS implementation of pulse triggered flip-flop.

$$T' = xT_0\left(1-k\frac{\Delta VDD}{V_0}\right)+(1-x)T_0 \qquad \text{(EQ 1)}$$

Where T' is the propagation delay at reduced VDD. T_0, and V_0 are nominal delay and nominal VDD voltage, respectively. k is the process dependent constant and x is the fraction of the total path delay due to gate delay in the signal path.

Although correlation methods are widely used in VLSI testing, yet these methods are probabilistic in nature. In most applications, pass/fail decision-making based on such methods is hazardous [14]. For example, correlation between a small size ring oscillator and relatively big IC may not be appropriate. Similarly, due to ever increasing interconnect delays, correlation between I_{DDQ} and maximum DUT frequency may become weaker. Moreover, as technology is scaled, the VDD voltage is also scaled to reduce power consumption and to enhance reliability. As a consequence, there may not be sufficient room to reduce supply voltage for low voltage testing. Agrawal and Chakraborty [8] pointed out that the routing delays remain largely unchanged as VDD voltage is lowered. Hence, critical paths at a low voltage may not be the same as at nominal voltage. Furthermore, at low voltage switching noise in

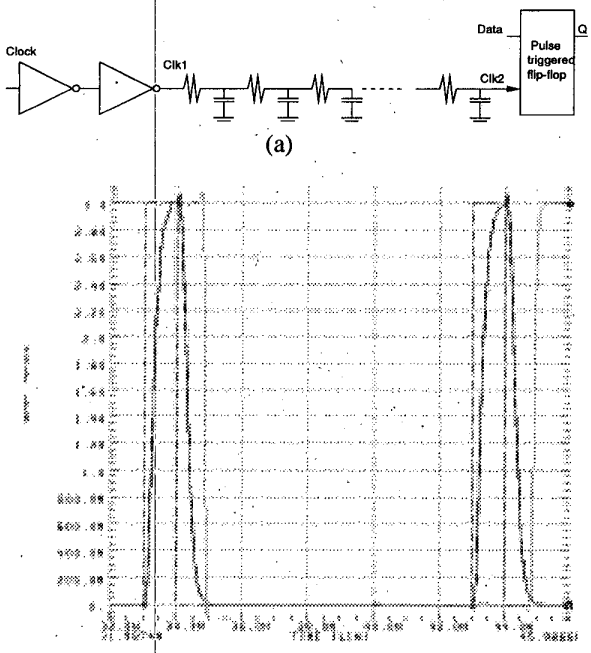


Fig. 4: A minimum of 1 ns pulse width is required for a pulse trigger flip-flop operation with 1 mm long clock line in 0.35 micron technology: model (a); and simulation results.

power supply lines will affect the reduced voltage operation and may also influence delays.

2.2. Direct test methods

Direct methods are generally preferred over indirect test methods. Direct methods include multiplexing of tester clock pins to extend the clock frequency range of a tester. Two or more high frequency clock signals are ORed to generate a higher frequency clock. This is a standard feature offered on most of the digital testers. Practical issues such as limited tester pins prevent from more than doubling of the original clock frequency.

Agrawal and Chakraborty proposed creation of a low frequency test mode in circuits. A quantifiable, externally controlled delay is added such that a high performance testing can be carried out with relatively slow speed testers [8]. The basic idea of their scheme is illustrated in Fig. 2 and Fig. 3. They proposed a pulse triggered flip-flop with two operational modes. In simple terms, a dynamic latch (highlighted pass transistor in Fig. 2) was introduced inside a traditional master-slave flip-flop. Three latch arrangement allowed modulation of flip-flop delay with the clock pulse width. In a digital circuit, all signal paths must satisfy timing relationship shown in EQ. 2.

$$T \geq PD_{FF} + PD_{CL} + T_{Setup} \qquad \text{(EQ 2)}$$

Where T is the clock period, PD_{FF} is the propagation delay through the flip-flop, PD_{CL} is the delay through the combinational logic, and T_{Setup} is the setup time for flip-flops. Fig. 2 also illustrates the clock timing in normal and test modes. In normal mode a small clock pulse width offers small propagation delay through the flip-flop. In the test mode, increased pulse width of the clock increases the propagation delay of the flip-flop. Considering that PD_{CL} and T_{Setup} remain unchanged, the clock period, T, must become larger for EQ. 2 to be valid. In other words, slower clock frequency is able to test critical or other paths with same timing specifications.

Although, the concept of adding delay in the test mode is elegant, it has some important consequences for normal functioning of IC. Some of them are listed below:

1. Realization and propagation of a small, precise pulse width over a complex VLSI for normal mode operation is a difficult task. A significant amount of propagation delay gets added in the normal functioning of the flip-flop since a finite, minimum pulse width is needed for robust flip-flop operation. In ideal conditions, the smallest pulse width is found to be 500 ps. However, a much larger pulse width is needed if realistic interconnect impedances are considered. Fig. 4 illustrates a schematic (a) and simulation (b) of a pulse triggered flip-flop with clock buffers and 1 mm long interconnect impedance in 0.35 micron technology. The graph shows, input clock, clock at the input of the flip-flop (Clk2) and output of the flip-flop. The simulation results show that a minimum of 1 ns pulse width is required for robust flip-flop operation. As a consequence, normal mode flip-flop propagation delay is more than 1.5 ns. A relatively large normal mode propagation delay of pulse triggered flip-flop proves to be counter productive for high performance applications.
2. The pass transistor inside the pulse triggered flip-flop is used as a dynamic latch. Dynamic latch makes flip-flop operation sensitive. As pulse width increases, output of the dynamic latch remains in high impedance for increasingly larger amount of time. Alternatively, one can put a static latch, however, its cost in terms of hardware and delay is higher.
3. Generation of small pulse width on a tester which does not have high frequency capability is also limited.

In this article, we revisit the issue of high speed testing incorporating controllable delays in flip-flops. We consider several flip-flop configurations and evaluate their normal mode and test mode behaviors. A 6x6 multiplier is

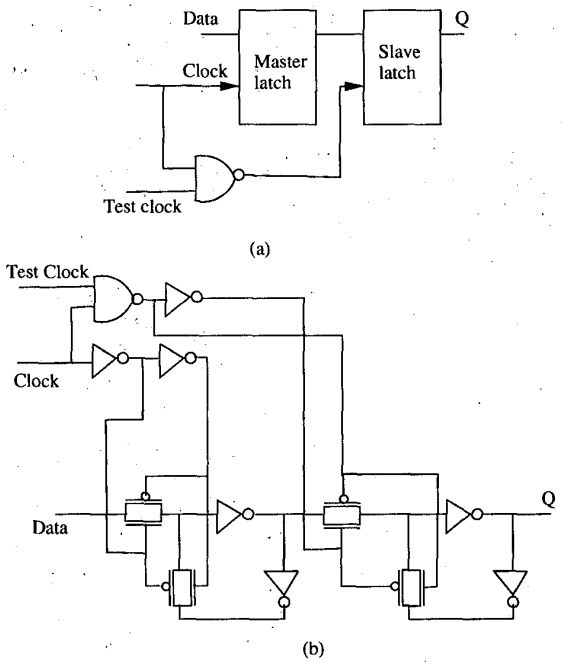


Fig. 5: First controlled delay flip-flop (CDFF1) to facilitate high speed testing: concept (a), and its gate level implementation (b).

designed to evaluate effectiveness of the proposed DFT technique.

3. Flip-flop as a Controlled Delay Element

One of the most significant implementation issue in pulse triggered flip-flop is realization and propagation of precise pulse width at the chip level. A small pulse width needed for high speed normal mode operation may appear significantly distorted due to interconnect impedance. Flip-flop delay can be controlled by an additional test mode clock. We called these flip-flops as controlled delay flip-flops (CDFFs). A CDFF differs significantly in concept and in implementation details from the pulse triggered flip-flop. These differences are crucial and will become apparent to the reader subsequently in the article.

Fig. 5 illustrates a block diagram and a gate level implementation of the CDFF. The CDFF has an additional input, the Test clock. The slave latch receives clock that is logical NAND of the Clock with the Test clock. Such an arrangement allows master to slave data transfer on the rising edge of the Test clock. In the test mode, propagation delay through the flip-flop is controlled with the Test clock. Since propagation delay can be controlled, this flip-

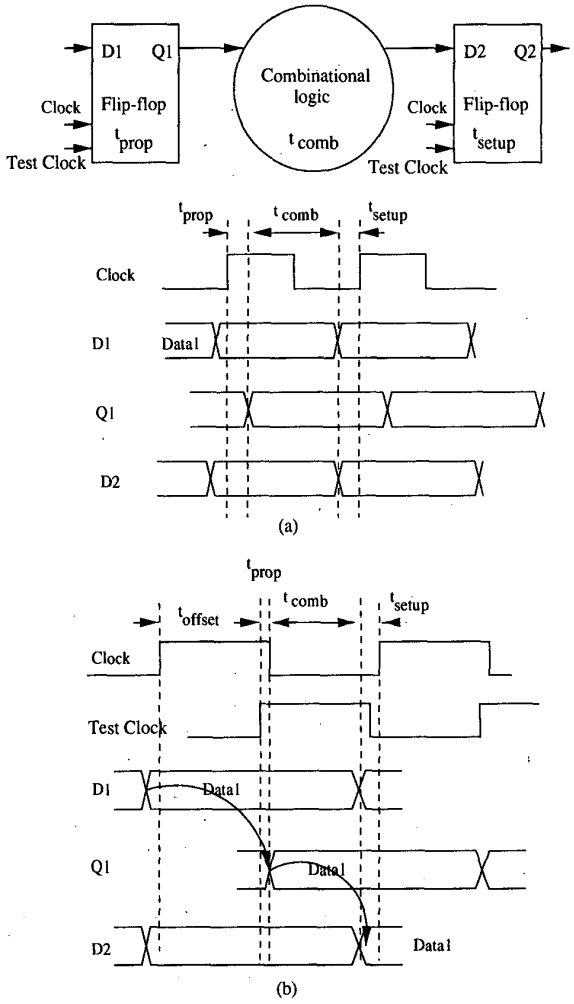


Fig. 6: Timing diagram of normal mode operation (a); and the test mode operation (b).

flop is called CDFF. The significance of the Test clock is further illustrated with the help of Fig. 6. This figure depicts the normal and the test mode timing diagrams of an arbitrary digital circuit with CDFFs.

In the normal mode, the Test clock has no function and is held high ensuring normal flip-flop operation (Fig. 6(a)). However, during the testing of an IC, it operates as a clock with tester programmed time offset with the normal IC clock. The Test clock goes to all, or a pre-determined subset of flip-flops in an IC. This clock when active, controls the data transfer from master to slave latch in flip-flops. In other words, depending on the timing relationship between the Clock and the Test clock, a delay is introduced between master and slave latches of the flip-flop. The net effect is that, flip-flop output, Q, appears after an additional

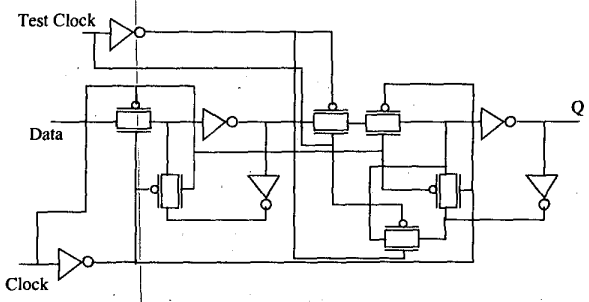


Fig. 7: Second CDFF (CDFF2) implementation.

delay which is the time offset between the Clock and the Test clock. The Fig. 6(b) illustrates the scenario when the Test clock is active. In this condition, the EQ.2 is modified as follows:

$$T_{TM} \geq PD_{FF} + PD_{CL} + T_{Setup} + T_{Offset} \quad \text{(EQ 3)}$$

T_{Offset} is time offset between the Clock and the Test clock. The test mode clock period, T_{TM}, should be large enough to accommodate all delay terms listed in EQ. 3. It is obvious from this equation that as the offset is increased the period of the clock is also increased or the clock frequency is reduced. In other words, clock frequency can be reduced while the combinational circuit delays are tested with same delay margins.

The implementation of CDFF requires additional transistors and an additional test mode clock input. Depending on the number of CDFFs needed, a set of test clock buffers and interconnects may be required. The cost of implementation is high. Extra cost is compensated by cheaper, slower testers.

3.1. Second CDFF Implementation

Fig. 7 depicts second CDFF implementation. In this CDFF, two transmission gate pairs (TGs) are added. The first TG is added between master slave latches while the second one is added in the feedback path of the slave. Both TGs are controlled by the test clock. Addition of the first TG is obvious as it controls the master to slave data transfer. The need for the second TG can be explained as follows: In a situation when the Clock is high and the Test clock is low, the output of CDFF is not driven. High clock forces TG of the slave feedback path to be in high impedance state. At the same time, low on the Test clock forces high impedance on TG it controls between master and slave latch. Adding another TG in the feedback path which is controlled by the $\overline{\text{Test clock}}$ makes sure that Q is always in a driven state.

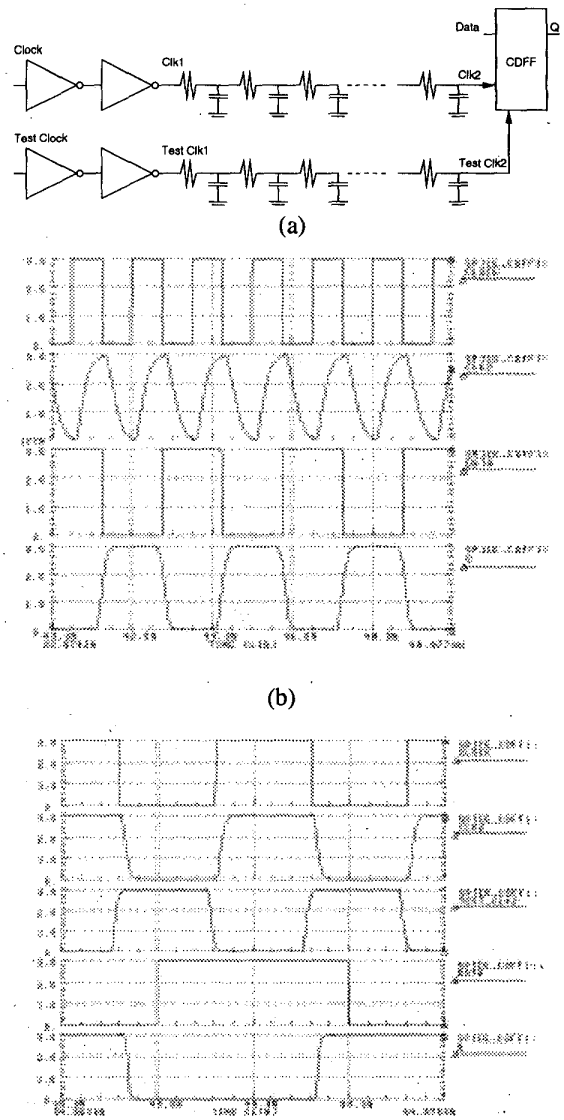


Fig. 8: Normal and test mode performance of CDFF simulation model (a); normal mode 750 MHz operation (b); and test mode 100 MHz operation in 0.35 micron CMOS technology (c).

3.2. CDFF Performance Evaluation

The spice simulations shown in Fig. 4 are repeated with CDFFs. Fig. 8 illustrates the simple simulation model of CDFF1 with interconnects and clock drivers, and its normal and test mode performance in 0.35 micron technology. Fig. 8(b) illustrates the normal mode CDFF operation. The simulations were performed at 750 MHz and the normal mode CDFF propagation delay was found to be approxi-

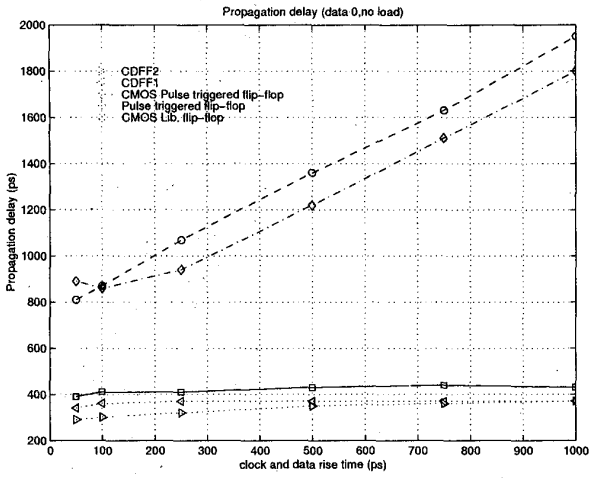


Fig. 9: Comparison of flip-flop propagation delays as a function of rise and fall times.

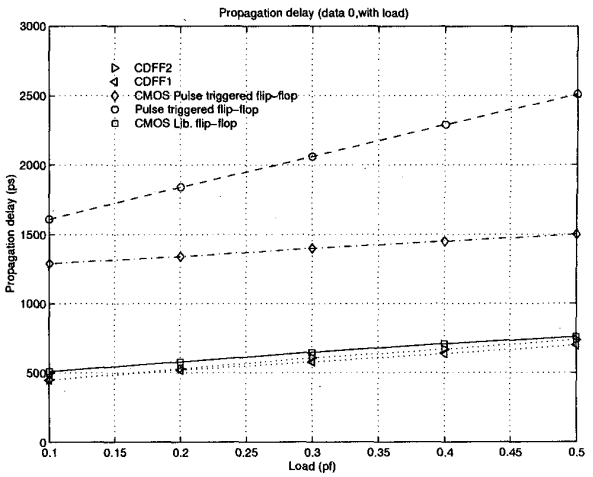


Fig. 10: Comparison of flip-flop propagation delays as a function of output load.

mately 0.5 ns. Fig. 8(c) depicts the test mode operation at clock frequency of 100 MHz.

Timing performance of a flip-flop is characterized by data setup time (t_{su}), hold time (t_h) and the propagation delay. CDFFs, pulse triggered flip-flop, and conventional flip-flop were characterized for setup and hold times and propagation delays. For this comparative study, we ensured that all flip-flops have same transistor dimensions. Transistors of similar dimensions were added in the CDFFs and pulse triggered flip-flops. Transistor sizes are selected to be representative of the technology and the design style. For this analysis, we selected a standard 0.35 micron single poly, double metal technology. However, no extra effort is made to particularly optimize flip-flops for power, performance, area, etc. All flip-flop configurations are circuit simulated with Hspice in Cadence design environment. Here, we must stress that for this comparative study, the selection of absolute transistor parameters or flip-flop optimization for performance is of minor consequences. It is the relative performance of the flip-flop configurations that is of crucial importance to quantify the impact of proposed flip-flop configurations on its timing performance. We simulated 5 flip-flops which include pulse triggered flip-flop (Fig. 2), CMOS pulse triggered flip-flop (Fig. 3), CDFF1 (Fig. 5), CDFF2 (Fig. 7) and a conventional flip-flop from a 0.35 micron commercial CMOS library.

Fig. 9 illustrates comparison of no load propagation delays as a function of clock and data rise time. The propagation delays of conventional flip-flops, CDFF1 and CDFF2 were found to be relatively small and comparable to each other. Furthermore, their respective propagation delays are not a strong function of data and clock rise times. On the other hand, pulse triggered flip-flops exhibit relatively large propagation delays which increase substantially as rise and fall times of the clock and data deteriorate. High speed on-chip clocks do not have very sharp rise and fall times owing to high fanout and large, distributed impedance of clock interconnect. Furthermore, the interconnect impedance is expected to increase significantly with scaling of CMOS technology [6]. As clock rise and fall times are increased, the pulse width of the clock is also increased. The increased pulse width results in larger propagation delay for the pulse triggered flip-flop. Furthermore, contrary to a normal flip-flop or CDFF, pulse triggered flip-flops make use of both rising and falling edges of clock. Therefore, they show greater variation in their propagation delay as rise and fall time vary.

Fig. 10 illustrates comparison of flip-flop propagation delays as a function of output load. It is apparent from the graph that the propagation delays of pulse triggered flip-flops are quite large compared to the conventional flip-flop or CDFFs. For this simulation, clock and data rise/fall times were kept at 500 ps. As mentioned before, delay through pulse triggered flip-flops is a function of clock pulse width. A minimum of approximately 500 ps pulse width is required for functioning of pulse triggered flip-flops. The simulation of pulse triggered flip-flops are carried out with keeping pulse width of 500 ps in order to have lowest propagation delay.

Fig. 11 and Fig. 12 illustrate setup and hold times respectively, as a function of clock and data rise and fall times. CDFFs and pulse triggered CMOS flip-flop exhibit relatively small setup times. The library flip-flop exhibits

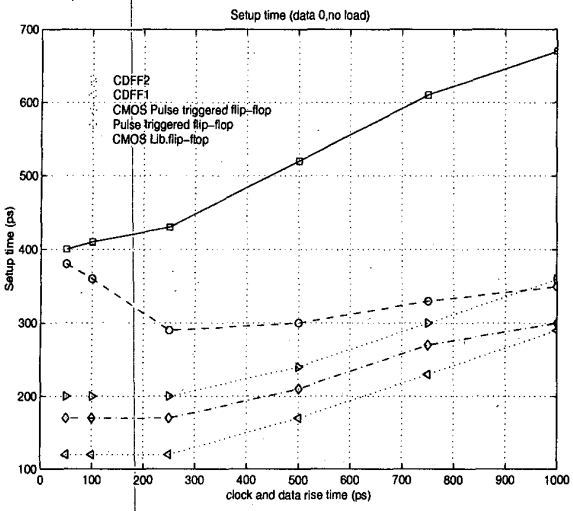


Fig. 11: Comparison of setup times.

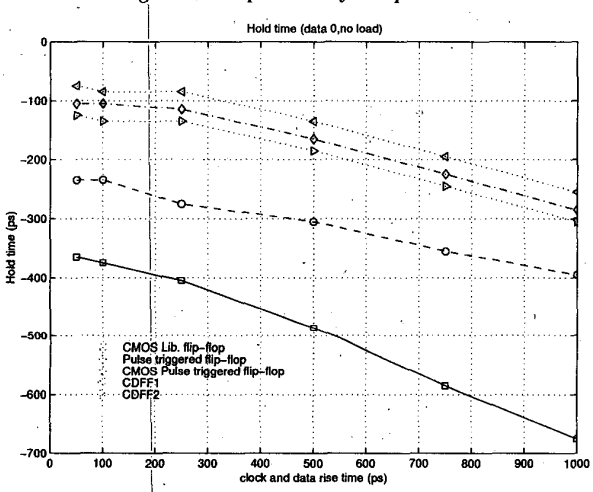


Fig. 12: Comparison of hold times.

the largest setup time. The hold times of flip-flops track their respective setup times. As a consequence, hold times of CDFFs and pulse triggered CMOS flip-flop are less negative. The illustrated graphs in figures are plotted with data 0. The simulation results with data 1 do show a similar behavior and therefore are not included here.

3.3. Implementation Issues

The implementation of CDFF requires an additional input and 6 additional transistors. It is relatively large overhead for a flip-flop implemented with 18 or 20 transistors. Cost of a transistor with scaling is reducing dramatically. Furthermore, transistors can be scaled much more aggressively than the interconnects. Therefore, it is often inter-

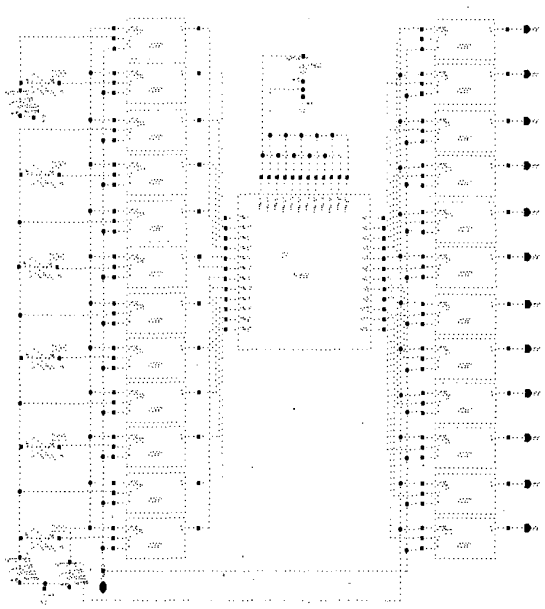


Fig. 13: Schematic of a 6x6 multiplier with CDFFs at its inputs and outputs.

connects, pads, etc. that determine the chip size. In many applications cost of few extra transistors per flip-flop may be acceptable if it reduces the cost of testing and manufacturing.

Arguably replacing normal flip-flops with CDFFs may cause some performance loss. However, our simulations do not show a significant timing difference between a normal flip-flop from cell library and CDFFs. Contrary to expectations, CDFF1 shows lower propagation delay compared to the conventional flip-flop. However, such a comparison has its shortcomings. The internal details of the conventional flip-flop are not available owing to proprietary nature of the cell library. In spite of lack of details, these simulations do show realization of CDFFs with comparable performance. CDFF implementation also requires an additional signal, Test clock which may cause additional overhead.

A two phase clocking schemes such as Level sensitive scan design (LSSD) [7,14] can also be used for high performance testing. However, LSSD is not widely used owing to its higher overhead compared to scan path technique based on edge triggered flip-flops. Furthermore, its additional power consumption associated with the two phase clocking leads to higher power consumption. Power consumption is a serious concern for high performance ICs where clock related power consumption is a significantly large contributor to the overall power consumption. The

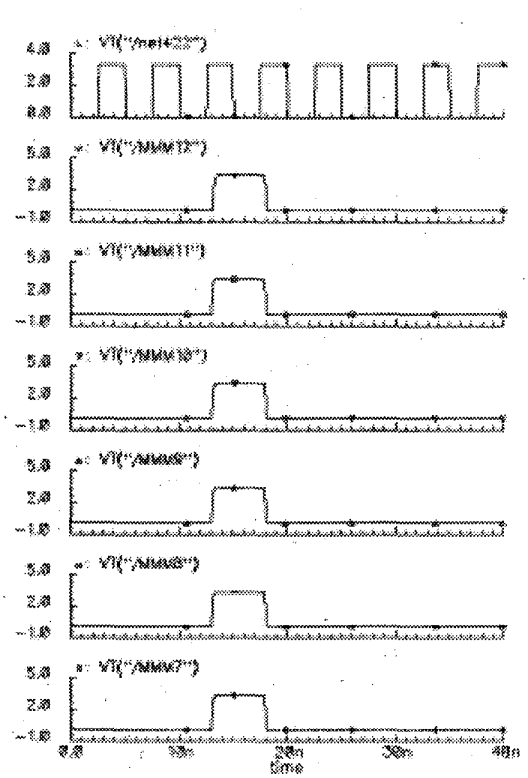


Fig. 14: Hspice simulation of the multiplier illustrating its functionality at 200 MHz.

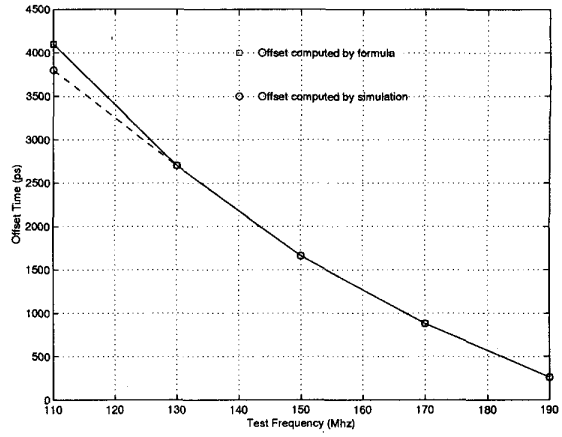
proposed technique offers, LSSD like capabilities for edge triggered flip-flop based designs. Furthermore, since the test clock is active only in the test mode, normal mode power consumption is not increased. Finally, scan is not a prerequisite for the proposed method.

4. Experimental Results

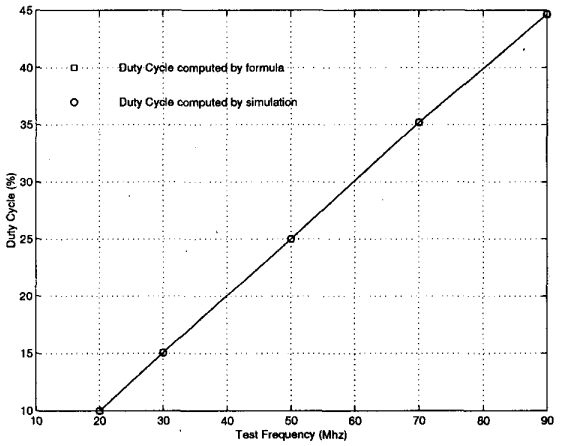
A 6x6 multiplier was chosen as a vehicle to quantify the benefits of the proposed scheme. The size of the multiplier was large enough to introduce a number of unique, timing only failures and draw conclusions. On the other hand, the multiplier was small enough to circuit simulate it in reasonable time. Fig. 13 shows its block level schematic diagram. CDFF flip-flops were placed at the inputs as well as at the outputs of the multiplier. The design was carried out in 0.35 micron CMOS technology provided by Canadian Microelectronics Corporation (CMC).

4.1. Characterization

As part of the performance characterization, schematic shown in Fig. 13 was simulated in Hspice to determine its



(a)



(b)

Fig. 15: Simulated and computed offsets as a function of clock frequency (a); Simulated and computed test clock duty cycle as a function of clock frequency (b).

maximum operational frequency. Fig. 14 illustrates the Clock and 6 MSB outputs of the schematic working at 200 MHz clock rate. In other words, the critical path between two CDFFs was found to be 5 ns. At clock frequencies beyond 200 MHz, the CDFFs at the MSB outputs were not able to latch the correct data.

EQ 3 predicts a simple relationship between clock period (frequency) of the test and the offset between the clock and Test clock. Two assumptions are made in this equation: (i) all the combinational paths between the CDFFs are given no more than the nominal delay, and (ii) the duty cycle of the clock is 50%. Fig. 15(a) compares the simulated relationship between offset and clock frequency with that of computed from EQ 3 at various Clock frequencies.

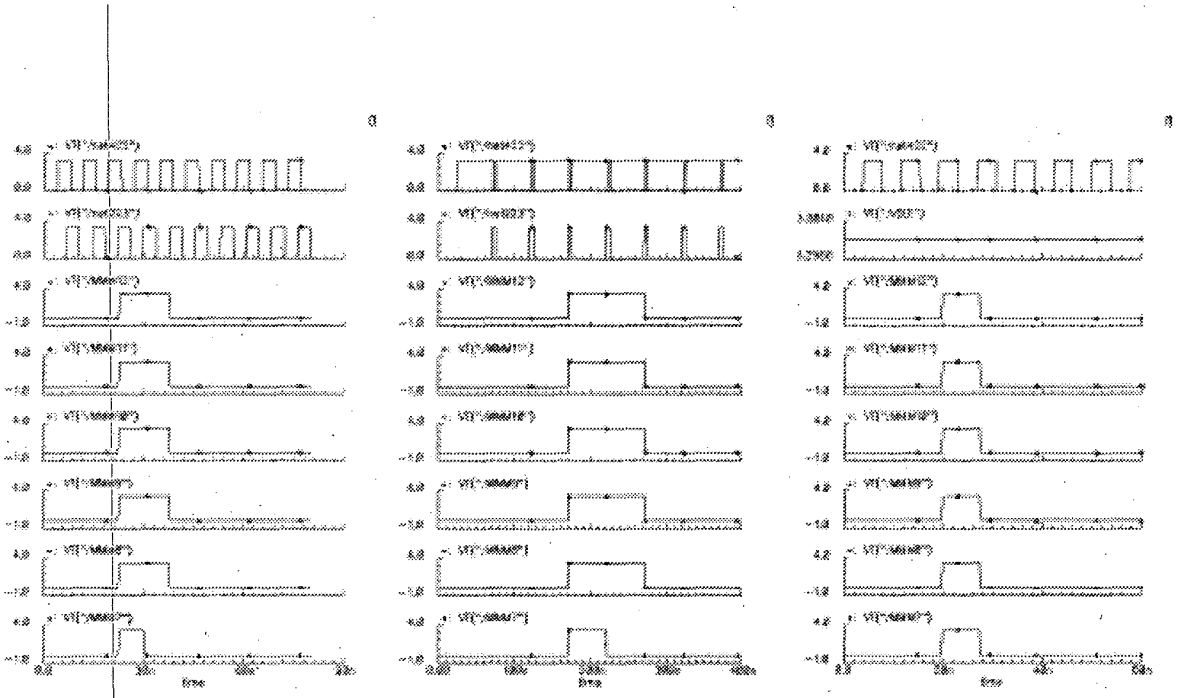


Fig: 16: A 1K ohm defect is detected at clock & test clock frequency (50% duty cycle) of 130 MHz (a); same defect is detected at clock (duty cycle >50%) and test clock (duty cycle <50%) frequency of 20 MHz (b); The defect is not detected when clock is active (130 MHz) and test clock is high (c).

The illustrated results do show a close match between computed and simulated numbers.

The Clock frequency in the test mode can not be reduced to less than half of the nominal clock so long the duty cycle of the Clock is restricted to 50%. For proper functioning of the CDFF, the positive transition of the Test clock must occur while Clock is high. In the limiting case, positive transition of the Test clock may occur at the negative transition of the Clock. In other words, if the Clock duty cycle can be increased to more than 50% and the Test clock pulse width is reduced correspondingly, the Test mode frequency can be reduced further. Most modern ATEs can generate small pulse widths of approximately 30% of the maximum rated clock frequency [15]. For example, HP 83,000 system capable of running at 660 MHz can generate a pulse width of 500 ps. As a consequence, if the constraint on narrow pulse width is removed, the circuit can be made to work at significantly lower clock frequency. The EQ 3 is modified to represent the pulse width of the Test clock by EQ 4.

$$T_{PW} \geq PD_{FF} + PD_{CL} + T_{Setup} \qquad \text{(EQ 4)}$$

The validity of EQ. 4 was verified with simulations. Fig. 15(b) compares the simulated relationship between the Clock frequency and the duty cycle of the Test clock with that of computed from EQ. 4 at various Clock frequencies. As it is apparent from the figure, simulated and computed values are closely matched.

4.2. Defect Detection

Typically, a low resistance defect gives rise to SA and/or gross timing failures. Therefore, such defects are detected with relative ease. On the other hand, high resistance defects often give rise to subtle performance variations. Low frequency tests are not able to detect such defects. Hence, for this analysis, we selected defects influencing the timing behavior of the circuit. Resistances of defects were chosen between 1K to 10K Ω in order to influence the timing. A small number of bridging defects (25) were introduced in the multiplier. Majority of defects gave rise to total failures and were detected by a low frequency (e.g., 20 MHz) test. A subset of bridging defects caused timing only failures. These defects were analyzed further and their characteristics are shown in Table 1. Fig. 16 illustrates simulations of the first analyzed bridging defect. This defect caused a node in the multiplier to be shorted to ground with 1K Ω resistor. This defect was detected at the Clock frequency of 178 MHz (and higher). We call this frequency as the transition frequency. In the test mode, the defect was excited at 130 MHz while keeping the duty cycle of the Clock and the Test clock at the 50%. Fig. 16(a) shows the Clock, Test clock and 6 MSB outputs of the multiplier. Top two waveforms show the Clock and the Test clock operating at 130 MHz. In this case, 5 MSB sig-

Table 1: High resitance defects detection with CDFFs.

Defect #	Defect (resistance)	Transition frquency MHz	Test mode detection	
			130 MHz	20 MHz
1	node - gnd (1 K)	178	Detected	Detected
2	node - Vdd (1.5 K)	164	Detected	Detected
3	node - node (1.75K)	175	Detected	Detected
4	node - node (2K)	183	Detected	Detected

nals exhibit faulty behaviors. As mentioned earlier, if the duty cycle constraint is removed, frequency of the Clock and Test clock can be reduced significantly for defect detection. Fig. 16(b) shows detection of the defect at 20 MHz. The same defect remains undetected at 130 MHz when the Test clock is disabled (Fig. 13(b)). Similarly, a detailed analysis was carried out on 3 more defects (Table1). The second defect caused a multiplier node to be shorted to the Vdd with 1.5KΩ resistor. The transition frequency of this defect was found to be 164 MHz. Defect 3 and 4 caused bridging faults between multiplier nodes with resistances of 1.75 KΩ and 2KΩ resistors respectively. Their transition frequency was found to be 175 and 183 MHz, respectively.

5. Conclusion and Future Directions

High performance testing is fast becoming one of the major concerns for VLSI testing community. Traditional performance edge of VLSI tester over DUT is fast disappearing. As a result, VLSI testers have difficulty in distinguishing between good and faulty devices. Inadequacy of the tester is causing substantial yield losses for high performance ICs. At the same time, owing to limitations of I_{DDQ} testing in deep sub-micron, need for performance testing is increasing for not only ensuring DUT specifications but also for ensuring the DUT reliability.

In this article, we have suggested a DFT technique for high performance testing that enables testing to be performed at significantly lower clock frequency while ensuring the timing specifications of the DUT. Addition of user controllable delays in flip-flops is the key element of this technique. Different types of flip-flops have been evaluated and their performance impact is compared. The effectiveness of the method is demonstrated on a multiplier with realistic defects causing timing failures. The proposed technique do show the potential for high performance testing.

There are many practical issues such as managing skew between the Clock and the Test clock, have not been addressed in this research. In future, we would like to address it along with a chip level implementation.

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