characteristics. The dipole was mounted above a ground plane, which had dimensions of 15 × 15 cm. The *E*-plane patterns for ports 1 and 2 are shown in Fig. 4*a*. The *H*-plane patterns for ports 1 and 2 are shown in Fig. 4*b*. The asymmetries in the pattern can be accounted for by misalignment of the antenna (which was done visually), and radiation by the microstrip feed lines as they come into view at wide angles.

Conclusion: The characteristics of the hybrid ring fed dipole were demonstrated. The hybrid feed provides simultaneous sum and difference element patterns. The difference port can serve as an auxiliary antenna for sidelobe cancellation or mutual coupling compensation. Measurements on a prototype have shown that low return loss and high isolation can be achieved. The major limitation of the design is that the difference pattern cannot be scanned.

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1-bit quantiser with rail to rail input range for sub-1 V ΔΣ modulators

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A new, fully differential comparator with rail to rail input range is presented. This comparator can be used as a 1-bit quantiser in sub-1 V ΔΣ modulators. The quantiser is laid out in 0.18 μm CMOS technology. The post-layout simulation results show that the quantiser is capable of working at 10 MHz with 10 μV resolution. This quantiser is successfully used in 0.8 V first-order and second-order fully differential ΔΣ modulators.

Introduction: Analogue-to-digital converters are one of the main building blocks of most portable electronic equipments, such as cell phones, hearing aids, etc. The increasing demand of longer battery life time of portable equipments has forced circuit designers to use lower supply voltages. However, as the supply voltage is lowered the performance of analogue circuits is degraded and the design of low voltage analogue circuits becomes more challenging. The ΔΣ analogue-to-digital converters are very suitable for low voltage applications. They can be implemented by switched capacitor (SC) circuits and therefore they are more tolerant to circuit non-idealities caused by low supply voltage. However, in a sub-1 V ΔΣ modulator, not only the design of different building blocks becomes more difficult, but also the coupling of these blocks becomes a serious problem.

Fig. 1*a* shows the schematic diagram of a simple first-order ΔΣ modulator. As can be seen, this modulator consists of three capacitors, six switches, an opamp, and a 1-bit quantiser. The design of a low voltage opamp is a nontrivial task. Depending upon which type of transistor (NMOS or PMOS) is used at the input stage of the opamp, its input voltage range will be close to either V_{dd} or *GND*. However, the output voltage of the opamp is normally halfway between V_{dd} and *GND*. In the case of the quantiser, the input range is also close to either of the supply rails. The voltage ranges at the input and output of the opamp as well as at the input of the quantiser are shown in Fig. 1*b*. In this Figure we have assumed PMOS transistors with a threshold voltage of about 0.5 V at the input stage of the opamp and the quantiser. As can be seen in Fig. 1*b*, the output range of the opamp and the input range of the quantiser have a very small overlap. This makes the coupling of these two blocks almost impractical [1]. To overcome this problem, the output voltage of the opamp should be shifted to the lower voltages. This DC shifting is not easy in low voltage circuits and consumes extra power. Alternatively, we can use a quantiser with rail to rail input range. In this way the input voltage range of the quantiser covers complete output voltage range of the opamp. This helps the designer connect the quantiser directly to the opamp.

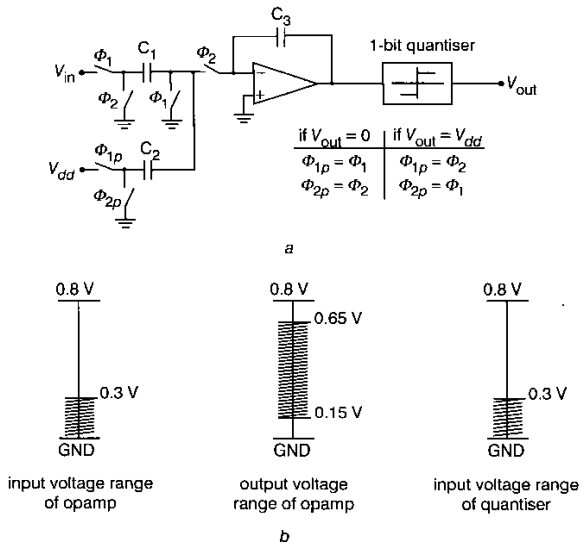

Fig. 1 *Simple first-order ΔΣ modulator and voltage range at different points of circuit*
a Modulator
b Voltage ranges

Using the body of the PMOS transistors in standard CMOS technology, it is possible to design a quantiser with rail to rail input range. In the next Section we propose a new quantiser with rail to rail input range. The quantiser is simulated and laid out in standard 0.18 μm CMOS technology with a typical threshold voltage of around 0.45 V. The post-layout simulation results are also presented.

Proposed quantiser circuit: It is possible to use the body contact of PMOS transistors in a standard CMOS technology to enhance the performance of the analogue and digital circuit [2, 3]. Changing the body potential of a MOSFET transistor causes the drain current to change accordingly (DTMOS technique). We have used the body contact of the PMOS transistors as the input terminals of the quantiser to make a track and latch comparator with rail to rail input range.

Fig. 2 shows the schematic diagram of the quantiser. The gate terminals of the input PMOS transistors (M1 and M2) are connected to ground while the body contacts are used as the input. The comparator (quantiser) has two operational phases which are separated by the *Reset* signal. In case of a ΔΣ modulator the *Reset* is connected to the system clock. When the *Reset* is high, the comparator is in the tracking phase. In this phase the current through transistor M7 is divided between the two transistors M1 and M2. Depending upon the body voltage of these transistors their currents may be different. It is worth mentioning that in a track and latch comparator in the tracking phase, normally the two outputs are shorted to each other by a switch [4]. This method is not suitable for low voltage application, since it is not easy to turn on the switch that connects the two outputs. Therefore, we short the two outputs to the *GND* in order to put the comparator at the metastable point. Transistors M5 and M6 are used for this purpose. When the *Reset*

gets low (latching phase), the voltages at the two outputs start rising. After the output voltages reach a certain value (the switching threshold voltage of the comparator) the cross-coupled transistors M3 and M4 form a positive feedback and, depending upon the initial currents of M1 and M2, one of the outputs goes to V_{dd} and the other one goes to *GND*. When the two outputs reach their final values, they stay there until the *Reset* signal goes high again.

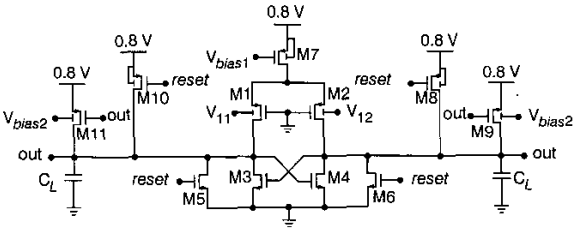

Fig. 2 *Schematic diagram of 1-bit quantiser*

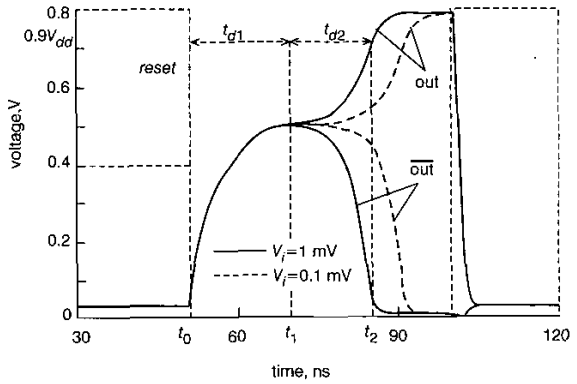

Fig. 3 *Transient response of comparator for two different input levels*

Fig. 3 shows the transient response of the comparator with a capacitive load of 1 pF running at a frequency of 10 MHz. The transient response depicts two cases: (i) $V_i = 1$ mV, and (ii) $V_i = 0.1$ mV. As can be seen when the input has a larger value, the comparator response is faster. This is because the difference between the currents of M1 and M2 is larger. This larger difference enables the quantiser to reach its switching threshold quickly. The delay response of the comparator in the latching phase can be divided into two time periods. In the first period, the two outputs take finite time to charge to the quantiser switching threshold (t_{d1}). During this time the positive feedback is not yet triggered. In the second period after the positive feedback is turned-on, it takes time t_{d2} to reach its final value. These two delay times (t_{d1} and t_{d2}) depend on the differential input voltage (V_i). Table 1 shows t_{d1}, t_{d2}, and the total delay ($t_d = t_{d1} + t_{d2}$) of the comparator for different differential values of V_i. As can be seen, the total delay of the comparator depends on the input voltage. Therefore, there is a compromise between the maximum operating frequency of the comparator and the input voltage resolution (how small the input can be). Post-layout simulation results show (Table 1) that when the differential input voltage is 10 μV, the delay of the comparator is 49.15 ns. This delay should be smaller than half period of the clock. Therefore, running the comparator at a clock frequency of 10 MHz can provide a resolution of 10 μV. Increasing the clock frequency to 12 MHz results in the lowering of the quantiser resolution to 100 μV. In the proposed circuit, transistors M8 to M11 are used to speed up the circuit. These transistors source currents to output nodes after the *Reset* is inactivated. This causes the outputs to rise faster and t_{d1} is reduced. The body of transistors M9 and M11 are biased to reduce their threshold voltage and get the most benefit of them in this low voltage circuit. It is also possible to increase the biasing current and size of the input transistors to reduce the delay. However, this will increase the power consumption of the circuit. Therefore, there is a compromise between speed and power consumption.

Table 1: Delay of comparator for different differential input values

V_i	10 μV	100 μV	1 mV	10 mV
t_{d1} (ns)	26.25	23.05	19.95	16.75
t_{d2} (ns)	22.90	19.20	15.80	12.30
t_d (ns)	49.15	42.25	35.75	29.05

Conclusion: A new comparator using the body of the PMOS transistors is proposed. This comparator can be used as a 1-bit quantiser in sub-1 V ΔΣ modulators. One of the main issues in the design of low voltage analogue circuits is the coupling of different blocks. The input of the proposed quantiser can vary between V_{dd} and *GND*. Therefore, the comparator can be directly connected to the preceding opamp in a ΔΣ modulator. The post-layout simulation results of the comparator, using BSIM3 model, are presented. We have successfully used this comparator in 0.8 V fully differential first-order and second-order ΔΣ modulators as a 1-bit quantiser. The clock frequency of these modulators is 10 MHz. The quantiser consumes a power of 134 μW. The circuit-level simulations show that, with an over sampling ratio of 200, the first-order and the second-order modulators achieve a maximum SNR of 72 and 93 dB, respectively.

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Distributed fibre-optic loss sensor with chirped Bragg grating based on transmission-reflection analysis

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A novel distributed fibre-optic loss sensor with chirped Bragg grating based on the analysis of transmitted and reflected powers is presented. The localisation of loss region with error equal to ±2 mm along the 10 cm chirped grating for 0.7 dB induced loss is demonstrated.

Introduction: Distributed loss fibre-optic sensors are very attractive for the measurement of pressure, temperature, displacement, etc., where the measurand is associated with induced losses [1]. In our previous works we have reported a novel principle for localisation of a loss-inducing perturbation based on transmission-reflection analysis (TRA) using an unmodulated light source with a test fibre having several imprinted short Bragg gratings [2], or utilising the Rayleigh backscattering phenomenon [3, 4]. Localisation of a strong disturbance with a maximum localisation error of a few metres along a few km-long singlemode sensing fibre was demonstrated. However, for some applications it is important to localise even weak alarm-like perturbations with very high accuracy.