Impact of Gate Induced Drain Leakage on Overall Leakage of Submicrometer CMOS VLSI Circuits

Oleg Semenov, Andrzej Pradzynski, *Member, IEEE*, and Manoj Sachdev, *Senior Member, IEEE*

Abstract—In this paper, the impact of gate induced drain leakage (GIDL) on the overall leakage of submicrometer VLSI circuits is studied. GIDL constitutes a serious constraint, with regards to off-state current, in scaled down complimentary metal–oxide–semiconductor (CMOS) devices for DRAM and/or EEPROM applications. Our research shows that the GIDL current is also a serious problem in scaled CMOS digital VLSI circuits. We present the experimental and simulation data of GIDL current as a function of 0.35-μm CMOS technology parameters and layout of CMOS standard cells. The obtained results show that a poorly designed standard cell library for VLSI application may result in extremely high leakage current and poor yield.

Index Terms—Band-to-band tunneling, CMOS ICs reliability, gate-induced leakage current, standard logic cells layout.

I. INTRODUCTION

IN ORDER to optimize future test and yield, it is important to understand the existing failure mechanisms: defect types, defect behavior, changes in defect behaviors over time, and the effectiveness of various tests for detecting defects. Historically, detailed and comprehensive defect data is rarely published, mainly because of confidentiality concerns. In particularly, there is little manufacturing data published about the probability and behavior of defect types such as "timing-only defects," "I_{ddq}-only defects," and "stuck-open defects" [1]. This paper presents the results on the testing and performance investigation of abnormally high leakage current $(\sim 0.1–1 \text{ mA})$ in the drain and LOCOS isolation areas observed during the development of a commercial CMOS chip.

The leakage in the drain is an issue for scaling metal–oxide–semiconductor field-effect transistors (MOSFETs) toward the deep submicrometer regime. The reasons are: 1) the subthreshold conduction increases exponentially with the threshold voltage reduction; 2) the surface band-to-band tunneling (BTBT) or gate-induced drain leakage (GIDL) increases exponentially due to the reduced gate oxide thickness; and 3) the bulk BTBT increases exponentially due to the increased doping concentrations in bulk and well. The GIDL current depends only upon conditions in the immediate gate-to-drain overlap region. This current is very sensitive to the oxide geometry under the edge of the gate: the maximum value of the electric field in drain region is increased by the gate oxide
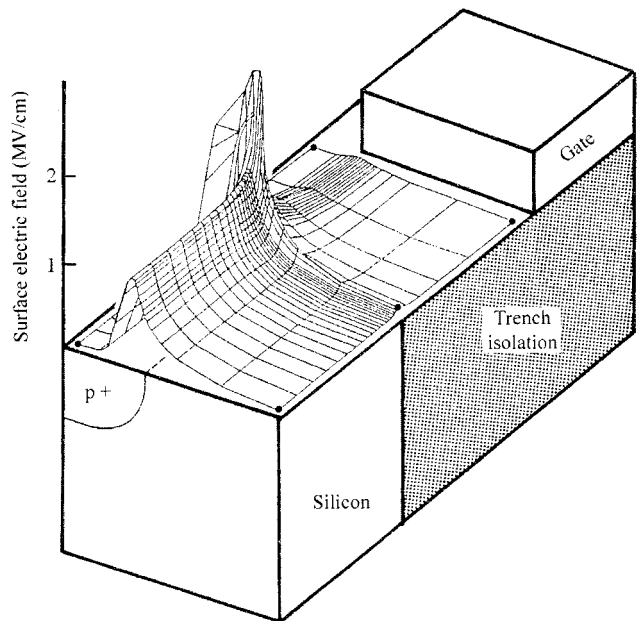
Fig. 1.   3-D perspective view of the surface electric field in DRAM cells [4].

bird's beak or by a imperfect optimization of the drain structure and the gate to drain overlap [2].

Another GIDL mechanism observed in the analyzed chip was mentioned in [3]. In this paper, a mechanism of 64-Mb DRAM circuit degradation was described. The problem was an abnormally high leakage current at the field oxide edges of LOCOS isolation. The constant current time dependent dielectric breakdown (TDDB) tests show that the field-edge structure has shorter lifetime than gate-edge structure. These results strongly support that the buildup of positive charges is one of the reasons for the degradation caused at the field oxide edge. The same mechanism of DRAM circuit degradation was analyzed in IBM scientific journal [4]. Band-to-band leakage current in 16-Mb DRAM circuit with trench isolation was simulated using FIELDAY II a three-dimensional (3-D) device simulator. Fig. 1 shows a plot of the simulated electric field at the device surface, which is enhanced at the "corner" where the gate and the isolation intersect. This high electric field causes GIDL to increase.

This paper is organized as follows: Section II presents an overview of GIDL current in submicrometer CMOS ICs. The description of an analyzed video-broadcasting chip and results of current and scan tests are given in Section III. In Section IV, the key parameters influencing the GIDL current are discussed. Section V deals with the impact of 0.35-μm CMOS processing parameters variation on a leakage current. The results of current
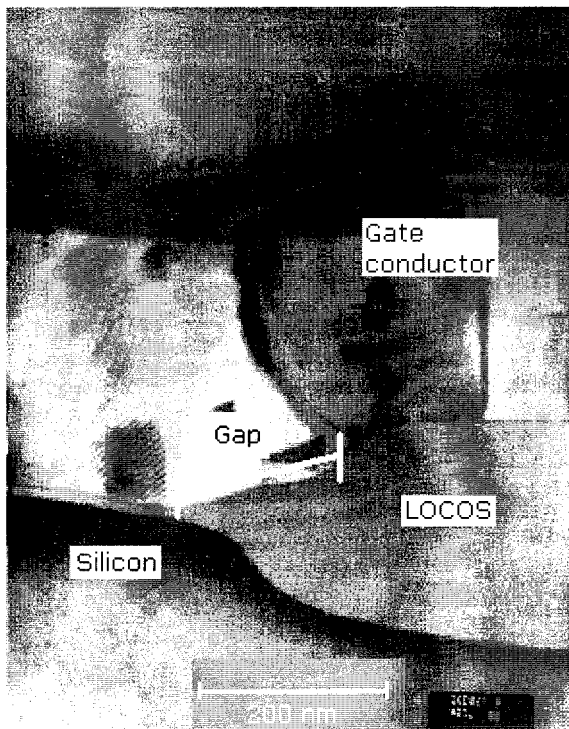
Fig. 2. TEM cross-section of LOCOS isolation in 4-Mb DRAM [4].

Fig. 3. Leakage mechanisms in EEPROM circuit [8].

TABLE I
GENERAL INFORMATION OF DEVICE UNDER TEST

Die size	6.0 mm x 6.0 mm
Maximum probe pins (including all V_{dd} and Gnd)	128
Nominal V_{dd}, V	3.3
Clock Input Frequency, MHz	80
Technology	Double well 0.35 - μm CMOS, 4 level metal.
Approximated transistors number	500, 000
Product type & description	Digital & Video

and scan tests and simulation data are discussed in Section VI. Finally, conclusions are presented in Section VII.

II. PREVIOUS WORK

The GIDL current is induced by band-to-band tunneling effect in strong accumulation mode and generated in the gate-to-drain overlap region. This leakage current has been observed in DRAM trench transistor cells and in EEPROM memory cells. It is identified as the main leakage mechanism of discharging the storage nodes in submicrometer dynamic logic [5]. Hence, these circuits require regular refresh, which is usually provided by a periodic signal.

The earliest reports about the impact of band-to-band tunneling effect on the reliability of 4-Mb DRAM circuits were done in [6], [7]. In these papers, different leakage mechanisms in trench transistor cell were analyzed and band-to-band tunneling leakage mechanism was identified as the dominant one. It was found that the tunneling was occurred at the overlap of the bit-line node to the transfer gate. Similarly, the IBM research on leakage current mechanisms in DRAM circuits found tunneling leakage current in overlap region of LOCOS isolation and gate conductor line [4]. To avoid the band-to-band tunneling leakage, it was proposed to form a space ("Gap") between "birds-beak" of LOCOS isolation and edge of gate conductor line (Fig. 2).

The band-to-band tunneling leakage current is also the main cause of nonvolatile memory ("flash EEPROM") circuits degradation. In these circuits the electrical erase relies on the charge transport through oxide in the n^+ diffusion and floating-gate overlap region and the tunneling leakage usually cannot be avoided [8]. Fig. 3 illustrates these mechanisms of the leakage current.
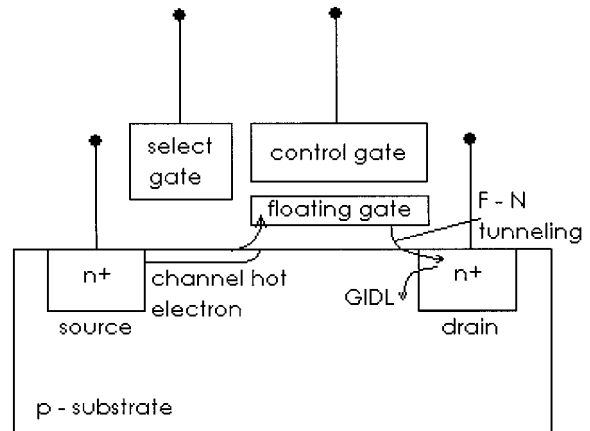
The reliability problems of submicrometer CMOS logic circuits as a result of technology scaling are discussed in [9]–[11]. Thinning of gate oxide, increasing of substrate doping concentration, doping concentration in LDD and drain regions enhance the electric field dependence of GIDL. These papers conclude that GIDL is a major obstacle in leakage current reduction in submicrometer CMOS logic circuits.

A short review of tunneling effect impact on the reliability of different CMOS circuits presented in this section shows that the reliability of a wide class of CMOS circuits is reduced as a result of GIDL current. This problem becomes crucial in view of the rapid CMOS technology scaling.

III. DEVICE UNDER TEST

In this paper, we analyze the reasons of abnormally high leakage current observed during characterization of a digital chip implemented in a standard 0.35-μm CMOS process. The general information about DUT is given in Table I.

A. Logic and Leakage Current Tests

Logic blocks in the DUT are tested with full scan methodology. Logic testing is implemented on the automated test equipment (ATE) HP83000 F660 (1.3-GHz data rate) and has stuck-at fault coverage approximately 95%. Devices, that are successfully passed logic testing, are then tested for the leakage current. Fig. 4 shows the results of logic and current testing of chips in a wafer. The typical results of the statistical variation of leakage current for different wafers from the same lot are presented in Fig. 5. All wafers in this figure had a nominal polymask bias (zero polymask bias). Other wafers from this lot,
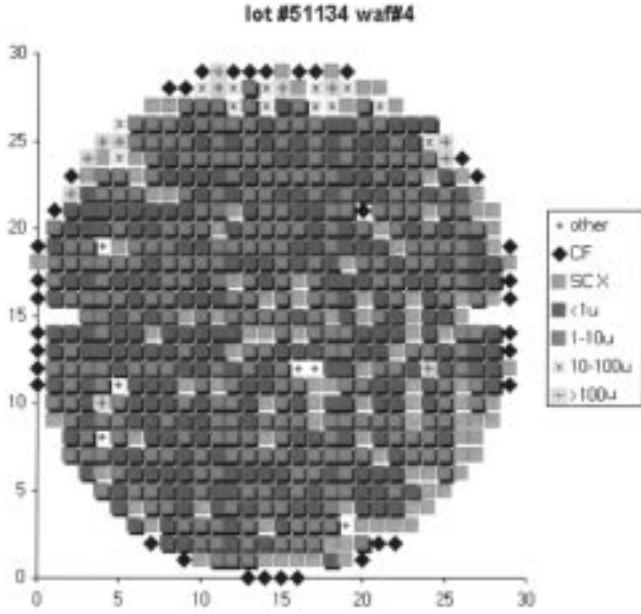
Fig. 4. Logic and current measurement results of chips testing in a wafer (SCX—logic test failed, CF—contact to the chip is failed).

which are not shown in Fig. 5, had increased ($+0.02$ μm) or reduced (-0.02 μm) polymask bias. The detailed description of mask bias technique in submicrometer optical lithography is presented in [12].

The distribution and leakage current values are significantly related to the polysilicon mask bias (± 0.02 μm) as shown in Fig. 6. In this case, the polysilicon mask was biased on -0.02 μm and the gap between the polysilicon line and the active areas was increased. As a result the leakage current of analyzed chips is reduced ten times. When the polysilicon mask was biased on $+0.02$ μm, the leakage current of analyzed chips is increased approximately five times. The average leakage current of the chips is 0.1–1 mA ($\sim 0.4 \times 10^{-9}$–4×10^{-9} A/transistor). Consequently, the current testing results show the strong dependence of the leakage current on the accuracy of polysilicon lines alignment to the diffusion edge or LOCOS bird's beak. Note that the nominal leakage current of a MOSFET is 10 pA/μm and chip has 500 000 transistors. Approximately half of the total number of transistors are off. The average width of transistors in analyzed chip is 5 μm. It means that we should expect the leakage current in defect free case at the level of 12.5 μA.

In order to do the root cause analysis of the fault, photon-emission microscopy (PEM) is applied on the analyzed samples. PEM measures the photons emitted when transistors are improperly saturated or when defect sites are passing current. The results of PEM are given in Fig. 7. Analysis of hot spots allows us to find standard cells that may have abnormally high leakage current. The typical design of these cells is shown in Fig. 8. In this figure, black lines indicate possible leakage current locations. These are the overlap regions of polysilicon lines and diffusion regions that are formed as a result of lateral diffusion. It was found that 30% of logic cells had large overlap regions. The total number of cells in a chip is 89 304.

To explain measurement results, the theory of band-to-band tunneling current and the impact of processing parameters variation on the leakage current should be considered.

IV. PARAMETERS INFLUENCING GIDL CURRENT

It is known that GIDL current is attributed to the tunneling, which is taking place in the deep depleted drain region underneath the gate region. Several mechanisms have been proposed to describe the behavior of GIDL current, for example the indirect band-to-band tunneling model presented in [13] and the band-trap-band tunneling model explained in [14]. However, based on qualitative agreement between experiments and theory, the band-to-band tunneling has been identified as the major leakage mechanism. In this section we describe the origin of GIDL current and present the main parameters, which impact on the GIDL current value.

The GIDL current is due to the potential difference applied between drain and gate. A strong depletion region is therefore formed under the gate-to-drain overlap region. The presence of a gate-induced high electric field entails the overlap of silicon energy bands and breeds the emission of minority carriers. These minority carriers will be in transit by band-to-band tunneling from the valence band to conduction band of silicon. The electrons emitted at the surface of the deep depletion layer are collected by the drain and move toward the substrate, under the transversal electric field effect [15]. Note that tunneling is only possible in the presence of a high electric field. The field in silicon at the Si–SiO$_2$ interface depends on the doping concentration in the diffusion region and the difference between V_d and V_g, i.e., V_{dg}.

The simple 1-D band-to-band tunneling current model was presented in [16]. Band-to-band tunneling current density is the highest where the electric field is the largest. The theory of tunneling current predicts:

$$I_{\mathrm{gidl}} = A \cdot E_s \exp\left(\frac{-B}{E_s}\right) \tag{1}$$

where A is a constant [15]:

$$A = \frac{q^2 \cdot m_r^{1/2}}{18 \cdot \pi \cdot h^2 \cdot E_{\mathrm{gap}}^{3/2}} \tag{2}$$

$$B = \frac{\pi \cdot m_r^{1/2} \cdot E_{\mathrm{gap}}^{3/2}}{2\sqrt{2} \cdot q \cdot \hbar} = 21.3\,\mathrm{MV/cm} \tag{3}$$

with $m_r = 0.2\,\mathrm{m_0}$ (electron effective mass). E_{gap} is the direct energy gap of silicon (~ 3.5 eV) [17].

E_s is the surface electric field at the tunneling point in the gate-to-drain overlap region and can be obtained as follows [16]:

$$E_s \approx \frac{V_{\mathrm{gd}} - 1.2}{3T_{\mathrm{ox}}}. \tag{4}$$

This is the vertical electric field at silicon surface, "3" is the ratio of silicon permittivity to oxide permittivity, T_{ox} is the oxide
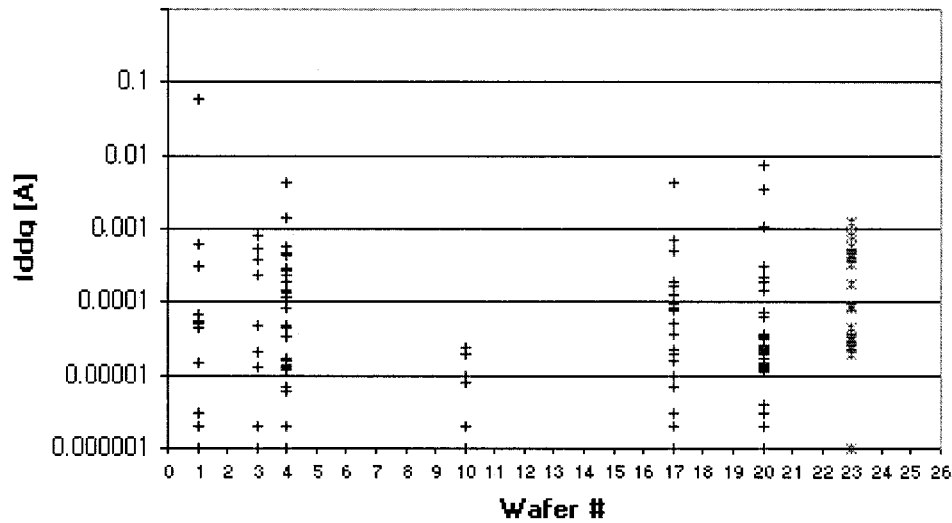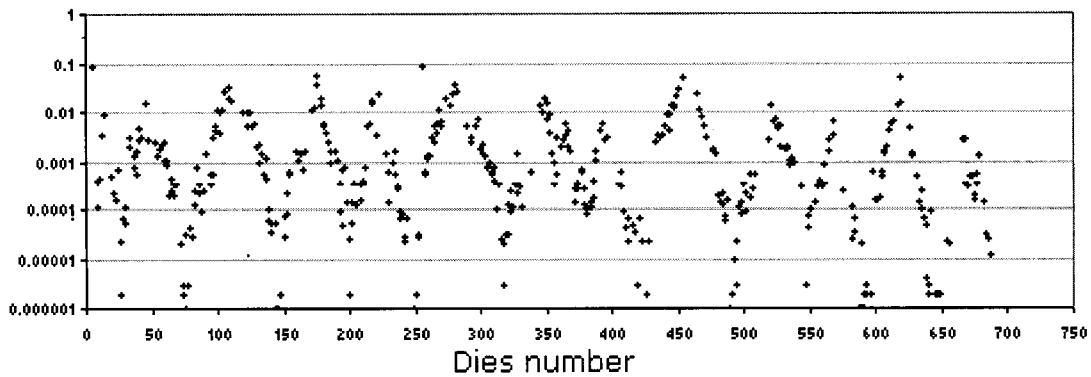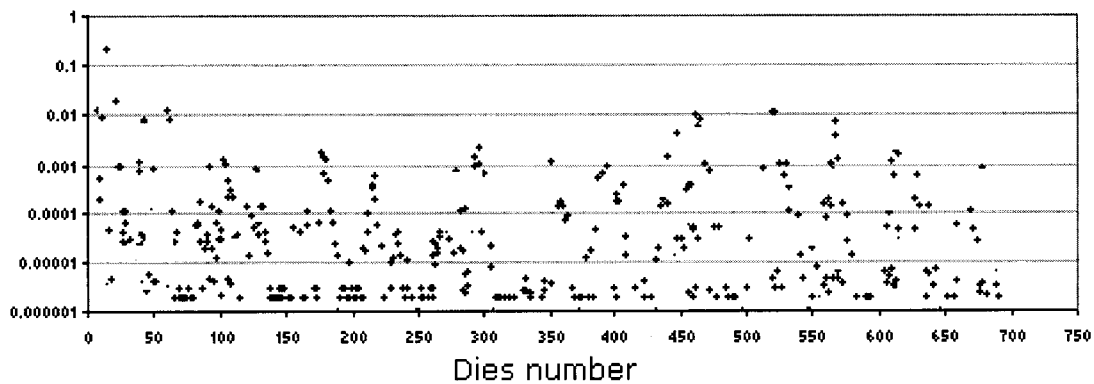
Fig. 5. Statistical variation of leakage current values for different wafers in a one lot.

(a)

(b)

Fig. 6. I_{ddq} testing results at nominal polymask bias (a) and after poly silicon mask bias on $-0.02\ \mu$m (b).

thickness in the overlap region in centimeters and V_{gd} represents the gate to drain voltage in volts. A bend bending of 1.2 eV is the minimum necessary for band-to-band tunneling to occur.

The described one–dimensional (1-D) band-to-band tunneling current model will be used in Section V for GIDL current calculation of submicrometer n-MOSFET.
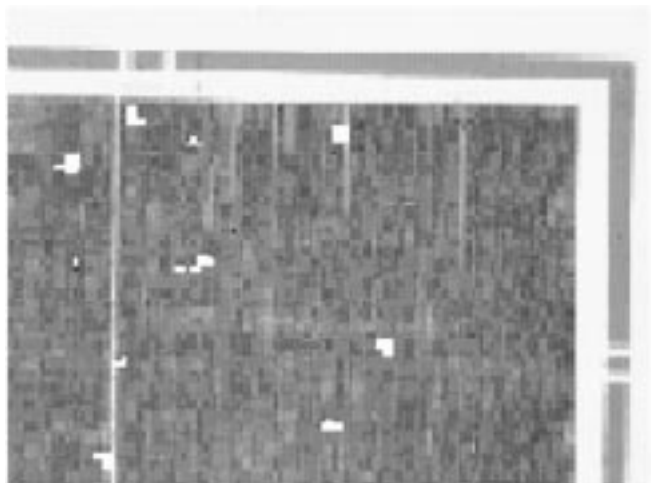
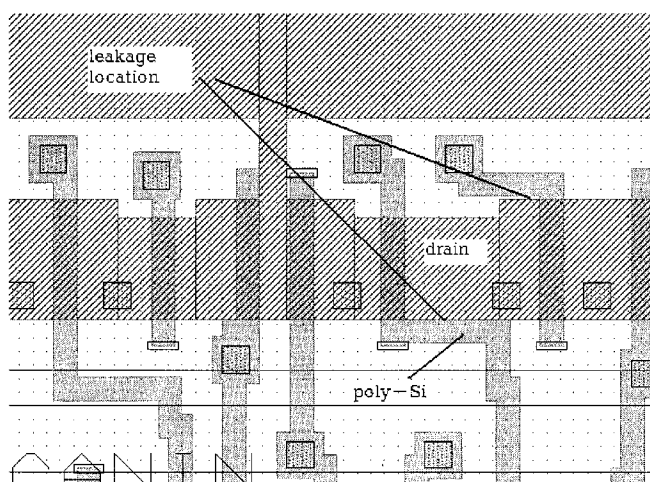Fig. 7. PEM image fragment of the analyzed chip (hot spots have a white color).

Fig. 9. Variation of the GIDL current as a function of the temperature [15].

Fig. 8. Section of standard flip-flop cell layout.
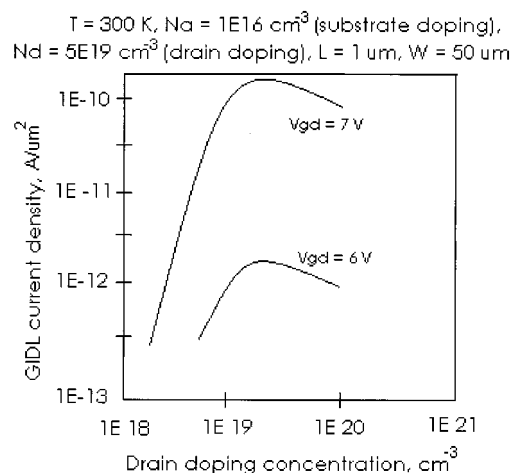
Fig. 10. Effect of drain impurity concentration on GIDL current density [15].

A. Impact of Temperature on GIDL Current

The GIDL current depends on temperature, because band gap (E_{gap}) has a small temperature dependence [18]:

$$E_{gap}(eV) = 1.12 - 2.4 \times 10^{-4} \times (T - 300) \qquad (5)$$

T is the temperature in Kelvin. The experimental GIDL curves as a function of temperature for the n-MOSFET under test is presented in [15]. The results show the exponential dependence of GIDL current on temperature (Fig. 9). On the basis of this graph, we can conclude that the GIDL current may increase in submicrometer ULSI circuits, because the operating temperature of the chip will be increased due to the increased current density and transistor numbers.

B. Impact of Oxide Thickness Reduction and Drain Doping Concentration on GIDL Current

As a result of technology scaling, the gate oxide thickness is dramatically reduced. This is translated to an increase of the electric field at the surface of the drain-gate overlap region (4), that favors the transit of the electrons by band-to-band tunneling. Therefore, the band-to-band tunneling rate increases and entails
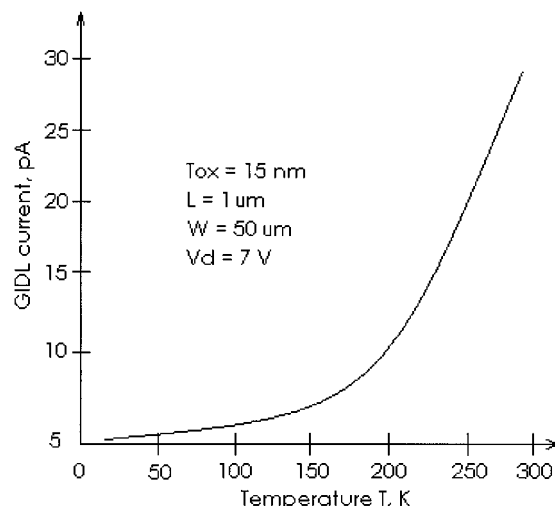
an increase of the GIDL current. For an oxide thickness variation of 8–20 nm, the GIDL current varies about eight decades for a zero gate bias [15].

The impurity concentration in the gate-to-drain overlap region plays an important role in the evolution of the GIDL current. This tendency is shown in Fig. 10 [15]. As the drain doping concentration increases, the depletion layer width becomes less and the electrical field in the depletion layer increases. It favors the carrier's generation by band-to-band tunneling effect, and hence, the GIDL current increases. Note that the source/drain and substrate doping concentration is increased under the technology scaling. The GIDL current model considering the effect of drain doping concentration was proposed in [19].

Although, the supply rail voltage is reduced under technology scaling, the increase of operating temperature and doping concentration, and decrease of gate oxide thickness cause an increase of GIDL current in submicrometer MOSFETs.

V. IMPACT OF TECHNOLOGY PARAMETERS ON OVERALL LEAKAGE CURRENT: SIMULATION RESULTS

The random variability of the parameters of the semi-conductor fabrication process is reflected in the corresponding stochastic spread of circuit performance [20]. This is due to the fact
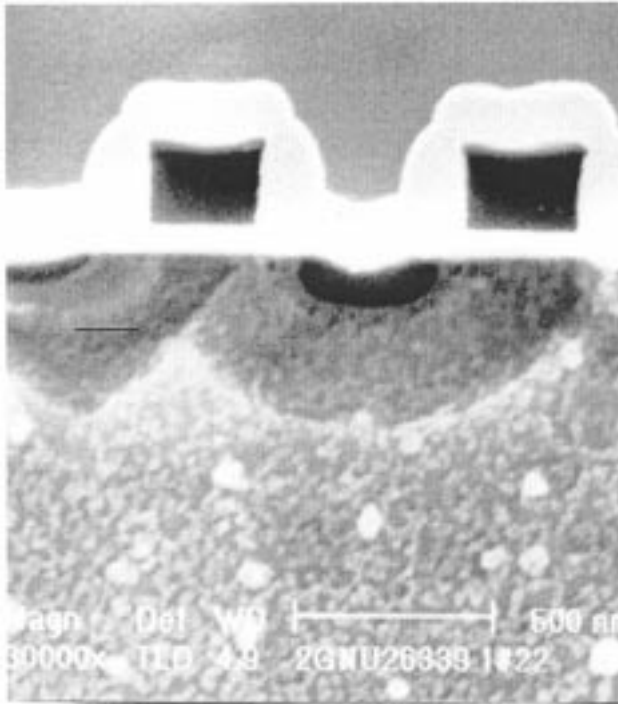
Fig. 11. TEM cross-section of test MOSFET ($L_{\text{eff}} = 0.32\ \mu$m).

TABLE II
N-MOSFET SIMULATION PARAMETERS FOR SHORT CHANNEL EFFECTS

Parameter	Value	Unit
Substrate doping	5×10^{15} (p -type)	cm^{-3}
Source/Drain doping	1×10^{20} (n -type)	cm^{-3}
V_{th} adjusted doping:		
"short-channel" case	1.1×10^{18} (p-type)	cm^{-3}
"long-channel" case	1.6×10^{18} (p-type)	cm^{-3}
Punch-through doping	2×10^{17} (p-type)	cm^{-3}
L_{eff}/W:		
"short-channel" case	0.28/5	μm/μm
"long-channel" case	0.37/5	μm/μm
Gate oxide thickness	65	Å

TABLE III
N-MOSFET SIMULATION RESULTS

Parameter	"Long-Channel" case	"Short-Channel" case
$V_{\text{th,}}$ V	0.73	0.51
$I_{\text{sat,}}$ mA	2.3	3.0
$I_{\text{off,}}$ pA	15	5000

inversion leakage current component in a total leakage current as a result of short-channel effect can not explain the abnormally high leakage current observed in the tested chips. Note that the nominal total leakage current of MOSFET for 0.35-μm CMOS technology in CSM Corporation is 10 pA/μm.

B. Lateral Diffusion in Source/Drain Regions

Other problems of submicrometer CMOS technology are the fluctuations in the location of dopant atoms in the device active regions and the lateral diffusion of doping impurity in gate-to-source and gate-to-drain overlap regions. These effects reduce the threshold voltage and induce drain current fluctuations. The lateral diffusion distance of boron for the MOSFET source/drain has been investigated in [22]. The analyzed transistor has 0.32 μm effective gate length and 50 μm gate width. The ion implantation process for source/drain region fabrication has the following parameters: energy -1 keV, dose -1×10^{15} cm^{-2}, temperature -1050 °C, and time -10 s. The lateral diffusion distance for 5×10^{18} cm^{-3} doping level is 72 nm. Finally, it is founded that the lateral diffusion distance at the p–n junction is about 0.6 times the vertical distance for the 80–100-nm junctions. This result is then used in the GIDL current simulation.

C. Band-to-Band Tunneling Leakage Current in Gate-to-Drain Overlap Region

As it is discussed in Section II, GIDL current is one of the dominant reasons of submicrometer CMOS circuits degradation. Thus we attempt to estimate the GIDL current value as the function of gate-to-drain overlap width. This simulation is done in the Microtec device simulator. For this purpose, the "long-channel" case of n-MOSFET (Table II) is used. The cross-section of the analyzed transistor is shown in Fig. 12. Generally, the band-to-band tunneling current depends on Gate-Drain voltage (V_{gd}), vertical and lateral electric field in channel region, drain-doping concentration, gate oxide thickness, width of gate-drain overlap region and temperature [15], [19]. In our research, we assume that the operating temperature is room temperature. The electrostatic potential voltage that has impact on tunneling current can be described as $V(x) = V_{\text{gd}} + V_{\text{FB}}$ [13], where V_{FB} is the flat-band voltage in the gate region. For 0.35 μm CMOS technology, the nominal V_{dd} and V_{gdmax} are

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that the fabrication equipment, materials, and control variables cannot be controlled with infinite precision, but only within given tolerances. As their values drift and fluctuate over time, devices belonging to different wafers and lots are processed with slightly different physical and environmental conditions. Another source of randomness is the imperfect spatial uniformity of the processing steps (for example, gas flows, etching, and deposition of materials, ion implantation, CMP, etc.). It causes differences in the geometry and the composition of different patterned layers on the same chip and the same wafer. The effect of equipment, material drift, fluctuations, and process nonuniformity, introduces spatial and temporal variations of the electrical device parameters and increases power consumption per chip [20].

A. Short-Channel Effect

The TEM cross-sections (see example in Fig. 11) and the electric measurements of the n-MOSFETs under test show that for the given technology the effective channel length (L_{eff}) is changed from 0.28 to 0.37 μm (the nominal channel length is 0.35 μm) and the threshold voltage (V_{th}) is changed from 0.5 V to 0.7 V (the nominal threshold voltage is 0.64 V). The impact of short-channel effects on MOSFET weak inversion leakage current has been investigated through the simulation of "the long-channel" and "the short-channel" cases in 2-D device simulator Microtec [21].

Technology parameters of the n-MOSFET that are used for simulations are given in Table II. The simulation results are presented in Table III. These results show that technology parameters' variation significantly influences the leakage current value in MOSFET and consequently influences the total leakage current of the fabricated chip. However, we found that the weak
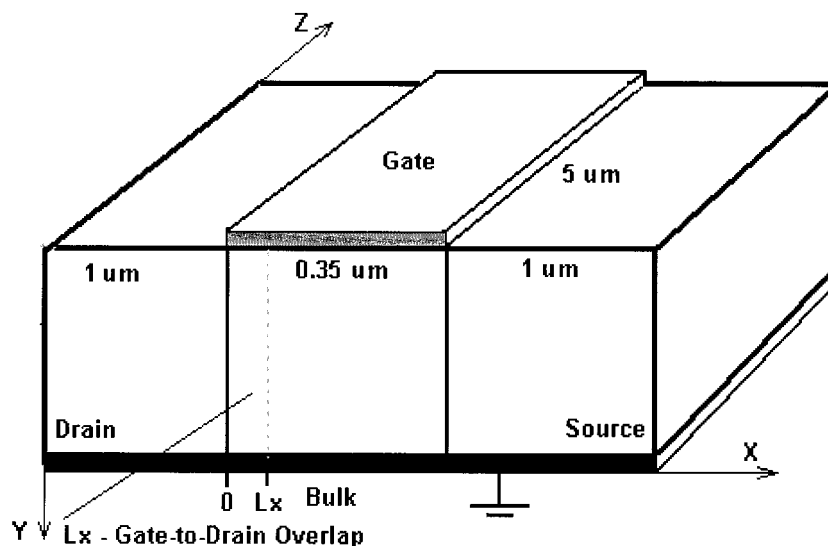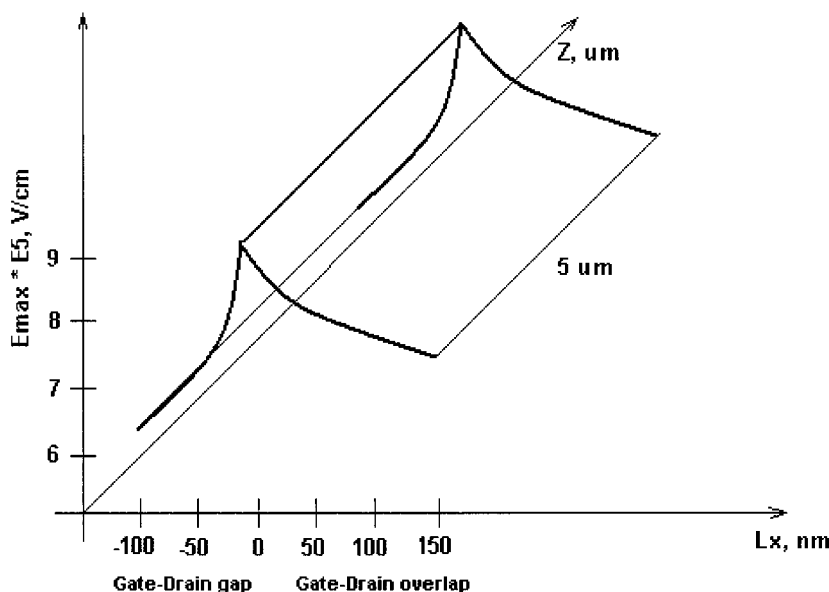
Fig. 12.   Cross section of analyzed n-MOSFET.

Fig. 13.   2-D electric field distribution in $L_x - Z$ plane.

both 3.3 V. From the simulations, the distribution of vertical and lateral electric fields as a function of gate-to-drain overlap (L_x) is obtained. The simulations are done for $L_x = -100$ nm, -50 nm, 0, 50, 100, and 150 nm. The distribution of the maximum electric field as a function of gate-drain overlap is shown in Fig. 13.

At the second step, the tunneling leakage current is calculated using simple 1-D band-to-band tunneling current model (1), which is discussed in Section IV. The value of maximum electric field (E_s) in the depletion layer of gate-to-drain overlap region is estimated as 9.1×10^5 V/cm from simulations. Constant B (3) is 21.3 MV/cm where m_r is the reduced mass of electron given by [15]. Constant A is calculated from (1). The experimental graph I_{gidl} versus V_{gd}, which has been presented in [23] gives $A = 2.06 \times 10^{-6}$ [A/V×cm]. The calculation of the band-to-band tunneled leakage current by (1) gives the result of $I_{gidl} = 1.29 \times 10^{-10}$ A/μm^2 for the analyzed n-MOSFET. The effective area of tunneled leakage current (S) is $W \times L_x$, where W is the channel width and L_x is the gate-to-drain overlap

length. In our case, W is 5 μm and L_x is 72 nm (see Section V-B). Thus, the effective area of tunneled leakage current is 0.36 μm^2. Therefore, the total band-to-band tunneling leakage current is 4.6×10^{-11} A. Note that the nominal total leakage current of the MOSFET for 0.35-μm CMOS technology in CSM Corporation is 10 pA/μm. Thus the analyzed MOSFET of 5 μm width should have 50 pA of the leakage current. It means that lateral diffusion of source/drain regions and tunneling effect may double the nominal leakage current.

D. Leakage Current at LOCOS Isolation Edge

As the packing density of integrated circuits increases, the peripheral length surrounding the active region per unit area becomes longer. The leakage phenomenon at the local oxidation of silicon (LOCOS) isolation edge, caused by the recombination and generation process, has become a major issue for discussion. In this section, we consider leakage current generation because of tunneling effect in an overlap region of polysilicon con-
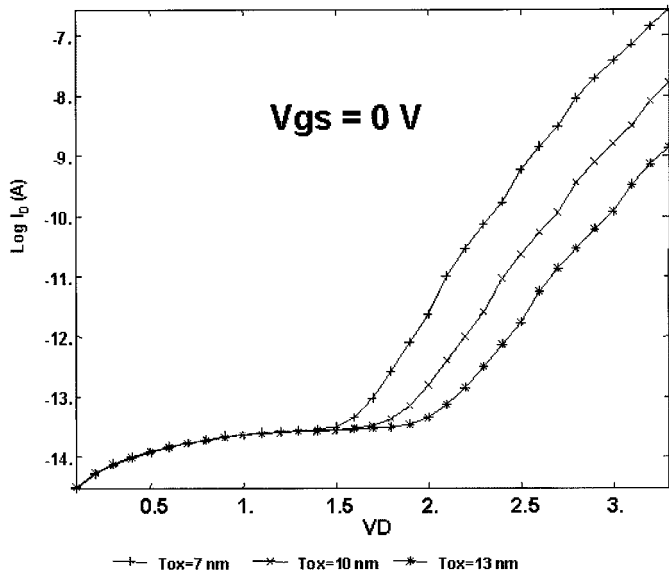
Fig. 14. GIDL leakage current in pseudo-LOCOS structure (N_{ss} = $1E12$ cm^{-2} eV^{-1}).

ductor line and LOCOS bird's beak, because typically 0.35-μm CMOS technology uses LOCOS process for MOSFETs insulation in the chip. The analyzed situation is shown in Fig. 2. However, we assume that the polysilicon conductor is deposited directly at LOCOS bird's beak. The simulation of GIDL current in pseudo-LOCOS structure is done in Microtec device simulator [21]. Standard MOSFET structure ($W/L = 5$ μm/0.35 μm) with three different values of gate oxide thickness is used in a pseudo-LOCOS structure. Typically, p-channel stop layer is formed under LOCOS bird's beak. In our simulation, we use the p-channel stop layer, which has the following parameters: implantation energy -260 keV, dose -4×10^{12} cm^{-2}. Note that the LOCOS bird's beak region has a large density of electrically active defects (N_{ss}). C–V measurements, which are done in [24], [25], show that the typical N_{ss} value is 1×10^{12} cm^{-2} eV^{-1} and this means that its density is almost two order of magnitude larger than the one observed at the SiO$_2$/Si interface grown on a (100) Si plane.

The simulation results are shown in Fig. 14, where drain current (I_d) is the drain-to-substrate GIDL current. The obtained results show that the GIDL current is a strong function of gate oxide thickness. Since the actual LOCOS oxide thickness is increasing quickly with the distance from the thin (pad) oxide, the leakage current may be reduced to an acceptable level (~ 1 nA) if the distance from polysilicon line to the LOCOS edge is approximately 0.02 μm. In this case the LOCOS oxide thickness is increased from 7 to 13 nm. Another method, which can significantly reduce the GIDL current at the LOCOS edge, is the low-temperature hydrogen annealing at $400\ ^\circ$C. In this case, the interface charge density in LOCOS bird's beak region is reduced [26].

VI. ANALYSIS OF TESTING AND SIMULATION DATA

Strong dependence of the leakage current on bias of polysilicon line or layer to layer alignment (Fig. 6) shows indirectly that the possible reason of the leakage current, is the GIDL current at the LOCOS edge. This leakage mechanism was analyzed
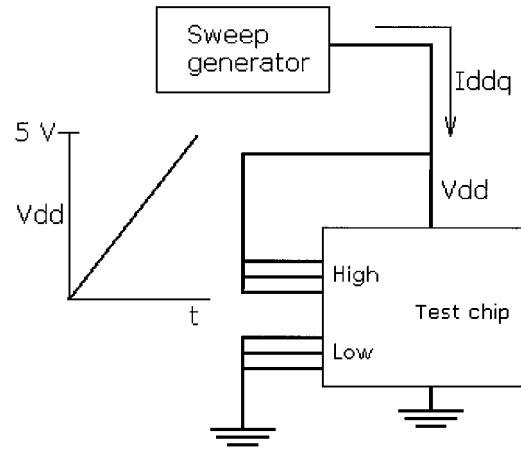

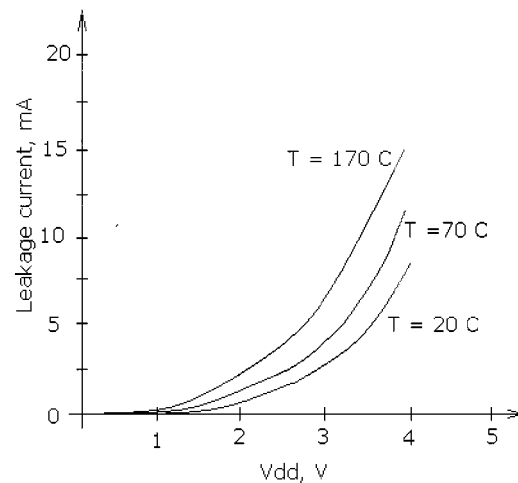Fig. 15. Setup of leakage current measurement.

Fig. 16. Leakage current of the test chip as function of V_{dd} and temperature.

in Section V-D. The measured average leakage current of the chip is 1 mA or $\sim 4 \times 10^{-9}$ A/transistor. The simulation of GIDL current at the LOCOS edge gives the leakage current close to this value. This fact shows that the GIDL is the possible reason of observed abnormally high leakage current. To check this assumption, the temperature dependence of the leakage current is measured. The current measurement setup is shown in Fig. 15. With the device properly initialized and with its signal-input pins set to appropriate logic states, V_{dd} is varied while I_{ddq} is measured. Device without defects usually has a flat, low current (< 10 μA) signature. All inputs of the analyzed chip were grounded in this experiment. The GIDL current as a function of temperature is analyzed in Section IV-A. The obtained results are shown in Fig. 16. Note that the breakdown voltage is reduced as temperature increases. This fact may have the following explanation. Since the band-gap energy (E_g) in silicon decreases with increasing temperature, the breakdown voltage due to tunneling effect has a negative temperature coefficient; that is, the breakdown voltage decreases with increasing temperature [27]. The obtained results confirm the band-to-band tunneling origin of leakage current in the DUT. To reduce GIDL current component of DUT off-state leakage current, the layout of standard cells was modified as shown in Fig. 17. The gap between polysilicon lines and device active regions was set to
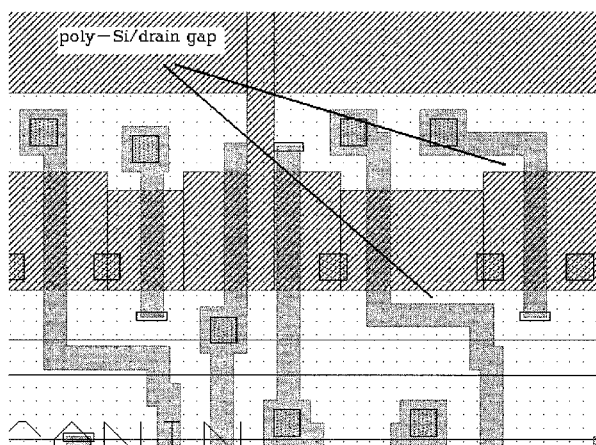
Fig. 17.   Section of corrected flip-flop layout.

0.2 μm. As a result the leakage current of analyzed chip was reduced to the acceptable level ($\sim$10–15 μA).

VII. CONCLUSION

Contribution of GIDL leakage to overall leakage for DRAMs and EEPROMs has been widely investigated. However, for logic VLSI circuits its impact on overall leakage and current testing has not been widely analyzed. In this paper, the submicrometer CMOC ICs degradation due to GIDL current is studied. This leakage current is commonly attributed to band-to-band tunneling near the gate-to-drain overlap region. The impact of technology/environmental parameters such as temperature, lateral diffusion in source/drain regions and LOCOS bird's beak thickness on GIDL current is investigated. The influence of 0.35-μm CMOS technology parameters variation on the overall leakage current is also presented. The following results are obtained.

1) The variation of V_{th} and L_{eff} increases the weak inversion component of off-state leakage current significantly. As example when V_{th} and L_{eff} are increased from the nominal values of 0.64 V and 0.35 μm to 0.73 V and 0.37 μm the off-state leakage current is reduced. At the same time when V_{th} and L_{eff} are reduced from the nominal values to 0.51 V and 0.28 μm the off-state leakage current is increased. The total variation of off-state leakage current for these two cases was found to be three orders of magnitude.

2) The lateral diffusion of source/drain regions may induce greater tunneling effect and increase the leakage current two times from the nominal value for the given technology.

3) The high charge trapped density (N_{ss}) in a LOCOS edge may dramatically increase GIDL current from 10×10^{-12} A to 1×10^{-7} A per transistor.

4) GIDL current may be the crucial factor of off-state leakage current degradation in digital submicrometer CMOS circuits in case of improper standard library cells layout.

5) The layout correction of standard library cells allowed to significantly reduce the overall leakage current of analyzed chip from 0.1–1 mA to 10–15 μA.

The recently published data [28], [29] show that shallow trench isolation (STI) structures have high interface trap density in trench sidewalls. As a result the junction leakage current is significantly increased when active regions of transistor are located close to trench sidewalls. This problem was observed in DRAM circuits, implemented in 0.25-μm CMOS technology. Hence, GIDL current is the crucial factor of off-state leakage current degradation in deep submicrometer CMOS circuits as well.

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Andrzej Pradzynski (M'97) received M.S. degree in physics in 1972 from University of Warsaw, Warsaw, Poland.

From 1974 to 1986 he has assumed various positions in CEMI—a semiconductor manufacturer in Poland, with primary focus on process development, yield improvement, and product engineering. In 1998, he moved to Canada. He is now a Principal Engineer in Process Engineering department in Gennum Corporation, Burlington, ON, Canada being primarily responsible for yield management and engineering support for internal and foundry based processes engaged in Gennum.

Manoj Sachdev (M'87–SM'97) received the B.E. degree (with honors) in electronics and communication engineering from University of Roorkee, India, and the Ph.D. degree from Brunel University, U.K.

He was with Semiconductor Complex Limited, Chandigarh, India, from 1984 till 1989, where he designed CMOS Integrated Circuits. From 1989 till 1992, he worked in SGS-Thomson at Agrate, Milan, Italy. In 1992, he joined Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on various aspects of VLSI testing and manufacturing. He is an Associate Professor in electrical and computer engineering department at University of Waterloo, Canada. His research interests include low power and high performance circuit design, test and manufacturing issues of integrated circuits. He has written a book, two book chapters on testing and has published significantly in refereed conferences and journals. He received the best paper award for his paper in European Design and Test Conference, 1997 and an honorable mention award for his paper in International Test Conference, 1998. He holds several granted and pending patents in the area of VLSI design and test.

Oleg Semenov received the engineer degree (with honors) and doctor of science degree in microelectronics technology from the Moscow Institute of Electronics Engineering (Technical University), Russia, in 1993 and 1996 respectively, and the M.Sc. degree in electrical engineering from the University of Waterloo, Canada, in 2001.

He was with Joint Stock Company (Hong Kong-Russia) "Korona Semiconductor", Moscow from 1996 till 1998 where he worked as a Process Engineer. He is currently with the VLSI research group at the University of Waterloo. His research interests include reliability and testing of submicrometer CMOS ICs and impact of technology scaling on MOSFET characteristics.