Impact of Power Dissipation on Burn-in Test Environment for Sub-micron Technologies

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Abstract

The leakage power is expected to increase with scaling of CMOS technology. The increased leakage is a strong function of the elavated temperature and voltage stress. As a consequence, under the burn-in conditions the elevated leakage power may cause increased post Burn-in fallout. In this paper the impact of elevated leakage during burn-in environment on post BI yield is analized. We have also shown that to maintain a constant post-BI yield loss, the burn-in temperature should go down by $10°C$ for each technology generation.

Key words: CMOS, Yield, Burn-in, Thermal Stress

1 Introduction

Burn-in (BI) is an important test technique to weed out infant mortality from the main population. As a result, quality and reliability of outgoing Integrated Circuits (ICs) are improved. During the BI, ICs are subjected to elevated voltage and temperature stress. As a consequence, the field and temperature enhanced failure mechanisms are accelerated [1]. Optimizing the effectiveness of BI test has been the constant focus of quality and reliability engineers.

As we scale the transistor to deep sub-micron regime, it's off state leakage increases significantly. A linear reduction in transistor threshold voltage with technology scaling, results in exponential increase in its leakage. This leakage is further increased under voltage and temperature stress conditions. High leakage causes further elevation in chip temperature and eventually leads to a positive feedback. Therefore, handling the power dissipation, becomes an important consideration during the burn-in. In this article, we investigate static power dissipation as a function of temperature. The objective is to minimize the burn-in temperature, while maintaining constant yield during the burn-in test for future technologies

2 Leakage Components and Power Issues

Several short channel effects contribute to I_{off} in a deep-submicron transistor. Keshavarzi et al. lists eight leakage mechanisms, which are shown in Fig. 1 [2].These leakage components, collectively referred to as short channel effects, include the following:

- I_1 is pn-junction reverse-bias current.
- I_2 is weak inversion current.
- I_3 is drain-induced, barrier-lowering (DIBL) current.
- I_4 is gate-induced, drain-leakage (GIDL) current.
- I_5 is punch-through current.
- I_6 is narrow-width-effect current.
- I_7 is gate-oxide-tunnelling current.
- I_8 is hot-carrier-injection current.

Among these leakage components weak inversion (subthreshold), GIDL and DIBL contribute the most to the total leakage current. Since subthreshold current is a strong function of temperature, in burn-in conditions it increases dramatically, and causes a large portion of total leakage current. The total leakage of a transistor in $0.18\mu m$ technology

as a function of temperature and voltage stress is shown in Fig. 2. In this figure it can be seen that the leakage increases exponentially as a function of temperature. This increase in leakage is estimated to be as much as by three order of magnitude from the nominal conditions ($40pA/\mu$ for $T = 25°C$ and $V_{dd} = 1.8V$).

The die temperature, commonly referred as the junction temperature or T_j, is defined as [3]:

$$T_j = T_a + P \times \theta_{ja} \tag{1}$$

$$P = P_{Dynamic} + P_{Static} \tag{2}$$

$$P_{Static} = I_{Leak} \times V_{dd} \tag{3}$$

where T_a is the ambient or set point temperature, P is the device total power, and θ_{ja} is the junction-to-ambient thermal resistance. In equation 2, the dynamic power is $C.V_{dd}^2.f$ where C is the total circuit capacitance and f is clock frequency. Since in BI environment, the device operates at lower frequensy (often 1/1000th), the dynamic portion of power dissipation can be ignored. On the other hand, the leakage power component is elevated. Combining all leakage components, and using curve fitting techniques, it can be shown that transistor leakage is an exponential function of the die temperature:

$$I_{off} = f(T_j) = Ae^{\frac{(T_j+B)(T_j+C)}{D}} \tag{4}$$

where A is a prefactor and B, C, and D are constants which are used to fit the function to the experimental data. The power of the high performance circuits is increasing with respect to comming technology generations. Fig. 3 illustrates power and temperature tendencies future technologies [4]. From these tendencies and above mentioned equations, it can be safly concluded that the elevated temperature results into excessive power dissipation causing further increase in temperature. In other words, resulting in a positive feedback mechanism that may eventually lead to a thermal runaway. Therefore experts have been trying to limit the leakage current using techniques such as back body biasing [5], dual-threshold transistors [11], and dynamic threshold transistors [6][7], to reduce the static power dissipation.

Besides the circuit techniques to limit the static current leakage, researchers have been trying to reduce thermal resistance (θ_{aj}). In Equation 1, T_j or junction temperature is linearly dependent on thermal resistance, θ_{ja} and power consumption P with an offset of P_a, ambient temperature. Lowering ambient temperature below $-10°C$ requires expensive tool upgrades to enable the chiler to go down to such low temperature. In addition lowering T_a may be practical for steady state condition, but in the presence of power flutuations, it may undercool the device during low power portion of the test. Hence the focus has been on lowering thermal resistance. Thermal Interface Materials (TIM) have been shown to reduce the thermal resistance, and cosequently Tj by 30% [3]. In Fig. 3, T_a and θ_{ja} has been considered $0°C$ and $0.35°C/W$ respectively, to find the temperature tendency. In Equation 1, it can be seen that to limit junction temperature to T_{Jmax} we should limit θ_{ja} as follow:

$$\theta_{ja} < \frac{T_j - T_a}{P} \tag{5}$$

3 Time to Breakdown and Yield under Thermal Stress

The yield during the BI process is of critical importance. Therefore, BI parameters should be evaluated to have a constant predictable yield.

The logarithm of the time to breakdown t_{bd}, for gate oxide of a transistor, based on constant voltage test, has been shown to be [8]:

$$t_{bd} = \tau_o exp[\frac{G}{E_{ox}}] = \tau_o exp[\frac{GT_{ox}}{V_{ox}}] \tag{6}$$

where T_{ox} is the oxide thickness, V_{ox} is the voltage across the oxide, and G(350 MV/cm) and $\tau_o(1 \times 10^{-11}s)$ are the slope and intercept of the $\ln(t_{bd})$ versus $1/E_{ox}$ plot, respectively [8]. In this equation, τ_o and G are the only temperature dependent factors. These parameters, using Arrhenius equation form with activation energy, E_b, can be expressed as:

$$\tau_o(T) = \tau_o exp(\frac{-E_b}{k}[\frac{1}{T} - \frac{1}{300}])$$

$$G(T) = G(1 + \frac{\delta}{k}[\frac{1}{T} - \frac{1}{300}]) \quad \delta = \frac{k}{G}\frac{dG(T)}{d(1/T)} \tag{7}$$

where k is Boltzmann's constant, T is the absolute temperature, and τ_o and G are the room temperature constants given earlier. In the temperature range between $25°C$ and $150°C$, δ and E_b have been determined to be 0.0167 and 0.28 eV, respectively [9]. Fig. 4 shows temperature acceleration factor as a function of temperature.

Although the burn-in is related to the removal of infant mortalities, it may affect the yield of semiconductor devices. This is due to the fact that defects will grow during burn-in and some of them will cause yield loss. The amount of the defect growth and yield loss depends on burn-in environment, such as stressed voltage, stressed temperature and burn-in time.

In order to choose burn-in conditions which maximize the burn-in yield while improving the projected failure rate, the defect distribution models and their growth model should be studied. For the gate oxide defects in a transistor with a width of W, the growth model for defects are given as follows [10]:

$$W_b = W \times \nu, \quad 0 \leq \nu \leq 1 \tag{8}$$

$$W_g = W \times u, \quad 0 \leq u \leq 1 \tag{9}$$

where

$$\nu = \frac{t_b}{\tau_O(T_b)} exp[-\frac{G(T_b)T_{ox}}{V_b}]$$

$$u = \frac{t}{\tau_O(T_o)} exp[-\frac{G(T_o)T_{ox}}{V_o}]$$

W_b and W_g are defect growths in gate oxide during burn-in and operation, V_b and T_b are the burn-in voltage and temperature, and V_o and T_o are the operation voltage and temperature respectively. Temperature-dependent expressions for $\tau_O(T)$ and $G(T)$ are given in (7). It has been shown in [10] that the yield loss during burn-in will be:

$$Y_{loss} = Y - Y_l = Y(1 - Y^{\nu/(1-\nu)}) \tag{10}$$

where Y_l is the yield after burn-in and equals to $Y^{1/(1-\nu)}$.

In Fig. 5 we have shown the yield loss percentage for two given yield (0.9 and 0.99) before burn-in in $0.18\mu m$ technology for maximum voltage stress ($1.4 \times V_{dd}$). It can be seen that for a given pre-BI yield, the post-BI yield loss will increase exponentially with increasing temperature. Furthermore, the pre-BI yield will play an important role in post-BI yield loss. The lower the pre-BI yield is, the higher will be the post-BI yield loss.

4 Discussion

In Fig. 6 we illustrate the post-BI yield loss as a function of temperature, using Equation 10, for three technology generations ($0.18\mu m$, $0.13\mu m$, and $0.10\mu m$). In this simulation, voltage stress of $1.4 \times V_{dd}$ and 12 hours BI time are used. In Table 1, the electric field across the gate oxide for above mentioned technologies is calculated. It can be seen that with scaling, electric field across the gate oxide is increasing. Hence the yield loss is expected to increase. In order to compensate this, we need to bring down the burn-in temperature with each technology generation. In Fig.6, the horizontal line shows that to maintain a constant yield loss during the burn-in for three technology generation we need to bring the burn-in temperature by $10°C$.

Technology	V_{dd} (V)	T_{ox} ($A°$)	$1/E_{ox}$ (cm/V)
$0.18\mu m$	1.8 V	$30A°$	$11.90 \times 10^{-8} cm/V$
$0.13\mu m$	1.3 V	$20A°$	$11.80 \times 10^{-8} cm/V$
$0.10\mu m$	1.0 V	$15A°$	$11.70 \times 10^{-8} cm/V$

Table 1: $1/E_{ox}$ for different technologies.

5 Conclusion

In this work, post-BI Yield fallout is an impotant consideration, while setting the BI conditions. Under the burn-in conditions, the elevated leakage power may cause increased post Burn-in fallout. We have also shown that to maintain a constant post-BI yield loss, the burn-in temperature should go down by $10°C$ for each technology generation.

References

1. R.-P. Vollertsen, "Burn-In" Integrated Reliability Workshop Final Report, 1999. IEEE International , 1999, Page(s): 167 -173

2. A. Keshavarzi, R. Kaushik and C.F. Hawkins,

"Intrinsic Leakage in Low Power Deep Submicron CMOS ICs", IEEE International Test Conference, 1997, pp 146-155.
3. p. Tadayon, "Thermal Challenges During Microprocessor Testing" Intel Technology Journal Q3, 2000
4. International Technology Roadmap for Semiconductors (ITRS) 1999 Edition.
5. A. Keshavarzi, S. Narendra, C. Hawkins, K. Roys and V. De, "Technology Scaling Behaivior of Optimum Body bias for Standby Leakage power Reduction in CMOS ICs", 1999, ISLPED, pp 252-254.
6. F. Assaderaghi, "Dynamic Threshold-Voltage Mosfet (DTMOS) for Ultra-Low Voltage VLSI", IEEE Transactions On Electron Devices, Vol.44, No.3, March 1997.

7. F. Assaderaghi, "DTMOS: Its Derivatives and Variations, and Their Potential Applications", The 12th International Conference on Microelectronics, 2000.
8. R. Moazzami and C. Hu, "Projecting Gate Oxide Reliability and Optimizing Reliability Screens" IEEE Transactions on Electron Devices, VOL.37, NO 7, July 1990.
9. R. Moazzami, J. Lee, and C. Hu, "Temperature Acceleration of Time Dependent Dielectric Breakdown", IEEE Trans. Electron Device, Vol. 36, No. 11, pp. 2462, Nov. 1989.
10. T. Kim, W. Kuo,and W. K. Chien, "Burn-in Effect on Yield", IEEE Transactions on Electronics Packaging Manufacturing, Vol. 23, No. 4, Oct 2000.
11. L. Wei, Z. Chen, K. Roy, M. C. Johnson, Y. Ye, and V. K. De, "Design and Optimization of Dual-Threshold Circuits for Low-Voltage Low-Power Applications", IEEE Transaction (VLSI) Systems, Vol. 7, No. 1, March 1999, pp 16-24

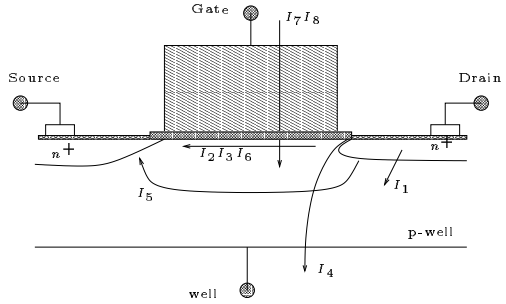

Figure 1: Summary of leakage current mechanisms of deep submicron transistors

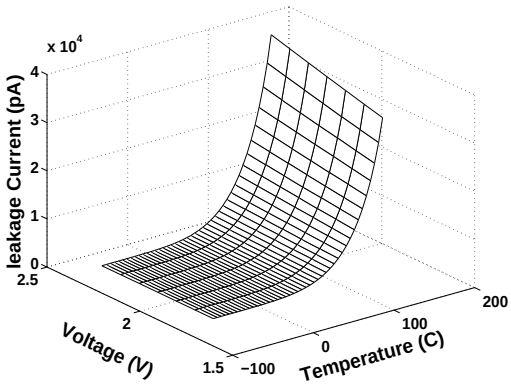

Figure 2: SPICE simulation of transistor leakage as a function of voltage and temperature in TSMC 0.18 μm technology

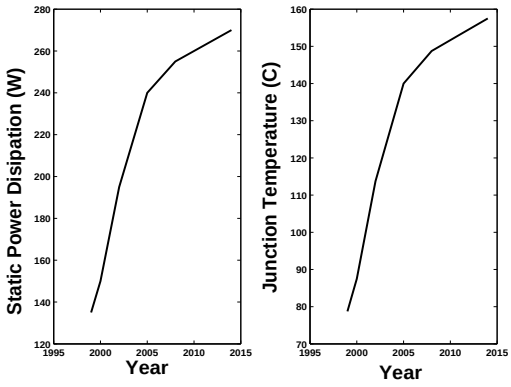

Figure 3: Static dissipated power and temperature projections [4].

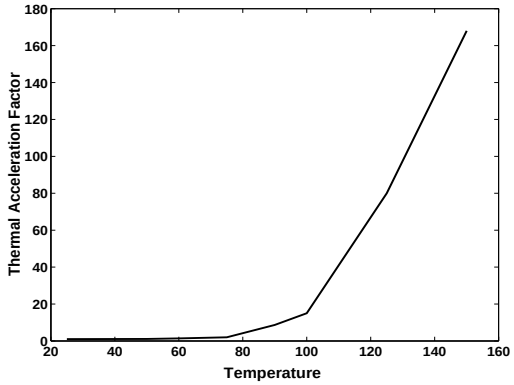

Figure 4: Thermal acceleration factor as a function of temperature.

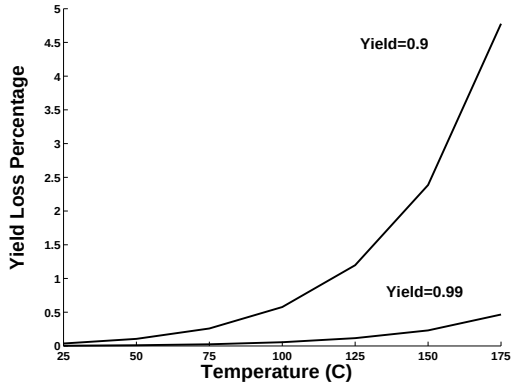

Figure 5: Post BI yield loss percentage vs. BI temperature for two pre-BI yields.

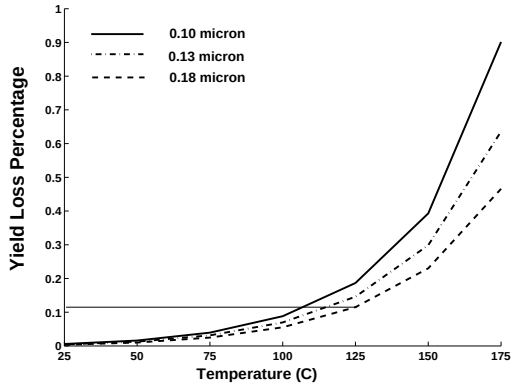

Figure 6: Hypothetical post BI yield loss percentage for different technology and pre-BI yield of 0.99.