Impact of Technology Scaling on Bridging Fault Modeling and Detection in CMOS Circuits

Oleg Semenov, Bhaskar Chatterjee, and Manoj Sachdev

Dept. of Electrical and Computer Engineering
University of Waterloo, Waterloo, Canada N2L 3G1
osemenov@vlsi.uwaterloo.ca, bhaskar@vlsi.uwaterloo.ca, msachdev@ece.uwaterloo.ca

ABSTRACT

Bridging faults are one of the most commonly observed failure mechanisms in contemporary integrated circuits (ICs). Several defects, such as gate oxide short, shorts between two different nodes may cause bridging faults (BF). BFs are known to cause intermediate logic levels and therefore are hard to detect by logic testing. In this article, we investigate the impact of technology scaling on BF detection. Theoretical analysis and HSPICE simulations carried out in four different technologies (0.18 µm, 0.25 µm, 0.35 µm, 0.8 µm) show that the detection of BFs is becoming increasingly harder with technology scaling. Fast and accurate calculations of the intermediate bridging voltages on the basis of BF model are presented. CMOS inverters were analyzed to find the impact of technology scaling on BF behavior. The results obtained with the developed model indicate close relationship with the results obtained by HSPICE simulations.

Keywords - CMOS integrated circuits, bridging faults, modeling, technology scaling, VLSI testing, defects

1. Introduction

Shrinking of device geometry have enabled realization of complex very large scale ICs (VLSI) at low costs. However, high packaging density results in increase of susceptibility of ICs to various manufacturing defects, such as gate oxide shorts and shorts between interconnect lines. These defects are commonly known as BF. Various researchers have reported BFs are being one of the dominant failure mechanisms in CMOS ICs [1-3]. Therefore, BFs cannot be modeled adequately with stuck-at fault (SAF) models and are difficult to detect using logic testing technique. In this article, we investigate the impact of technology scaling on BF detection, its modeling and present an analytical model for computing output voltage levels in CMOS circuits with BF. This paper is organized as follows: The short review of previous investigations is explained in section 2. Section 3 deals with the description of analyzed circuit. Analysis of transistor operating modes and the estimation of the impact of technology scaling on BF behavior in CMOS circuits are presented in sections 3.1 and 4. Detailed description of BF model for submicron CMOS ICs is presented in section 3.1 also. Finally, future work trends and conclusion are drawn in section 5.

2. Review and Motivation

BF detection methods can broadly be classified into the current monitoring and logic testing methods. The current monitoring method (I_{DDQ} method) had been effective in detecting BF in CMOS technologies [4]. However, owing to technology scaling the increased number of transistors and sub-threshold leakage make it difficult to detect BFs in deep sub-micron VLSIs. Several researchers predicted defect and defect-free currents for scaled devices will have similar distribution [5,6].

Voltage testing is still the predominant test methodology. Studies show that low resistive BFs can be detected by logic testing if voltage at a node affected by BF is close to the faulty voltage level. Ferguson and Shen [1] extracted and simulated CMOS defects using IFA techniques. SAF model performed rather poorly in modeling extracted BF, only 73% - 89% BFs were detected by SA based test patterns. On the other hand the fault coverage of extracted BF by exhaustive test set was relatively high. In an another study Storey and Maly [4] demonstrated similar results. The SAF testing could detect only 80% of the BF in an 8:1 multiplexer. However, I_{DDQ} could detect all the bridging faults.

Resistance of BF plays a significant role in its detection. As the resistance of a BF increases, its detection becomes more difficult. Vierhaus et. al. [7] investigated the impact of defect resistance on CMOS combinational logic. Their analysis resulted in similar conclusions. For high resistance bridging faults, voltage testing was inadequate and delay fault testing gave improved coverage. However, authors concluded that zero defect testing is impossible without I_{DDQ} testing. Maiuri and Moore [3] extended this work by including impact of technology scaling on BF detection. They analyzed BFs in three different technologies. The results of their analysis show that with the scaling of technology the range of defect resistance for which defects are not detected is increasing.

Several researchers investigated test pattern generation techniques for BFs [8,9]. Chess and Larabee [8] described a system for simulating and generating tests for BFs. Their system could detect at least 98.32% of BFs

in ISCAS-85 combinational benchmark circuits. In this study authors assume the resistance of BFs to be low. Recently, Lee et al. [9] further investigated test pattern generation technique for BFs. An automatic test pattern generation (ATPG) algorithm developed for faults that are logic testable. A built-in intermediate voltage sensor (BIVs) was embedded on-chip for BFs that generate intermediate voltages.

Randomly placed bridging faults are a serious problem in CMOS processes. As technology advances to smaller geometry, more metal layers, reduced design margins and higher frequencies, the effects of these defects will grow in complexity, increasing the variety of BF behavior that we need to detect. The motivation of this paper is to assess the impact of technology scaling on bridging fault detection. Theoretical analysis and HSPICE (BSIM3v3 MOSFET models, level 49) simulations carried out in four different technologies (0.18 µm, 0.25 µm, 0.35 µm, 0.8 µm) show that the detection of BFs is becoming increasingly harder with technology scaling. Fast and accurate calculations of the intermediate bridging voltages on the basis of BF model are presented.

3. Analyzed Circuit

Electrical effects of a resistive short located between two CMOS inverters (Figure 1) were analyzed. The modeling and simulations of BF was done under DC conditions. Inputs of two inverters are kept at logic levels "0" and "1" respectively.

The voltages at intermediate nodes are calculated as a function of BF resistances. We used three different technologies from Canadian Microelectronic Corporation (CMC) technology files. Transistor parameters for different technologies are listed in Table 1. These values are used for the intermediate bridging voltage calculations. Device parameters for 0.8 µm CMOS technology are used from [9].

3.1 Transistor Operating Modes

In Figure 1 let us assume that $V_{in1} = 0V$ and $V_{in2} =$ Vdd and BF resistance is sufficiently large. In this case the transistors N1 and P2 are in cut off mode and we have $I_{p1} \approx I_{n2} \approx I_{Rsh}$, where I_{p1} is the source-drain current of transistor P1 and I_{n2} is the drain-source current of transistor N2. Conversely, if $V_{in1} = Vdd$ and $V_{in2} = 0$ V, the transistors N2 and P1 are in cut off mode.

Theoretically, P1 and N2 transistors can have four possible operating modes:
- P1 saturation and N2 saturation;
- P1 linear and N2 saturation;
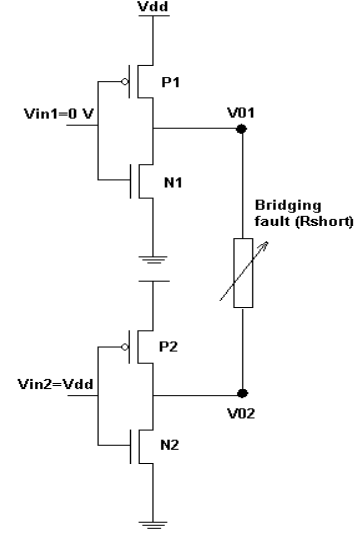- P1 saturation and N2 linear;
- P1 linear and N2 linear.

Figure 1. Circuit for bridging fault analysis

For transistor P1 to be in saturation the following condition should be valid:
$|V_{01} - V_{dd}| > |V_{in1} - V_{dd}| - |V_{tp}|$.
If transistor P1 is in the linear region then $V_{01} > |V_{tp}|$. Similarly, we can describe operating modes for N2. For example, transistor N2 in saturation mode if $V_{02} - 0 > V_{dd} - V_{tn}$ and it is in linear mode if $V_{02} < V_{dd} - V_{tn}$. The calculated voltage ranges for each operating mode and four different CMOS technologies are shown in Table 2. In order to calculate the voltages at V_{01} and V_{02} nodes, we describe the MOSFET DC model. At this stage we consider the long channel model (the SPICE MOS Level 1 model). The first order model is based upon following assumptions [10]:

i) Gradual channel approximation is valid

ii) Hole current can be neglected (for n-MOS)

iii) Recombination and generation are neglected

iv) Electrons flow (for n-MOS) along the length of the channel only

v) Carrier mobility μ in the inversion layer is constant along the length of the channel

vi) Electron flow (for n-MOS) is due to drift only (diffusion current is neglected)

vii) Bulk charge Q is constant at any point along the length of the channel.

The following equations describe the drain current of the transistor for different operating regions:

1) cut-off region: ($V_{gs} \leq V_{th}$), $I_{ds} = 0$;

2) linear region: ($V_{gs} > V_{th,}$ $V_{gs} \leq V_{dsat}$),

Parameter	0.8-μm technology	0.35-μm technology	0.25-μm technology	0.18-μm technology
V_{dd}, V	5	3.3	2.5	1.8
V_{tn}, V	0.75	0.56	0.42	0.47
V_{tp}, V	-0.9	-0.75	-0.6	-0.44
K_n, (μA/V^2)	101.05	148.3	212	224
K_p, (μA/V^2)	32.71	54.5	60	69.4

Table 1. Transistor parameters for different CMOS technologies

0.8 μm CMOS technology, [9]		0.35 μm CMOS technology		0.25 μm CMOS technology		0.18 μm CMOS technology	
P1 (V_{01})	N2 (V_{02})	P1 (V_{01})	N2 (V_{02})	P1 (V_{01})	N2 (V_{02})	P1 (V_{01})	N2 (V_{02})
Saturation (< 0.9 V)	Saturation (> 4.25 V)	Saturation (< 0.75 V)	Saturation (> 2.74 V)	Saturation (< 0.6 V)	Saturation (> 2.08 V)	Saturation < 0.44 V	Saturation > 1.33 V
Linear (> 0.9 V)	Saturation (> 4.25 V)	Linear (> 0.75 V)	Saturation (> 2.74 V)	Linear (> 0.6 V)	Saturation (> 2.08 V)	Linear > 0.44 V	Saturation > 1.33 V
Saturation (< 0.9 V)	Linear (< 4.25 V)	Saturation (< 0.75 V)	Linear (< 2.74 V)	Saturation (< 0.6 V)	Linear (< 2.08 V)	Saturation < 0.44 V	Linear < 1.33 V
Linear (> 0.9 V)	Linear (< 4.25 V)	Linear (> 0.75 V)	Linear (< 2.74 V)	Linear (> 0.6 V)	Linear (< 2.08 V)	Linear > 0.44 V	Linear < 1.33 V

Table 2. Transistor operation conditions for different CMOS technologies

$$I_{ds} = \beta\,(V_{gs} - V_{th} - 0.5\,V_{ds})\,V_{ds}; \qquad (1)$$

3) saturation region: $(V_{gs} > V_{th}, V_{gs} > V_{dsat})$,

$$I_{ds} = \beta/2\,(V_{gs} - V_{th})^2\,(1 + \lambda V_{ds}), \qquad (2)$$

where λ is the channel length modulation parameter and β is the gain factor, which is defined as $\beta = K^* (W/L)$ and $K = \mu\,C_{ox}$ is the process transconductance parameter (see Table 1 for values of this parameter for different technologies). Typically, λ values between 0.05 - 0.001 V^{-1} [10]. Table 1 has K_n and K_p for different CMOS technologies.

The data in Table 2 can be analyzed to simplify the analysis for a given technology. For example, certain operating modes are impossible and some other modes are unlikely. The impossible mode is shaded dark while unlikely modes are shaded lightly in Table 2.

1. P1 Saturation and N2 Saturation case
This mode requires $V_{01} > V_{02}$. For 0.18-μm technology, $V_{01} < 0.44$ V (V_{tn}) and $V_{02} > 1.33$ V ($V_{dd} - V_{tn}$). This condition contradicts the $V_{01} > V_{02}$ condition hence it is not possible.

2. P1 Linear and N2 Saturation case
Using the condition $I_{p1} \approx I_{n2} \approx I_{Rsh}$ and equations for the drain current of transistor for these operating regions (Eq. 1 and Eq. 2), we have Eq. 3 and Eq. 4. Dividing Eq. 3 by Eq. 4 and substituting specific parameters for 0.8 μm CMOS technology in [9] has obtained the Eq. 5 and Eq 6. In the Eq. 6, W_{p1} and L_{p1} are channel width and length for P1 transistor; W_{n2} and L_{n2} are channel width and length for N2 transistor. A transistor size ratio of p-MOS to n-MOS of an inverter more than 9.99 is seldom used for most logic circuits, hence this condition is very unlikely.

3. P1 Saturation and N2 Linear case

A similar technique may be used for P1 Saturation - N2 Linear transistor mode. From Table 2 for 0.8 μm CMOS technology it follows that $V_{01} < 0.9$V and $V_{02} < 4.25$V. Using a similar derivation to the previous case in [9] was obtained Eq. 7 and Eq. 8. Typically, the ratio of transistor sizes in digital CMOS circuits lies between 2 and 3 for equal noise margin or balanced rise/fall times.

4. P1 Linear and N2 Linear case

Because $I_{p1} \approx I_{n2} \approx I_{Rsh}$, the voltage drop across the R_{sh} is described by two equations (see Eq. 9). Since both equations are nonlinear, the general approach to solving this kind of problem is by iteration, i.e. first guessing a solution and then successively refining it. The method of approximated solution of this case is described in [9] for 0.8-μm technology and we used it for other technologies. Dimensions of transistors, which were used for the BF modeling and simulation in HSPICE, are shown in Table 3 and required transistor parameters are shown in Table 1.

CMOS technology	Size of n-MOS transistor, $Z_n = (W/L)$	Size of p-MOS transistor, $Z_p = (W/L)$	Ratio coefficient: $Z = Z_p/Z_n$
0.8 μm [9]	2 μm/1 μm = 2	4 μm/1 μm = 4	2.0
0.35 μm	0.8μm/0.35 μm = 2.29	1.96μm/0.35μm = 5.6	2.44
0.25 μm	0.8 μm/0.25 μm = 3.2	1.64 μm/0.25 μm = 6.56	2.05
0.18 μm	0.58 μm/0.18 μm = 3.2	1.5 μm/0.18 μm = 8.3	2.6

Table 3. Transistor dimensions used for the BF simulation and modeling

$$V_{01} - V_{02} = R_{short} \cdot K_p \frac{W_{p1}}{L_{p1}} \left\{ \left(\left| V_{in1} - V_{dd} \right| - \left| V_{tp} \right| \right) \left(\left| V_{01} - V_{dd} \right| \right) - \frac{\left| V_{01} - V_{dd} \right|^2}{2} \right\} \tag{3}$$

and

$$V_{01} - V_{02} = R_{short} \cdot \left\{ \frac{K_n}{2} \frac{W_{n2}}{L_{n2}} (V_{in2} - V_{tn})^2 \right\} \tag{4}$$

$$V_{01} = 0.9 + \sqrt{\frac{16.8 - 55.8 W_{n2}}{L_{n2} \frac{L_{p1}}{W_{p1}}}} > 4.25V \tag{5}$$

$$\frac{W_{p1}/L_{p1}}{W_{n2}/L_{n2}} > 9.99 \tag{6}$$

$$V_{02} = 4.25 - \sqrt{18.06 - 5.44 \frac{W_{p1}}{L_{p1}} \frac{L_{n2}}{W_{n2}}} < 0.9 \tag{7}$$

$$\frac{W_{p1}/L_{p1}}{W_{n2}/L_{n2}} < 1.26 \tag{8}$$

$$V_{01} - V_{02} = R_{sh} K_p \frac{W_{p1}}{L_{p1}} \left\{ \left(\left| V_{in1} - V_{dd} \right| - \left| V_{tp} \right| \right) (V_{dd} - V_{01}) - \frac{(V_{dd} - V_{01})^2}{2} \right\}$$

and

$$V_{01} - V_{02} = R_{sh} \left\{ K_n \frac{W_{n1}}{L_{n1}} \left[(V_{in1} - V_{tn}) V_{02} - \frac{V_{02}^2}{2} \right] \right\} \tag{9}$$

The following results were cited in [9] for 0.8-μm technology:

$$\begin{cases} V_{01} = [4.51 R_{short} + 6133] / [3027 + R_{short}] \\ \\ V_{02} = 3.29 - 0.62 V_{01} \end{cases} \tag{10}$$

Using a similar approach the following expressions were obtained for 0.35-, 0.25- and 0.18- μm technologies:
For 0.35-μm technology:

$$\begin{cases} V_{01} = [3.24 R_{short} + 5000] / [3761 + R_{short}] \\ \\ V_{02} = 2.15 - 0.63 V_{01} \end{cases} \tag{11}$$

For 0.25-μm technology:

$$\begin{cases} V_{01} = [2.24 R_{short} + 604.7] / [720.7 + R_{short}] \\ \\ V_{02} = 1.2 - 0.43 V_{01} \end{cases} \tag{12}$$

For 0.18-μm technology:

$$\begin{cases} V_{01} = [1.57 R_{short} + 675] / [955.3 + R_{short}] \\ \\ V_{02} = 1.09 - 0.54 V_{01} \end{cases} \tag{13}$$

These equations were used to calculate intermediate bridging voltages V_{01} and V_{02} for a BF between two inverters.

HSPICE simulations of analyzed circuit for 0.35 μm, 0.25 μm and 0.18 μm CMOS technologies show that P1 and N2 transistors are operating in Linear - Linear modes over a wide range of transistor sizes (Eq. 14), which

$$1 \le \frac{W_{p1}/L_{p1}}{W_{n2}/L_{n2}} \le 10 \tag{14}$$

cover all practical MOSFETs applications in digital circuits. R_{short} was equal to 100 kOhm for circuit simulations to emulating the defect free case.

4. Impact of Technology Scaling on BF Behavior in CMOS Circuits

As technology scales, several short channel effects influence the drain current. Four parameters in the long channel model following are affected by the technology scaling (see Table 1, where $K = \mu C_{ox}$). These parameters are:

i) Carrier mobility μ in the channel

ii) Gate oxide capacitance (C_{ox})

iii) Supply voltage (V_{dd})

iv) Threshold voltage (V_{th})

In accordance with the equations for V_{01} and V_{02} (section 3.1) for different CMOS technologies, voltages at nodes V_{01} and V_{02} were plotted for various values of bridging resistance R_{sh}. These results were compared with the simulated results in HSPICE. Figure 2(a) and (b) illustrate the comparison of calculated as well as HSPICE simulated results. The average error between simulated results and that of the model was found to be 16%.

In our investigation we assumed that the critical value of BF resistance (R_{crit}) corresponds to R_{sh} that result in degradation of nominal logic levels by ($V_{tn} + |V_{tp}|$), (i.e. approximately 40% of V_{dd} for different technologies). This ensures that transistors are operate in linear mode

(the proposed BF model is valid), and degraded logic levels are located close to the middle of the "linear - linear" interval. It has been shown that the threshold voltage of different logic gates (INV and 1 to 6 input NAND, NOR, XOR, XNOR) is located in interval [V_{dd} - 40%; 0 V + 40%] [9].

The other criterion, which we used in our investigation for interpretation of BF impact on logic levels, is $R_{10\%}$ value. When BF value corresponds to $R_{10\%}$, the nominal logic levels are degraded by 10%. Typically, the degradation of logic levels less then 10% is not identified as the logic error [11].

The dependence of critical resistance (R_{crit}) on analyzed technologies is plotted in Figure 3. It is apparent from the figure that the critical resistance is reducing for each successive technology generation. Therefore, the range in which the bridging defect is robustly detected (0 - R_{crit}) is also reducing. In other words, bridging defect detection is becoming increasingly difficult with technology scaling.

The data from Figure 2 (a) and (b) are normalized in order to see the impact of technology scaling on voltages of nodes V_{01} and V_{02}. These, normalized node voltages are plotted as a function of BF resistance in Figure 4. Normalized plots were obtained for each technology for both V_{01} and V_{02} curves in the following manner. For V_{01}, the data points were divided by the Vdd of the corresponding technology, while for V_{02}, each point was divided by the voltage when R_{sh} is 0 Ohms. Thus the normalized plots for V_{02} for different technologies converge at 1 when R_{sh} is 0 Ohms. This plot allows comparison of the results obtained for different technologies and illustrates the general trends of V_{01} and V_{02} variation with bridging fault resistance.

Following conclusions can be drawn from Figure 4 using the analytical model:
1. For bridging resistances less than R_{crit}
(<~850 Ohms for 0.18 - μm technology; <~1030 Ohms for 0.25 - μm technology; <~1950 Ohms for 0.35 - μm technology; <~2750 Ohms for 0.8 - μm technology) BF may be detected by voltage testing methods. This is because the nominal voltage levels are significantly degraded and result in erroneous logic operation.
2. When the bridging resistance is between R_{crit} and $R_{10\%}$, the BF cannot be detected by voltage testing method (voltage levels in undefined range):

~ 850 Ohms ≤ R_{BF} ≤ ~ 3000 Ohms for 0.18 - μm technology;
~ 1030 Ohms ≤ R_{BF} ≤ ~ 3000 Ohms for 0.25 - μm technology;
~ 1950 Ohms ≤ R_{BF} ≤ ~ 5500 Ohms for 0.35 - μm technology;
~ 2750 Ohms ≤ R_{BF} ≤ ~ 5500 Ohms for 0.8 - μm technology.

3. For bridging resistance values grater then $R_{10\%}$ (~ 3000 Ohms for 0.18 - and 0.25 - μm technologies; ~ 5500 Ohms for 0.35 - and 0.8 - μm technologies), the output logic levels are not distorted, but the noise immunity is degraded near the above mentioned resistance values.

Note that the interval of BF resistance values, which can be tested by voltage test method, is reduced under technology scaling.

5. Future Work and Conclusion

As CMOS technologies scale down, background leakage increases inexorably, primarily due to device subthreshold leakage. As a result, even for 0.25 - μm technology, conventional pass/fail I_{DDQ} testing may no
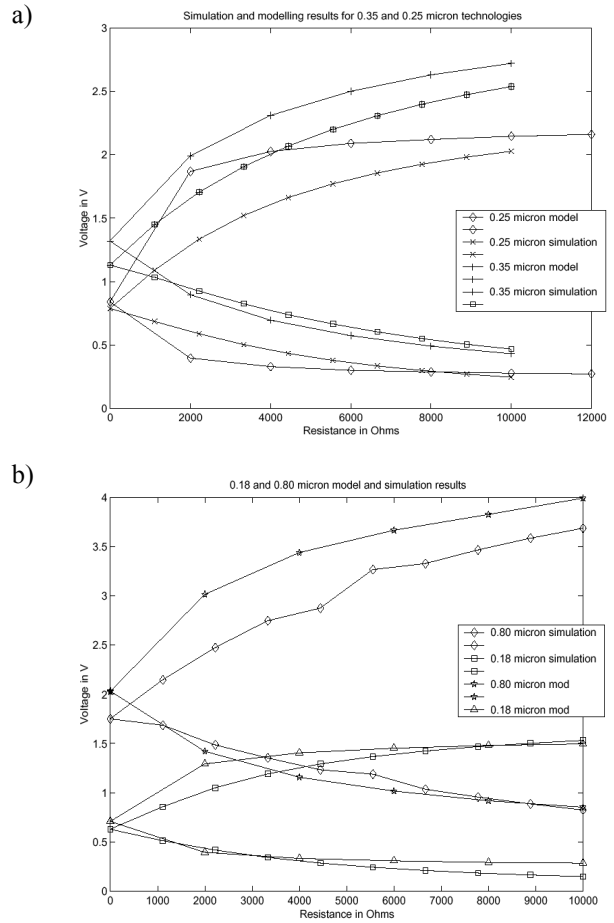
a)

b)

Figure 2. Output voltage levels (V_{01} and V_{02}) vs. bridging resistance (the applied model and HSPICE simulations): (a) - 0.25- and 0.35 - μm technology; (b) - 0.8- and 0.18- μm technology

longer be practical [2]. Thus for advanced CMOS technologies we should combine current and logic test methods for the best coverage and identification of

defects. From this point of view, the voltage modeling of BFs for deep submicron technologies may predict the perspectives of logic testing in the future.
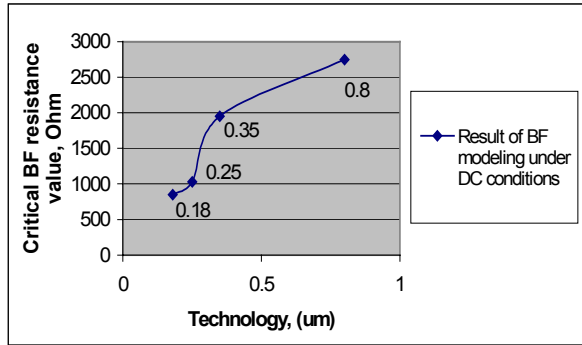

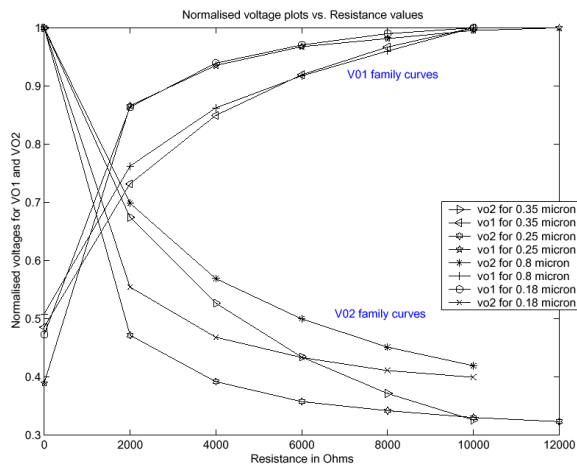*Figure 3. Critical BF resistance values vs. CMOS Technologies*

Figure 4. Normalized voltage plots vs. BF resistance values (V_{01} and V_{02} voltages for different technologies)

In future, we are planning to consider the following aspects of BF modeling:

- use accurate short-channel model of MOSFETs transistors for more accurate of BF modeling;

- estimate efficiency of I_{DDQ} testing in "undefined range" of BF resistance values, where logic testing cannot be used, for different CMOS technologies;

- develop BF model for more complicated CMOS gates.

In this paper we have analyzed the impact of CMOS scaling on BF modeling and arrive at the following conclusion:

- under technology scaling accurate BF models should include short-channel effects of MOSFETs. The range of intermediate voltages, which can be interpreted as a 0 by one gate and as a 1 by another, will be increased;

- R_{crit} value is reduced with technology scaling;

- the undefined range of R_{BF}, in which BF cannot be detected by voltage testing is increased under technology scaling. The possible solution of submicron CMOS IC testing is the "Test Mix" technique [12], combining I_{DDQ} and voltage test methods, which allow to increase the coverage of detected BFs in submicron CMOS technologies.

The error of applied BF model on the basis on long channel MOSFETs model was 16% in comparison with HSPICE simulations.

Acknowledgments

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