Contribution of Gate Induced Drain Leakage to Overall Leakage and Yield Loss in Digital submicron VLSI Circuits

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ABSTRACT

In this paper, the impact of gate induced drain leakage (GIDL) on overall leakage of submicron VLSI circuits is studied. GIDL constitutes a serious constraint, with regards to off-state current, in scaled down CMOS devices for DRAM and/or EEPROM applications. Our research shows that the GIDL current is also a serious problem in scaled CMOS digital VLSI circuits. We present the experimental and simulation data of GIDL current as a function of 0.35 - µm CMOS technology parameters and layout of CMOS standard cells. The obtained results show that a poorly designed standard cell library for VLSI application may result in extremely high leakage current and poor yield.

Keywords - band-to-band tunneling, gate-induced leakage current, LOCOS isolation, CMOS ICs reliability, standard logic cell layout

I. Introduction

The leakage in the drain region is a crucial issue for scaling of the MOSFET towards the deep submicron regime. The reasons are (i) the subthreshold conduction increases exponentially due to the threshold voltage reduction; (ii) the surface band-to-band tunneling (BTBT) or gate-induced drain leakage (GIDL) increases exponentially due to the reduced gate oxide thickness; and (iii) the bulk BTBT increases exponentially due to the increased doping concentrations in bulk and well.

GIDL current is one of the major contributors to the overall MOSFET leakage. GIDL is induced by band-to-band tunneling effect in strong accumulation mode and generated in the gate-to-drain overlap region. This leakage current component has been observed in DRAM trench transistor cells and in EEPROM memory cells and is identified as the main leakage mechanism of discharging the storage nodes in sub-micron dynamic logic [1-3]. This paper presents test results of abnormally high leakage current (~0.1 - 1 mA) observed in a digital ASIC. Our investigations show that the leakage current is caused by band-to-band tunneling in drain-LOCOS isolation overlap regions.

This paper is organized as follows: The description of an analyzed video-broadcasting chip and results of current tests are given in section 2. Section 3 deals with the impact of 0.35 - µm CMOS processing parameters variation on a GIDL current. The reasons of leakage current at LOCOS isolation edge are discussed in section 4. Section 5 is devoted to analysis of testig and simulation data. Finally, conclusions are presented in section 7.

II. Leakage Current Test of Device under Test (DUT)

In this paper, we analyze the reasons of abnormally high leakage current observed during the characterization of a digital chip implemented in a standard 0.35 - µm CMOS process. The general information about DUT is given in Table 1.

Logic blocks in the DUT are tested with full scan methodology. Logic testing is implemented on the automated test equipment (ATE) HP83000 F660 (1.3 GHz Data Rate) and has stuck-at fault coverage approximately 95%. Devices, that are successfully passed logic testing, are then tested for the leakage current.

Table1. General information of Device under Test.

Die size	6.0 mm x 6.0 mm
Maximum probe pins (including all V_{dd} and Gnd)	128
Nominal V_{dd}, V	3.3
Clock Input Frequency, MHz	80
Technology	Double well 0.35 - µm CMOS, 4 level metal.
Approximated transistors number	500, 000
Product type & description	Digital & Video

The current testing results show a strong dependence of the leakage current on the accuracy of poly-silicon lines alignment to the diffusion edge or LOCOS bird's beak. The leakage current distribution exhibits a strong dependence with respect to the poly-silicon mask bias. The detailed description of mask bias technique in submicron optical lithography is presented in [4]. Figure 1 illustrates distribution of I_{DDQ} current without any poly bias (Figure 1(a)) and with –0.02 µm poly bias (Figure 1(b)). The leakage current is reduced more than 10 times as the spacing between poly-LOCOS edge is increased. The average leakage current of this chip is found to be 0.1 – 1 mA range, which is approximately 100 times larger than the expected value.

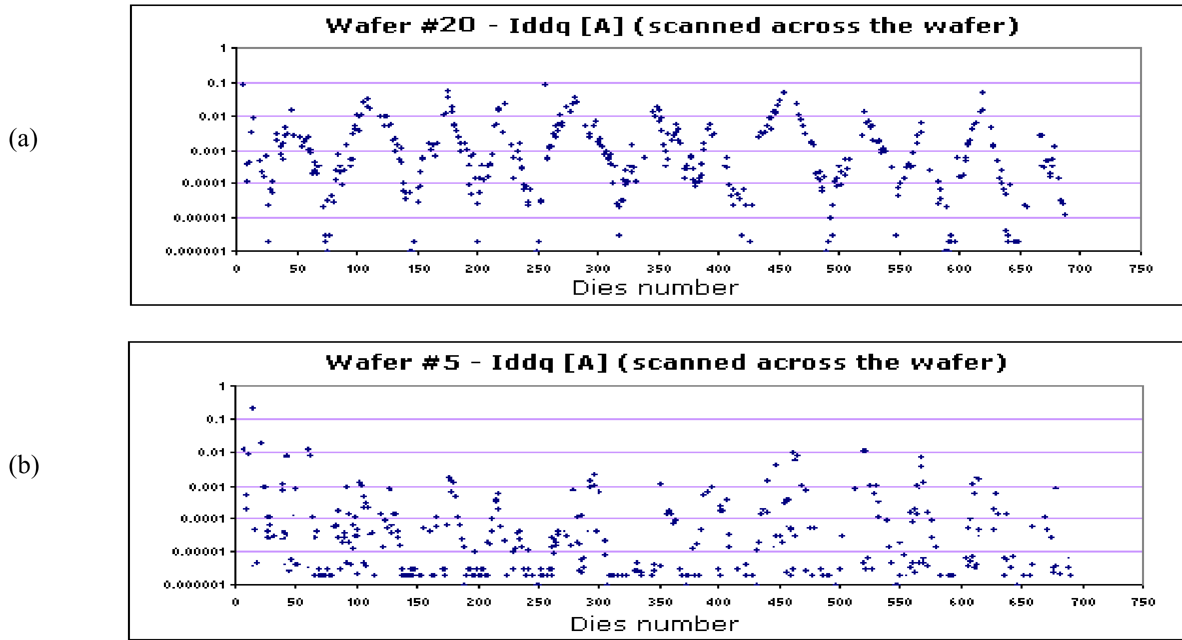

Fig. 1. I_{ddq} testing results at nominal poly-mask bias (a) and after poly silicon mask bias on -0.02 μm (b).

In order to do the root cause analysis of the fault, photon-emission microscopy (PEM) is applied on the analyzed samples. PEM measures the photons emitted when transistors are improperly saturated or when defect sites are passing current. Analysis of hot spots allows us to find standard cells that may have abnormally high leakage current. The typical design of these cells is shown in Figure 2. In this figure, black lines indicate possible leakage current locations. These are the overlap regions of poly-silicon lines and diffusion regions that are formed as a result of lateral diffusion. It was found that 30% of logic cells had large overlap regions. The total number of cells in a chip is 89304.

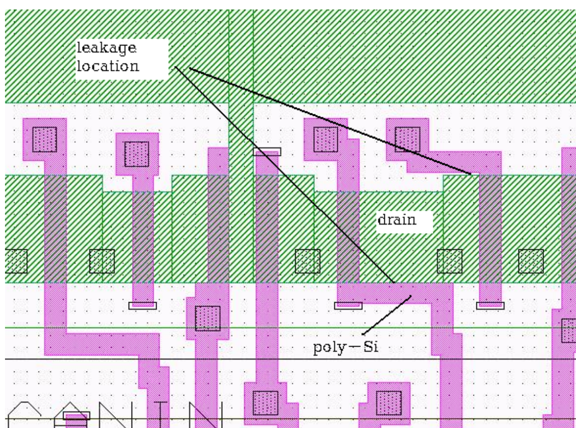

Fig. 2. Section of standard flip-flop cell layout.

III. Impact of Technology Parameters on GIDL: Simulation Results

The random variability of the parameters of the semiconductor fabrication process is reflected in the corresponding stochastic spread of circuit performance. This is due to the fact that the fabrication equipment, materials, and control variables cannot be controlled with infinite precision, but only within given tolerances. The effect of equipment, material drift, fluctuations, and process non-uniformity introduces 1) spatial and temporal variations of the electrical device parameters; and 2) increases power consumption per chip.

A. Lateral diffusion in source/drain regions

The serious problems of submicron CMOS technology are the fluctuations in the location of dopant atoms in the device active regions and the lateral diffusion of doping impurity in gate-to-source and gate-to-drain overlap regions. These effects reduce the threshold voltage and induce drain current fluctuations. The lateral diffusion distance of boron for the MOSFET source/drain has been investigated in [5]. It was founded that the lateral diffusion distance at the p-n junction is about 0.6 times the vertical distance for the 80 - 100 nm junctions. This result we used in the GIDL current simulation.

B. Band-to-band tunneling leakage current in gate-to-drain overlap region

GIDL current is one of the dominant reasons of submicron CMOS circuits degradation. Thus we attempt to estimate the GIDL current value as the function of gate-to-drain overlap width. These simulations are done in Microtec device simulator [6]. Technology parameters of the n-MOSFET that is used for simulations are given in Table 2.

The cross-section of the analyzed transistor is shown in Figure 3. In our research, we assume that the operating temperature is room temperature. In result of simulations, the distribution of vertical and lateral electric fields as a function of Gate-to-Drain Overlap (L_x) is obtained.

Table 2. N-MOSFET Simulation Parameters.

Parameter	Value	Unit
Substrate doping	5×10^{15} (p -type)	cm^{-3}
Source/Drain doping	1×10^{20} (n -type)	cm^{-3}
V_{th} adjusted doping	1.6×10^{18} (p-type)	cm^{-3}
Punch-through doping	2×10^{17} (p-type)	cm^{-3}
L_{eff}/W:	0.32/5	µm/µm
Gate oxide thickness	65	Å

The simulations are done for L_x = -100 nm, -50 nm, 0 nm, 50 nm, 100 nm and 150 nm. The distribution of the maximum electric field as a function of Gate-Drain overlap is shown in Figure 4. The value of maximum electric field (E_s) in the depletion layer of gate-to-drain overlap region is estimated as 9.1×10^5 V/cm from simulations.

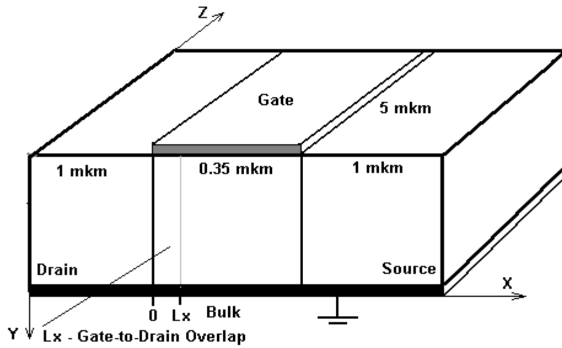

Fig. 3. Cross-section of analyzed n-MOSFET.

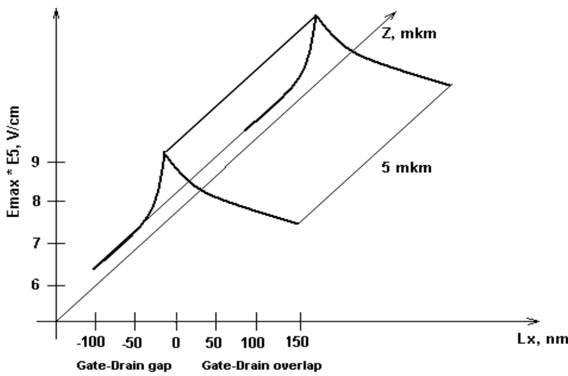

Fig. 4. 2-D electric field distribution in L_x - Z plane.

The tunneling leakage current is calculated using simple 1-D band-to-band tunneling current model [7]

$$I_{gidl} = A \cdot E_s \exp(-B / E_s) \quad (1)$$

Where physical constants are A=2.06 x 10^{-6} [A x cm/V] and B=21.3 MV/cm. Constant A was extracted from the experimental plot I_{gidl} vs. V_{gd} for submicron MOSFET and V_{dg} = 4 V [8]. The calculation of the band-to-band tunneled leakage current by Eq. (1) gives the result of $I_{gidl} = 1.29 \times 10^{-10}$ A/ μm^2 for the analyzed n-MOSFET. The effective area of tunneled leakage current (S) is W x L_x, where W is the channel width and L_x is the gate-to-drain overlap length. In our case, W is 5 µm and L_x is 72 nm [5]. Thus the effective area of tunneled leakage current is 0.36 μm^2. Therefore, the total band-to-band tunneling leakage current is 4.6×10^{-11} A. Note that the nominal total leakage current of the MOSFET for 0.35 - µm CMOS technology is 10 pA/µm. Thus the analyzed MOSFET should has 50 pA of the leakage current. It means that lateral diffusion of source/drain regions and tunneling effect may double the nominal leakage current.

IV. Leakage current at LOCOS isolation edge

As the packing density of integrated circuits increases, the peripheral LOCOS length surrounding the active region per unit area becomes longer. As a consequence, the leakage at the LOCOS-active area interface becomes an issue. The leakage phenomenon at the local oxidation of silicon (LOCOS) isolation edge, caused by the recombination and generation process [9]. This leakage is further enhanced by proximity of poly-silicon line. Adler et. al. [1] suggested that the poly-silicon line should have finite spacing from this interface (Figure 5).

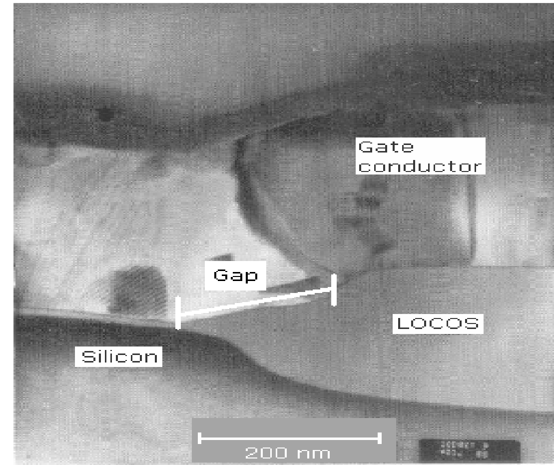

Fig. 5. TEM cross-section of LOCOS isolation in 4-Mb DRAM [1].

In order to estimate the GIDL leakage, erroneous layout conditions were recreated in Microtec device simulator [6]. A pseudo LOCOS structure is created using a n-MOS transistor (W/L = 5/0.35 µm) with varying gate oxide thickness. The variable gate oxide thickness mimicked the bird's beak phenomena and gate-to-drain overlap area mimicked the lateral diffusion of active region in LOCOS-active area interface. Note that the LOCOS bird's beak region has a large density of electrically active defects (N_{ss}). C-V measurements show that the typical N_{ss} value is 1×10^{12} cm^{-2}

eV^{-1} [10]. The trapped positive charge is one of the main reasons of leakage current at the field oxide edge. This value is used for pseudo LOCOS structure simulations. Simulation results are shown in Figure 6. This figure illustrates drain current (I_d) as a function of drain voltage (V_d) while $V_g = 0$ V (gate voltage). Here I_d actually represents the GIDL leakage, V_d represents the voltage at the active area of the interface and V_g is the voltage at the poly-silicon line. As it is apparent from this graph, the GIDL current is a strong function of LOCOS oxide thickness and it reduces as the poly to LOCOS-active area interface spacing is increased.

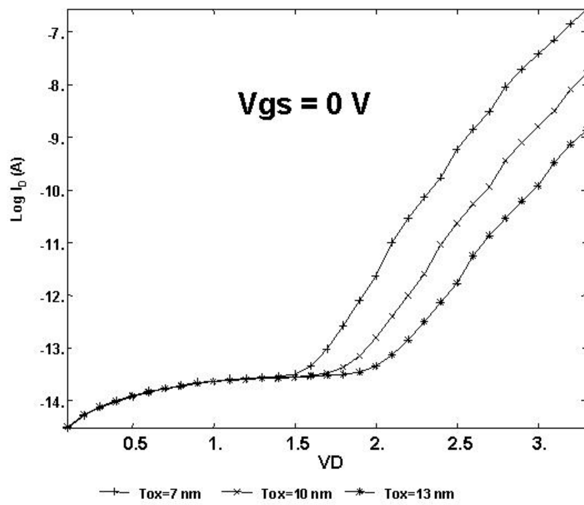

Fig. 6. GIDL leakage current in pseudo-LOCOS structure (Nss = 1E12 $cm^{-2}eV^{-1}$).

V. Analysis of Testing and Simulation Data

Strong dependence of the leakage current on bias of poly-silicon line or layer to layer alignment (Figures 1) shows indirectly that the possible reason of the leakage current, is the GIDL current at the LOCOS edge. The measured average leakage current of the chip is 1 mA or ~4 x 10^{-9} A/transistor. The simulation of GIDL current at the LOCOS edge gives the leakage current close to this value. This fact shows that the GIDL is the possible reason of observed abnormally high leakage current. To check this assumption, the temperature dependency of leakage current is measured. The current measurement setup is shown in Figure 7.

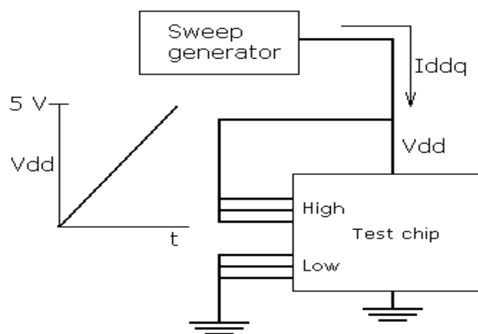

Fig. 7. Setup of leakage current measurement.

With the device properly initialized and with its signal-input pins set to appropriate logic states, V_{dd} is varied while I_{ddq} is measured. All inputs of the analyzed chip were grounded in this experiment. The obtained results are shown in Figure 8. Note that the breakdown voltage is reduced as temperature increases. This fact may have the following explanation. Since the band-gap energy (E_g) in silicon decreases with increasing temperature, the breakdown voltage due to tunneling effect has a negative temperature coefficient; that is, the breakdown voltage decreases with increasing temperature [11].

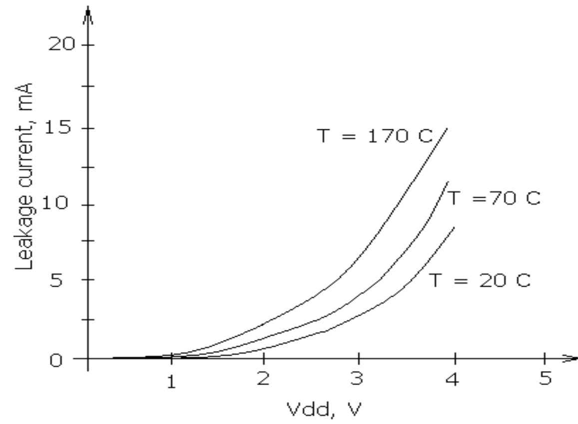

Fig. 8. Leakage current of the test chip as unction of V_{dd} and temperature.

The obtained results confirm the band-to-band tunneling origin of leakage current in DUT. To reduce GIDL current component of DUT off-state leakage current, the layout of standard cells was modified as shown in Figure 9. The gap between poly-silicon lines and device active regions was set to 0.2 µm. As a result the leakage current of analyzed chip was reduced to the acceptable level (~10 - 15 µA).

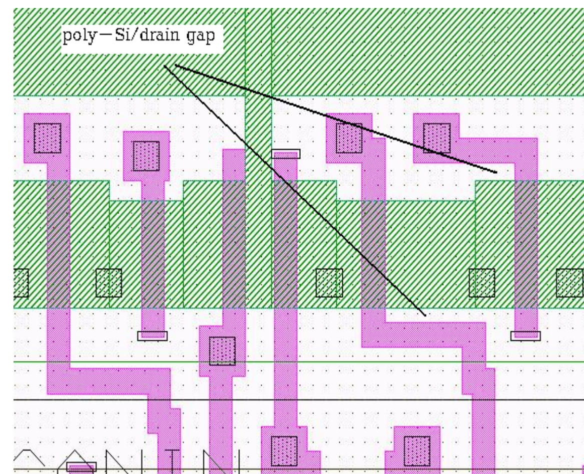

Fig. 9. Section of corrected flip-flop layout.

VI. Conclusion

In this paper, the submicron CMOC ICs degradation due to GIDL current is studied and the impact of LOCOS bird's beak thickness on GIDL current is investigated. The simulation results show that the lateral diffusion of source/drain regions may induce the tunneling effect and increase the leakage current two times from the nominal value for the given technology.

The obtained results show that the high charge trapped density (N_{ss}) in a LOCOS edge and the lateral diffusion of active regions may dramatically increase GIDL current from 10×10^{-12} A to 1×10^{-7} A per transistor. GIDL current is the crucial factor of off-state leakage current degradation in digital submicron CMOS circuits in case of improper layout of standard library cells. The layout correction of standard library cells allowed to significantly reduce the overall leakage current of analyzed chip from 0.1 - 1 mA to 10 - 15 μA and reduce the number of static I_{DDQ} failures in several times.

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