Impact of Technology Scaling on Bridging Fault Detections in sequential and combinational CMOS circuits

Oleg Semenov and Manoj Sachdev
Department of Electrical and Computer Engineering
University of Waterloo
Waterloo, Ontario, Canada N2L 3G1
osemenov@vlsi.uwaterloo.ca, msachdev@ece.uwaterloo.ca

Abstract - It is well known that classical fault models (stuck-at, stuck-open, stuck-on) cover only partially the spectrum of failures in today's integrated circuits (IC). Some realistic failures occurred in the logic circuits have to be considered at physical level and include its electrical behavior. Among these failures, gate-oxide short, floating gate and bridging fault types may produce intermediate voltages of difficult interpretations at logic level. This work investigates the influence of bridging fault (BF) between two interconnection lines on logic margin and logic swing of IC and the sensitivity of digital ICs realized on four different technologies (0.25 μm, 0.35 μm, 0.5 μm, 1.5 μm) to bridging fault. Several circuits, including D flip-flops and ISCAS benchmark circuits were analyzed to find out impact of technology scaling on BF defects detection. In this work we show that the sensitivity of IC to BF is increased with the technology scaling. The testing methodology was based on the use of voltage, temperature and frequency as parameters, which influence on the behavior of IC with BF.

Keywords - CMOS integrated circuits, bridging faults, logic margin, logic swing, technology scaling, VLSI testing, benchmark circuits

1 Introduction

The IC manufacturing process involves a sequence of basic processing steps, which are performed on sets of wafers. The outcome of manufacturing operations depends on three major factors: the process route which describes the sequence of fabrication steps and the process controlling parameters, the geometry of the fabricated IC, or layout and some randomly changing environmental factors, called disturbances. The control of a manufacturing operation is the set of parameters, which can be manipulated in order to achieve some desired change in the fabricated IC structure. The disturbances are environmental factors that cause variations in the outcome of a manufacturing operation.

This work is devoted to the research of a common cause of failure in CMOS digital ICs: the bridging fault (BF), which can be a major failure in ICs [1]. We describe the main technological reasons of BFs in ICs and their influence on the physical behavior of CMOS digital circuits. The parametric model of BFs to classify the BF resistance values was used. This is a general model, which can also include transistor stuck-on and stuck-at faults. We analyze the influence of BF on logic margin and logic swing of CMOS sequential IC under different operating temperatures, power supply voltages and frequency and estimate the sensitivity of CMOS digital IC to BF under different technological layout sizes (0.25 μm, 0.35 μm, 0.5 μm, 1.5 μm). Combinational CMOS benchmark 74X-Series Circuits was analyzed also for 0.25 μm and 0.35 μm technology. For each analyzed circuit we detected the value of critical resistance (R_b) and BF resistance under which the logic levels are reduced at 10% from the standard level. These values were detected for different operating temperatures, voltage supplier and technological feature sizes. DC and AC analyzed methods were used for the estimation of critical resistance values in a circuit. In the case of AC method the circuit simulation was carried out on operating frequency, which reached 60 - 70% of the maximum value for the given technology.

2 Review and Motivation

The trend projections of design and test characteristics are regularly published in the National Technology Roadmap for Semiconductors [2]. This review shows that in this decade transistors will scale down to 0.07-micron geometry, enabling the manufacture of fairly large memories and microprocessors. Another important factor is the increasing number of metal layers. It influences the types of tests and defects, which must be screened. The design and test for deep submicron IC will be dominated by interconnect. Gate delay and leakage currents will also have contribution to the total amount of defects but not so much [3], although there does not exist a unified opinion on this problem. Downsizing of components in ULSI scaling has continuously driven the progress of ULSI capabilities in terms of information processing density and complexity as shown in Figure 1 [4].

The first problem is the development new fault models. The experimental data shows that there are many new failure modes in deep submicron space, where metal lines are becoming narrow and spacing is becoming smaller. Some of these failure modes are inductive and capacitive. Because the dielectric constants are not improving fast enough, capacitive coupling effects dominate in interconnect and delay.

A new technology processes (for example the process of magnetron sputtering of complex metal films (Al-Ti-Si) influences the metal layer properties for signal wiring and increases probability of BF defects in the connecting lines. The second problem is the fault localization. For instance, a microprocessor contains over five million transistors and five levels of wiring in a 196-mm^2 area [5]. But the size of nickel particle, which can cause a short between two nodes, may be a 0.3 x 0.4 μm. The failure analysis would locate and identify this defect, knowing only its electrical effects on the chip. Figure 2. illustrates the projected increase in device complexity versus the projected decrease in minimum defect size, both relative to 1995 levels. The complexity is the sum of the number of transistors and the total wiring length on the chip [5].

0-7695-0637-2/00 $10.00 © 2000 IEEE

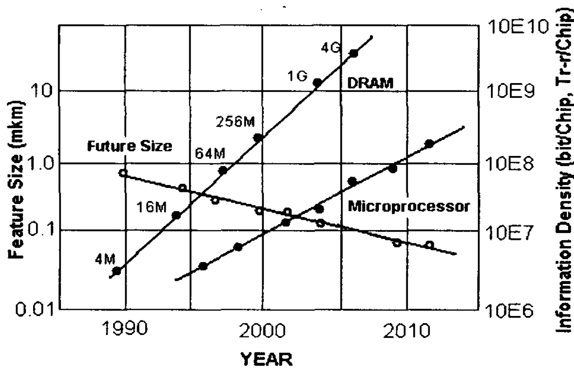

Figure 1. ULSI trends of feature size and information density in DRAM and microprocessors [4]

The decreasing of minimum defect size has the influence on accuracy of yield models, which are used to determine the probability that a manufactured semiconductor device performs its function correctly. The problem with the concept of the critical area as a function of the defect size is that the defect size is a random variable and therefore the critical area is a random variable, as well. A typical distribution of the defect size is such that the vast majority of defects have small sizes, but the density of defects is sharply increased with the decrease of the defect size. But on other hand, small defects may, or may not cause failure. Consequently, inadequate estimation of the critical area for ultra deep submicron (UDSM) technology may lead to a large error in yield estimation. As a result of technology scaling of MOS transistor dimensions, transistor characteristics can not be accurately modeled using the classical approach without recourse to a large number of empirical parameters. Various physical effects must be considered for UDSM modeling, such as quantization of the immersion layer carrier, mobility degradation, carrier velocity saturation and overshoot, vertical and lateral doping profiles.

In our article, we show that the scaling of technology result in not only increased sensitivity of bridging defects but also their detection becomes harder. Thus the used AC test method of BF defects is important for high performance testing of complex ICs.

3 The bridging fault in IC

The disturbances of technological processes can cause either global or local deformations. The deformations, which affect IC elements, can be called global. Similarly, disturbances that cause only local deformations (affected regions are small compared to the total area of an IC chip) are the local disturbances. Traditionally, they are assumed to be produced by the lithography process and to cause shorts or break in IC connections [6].

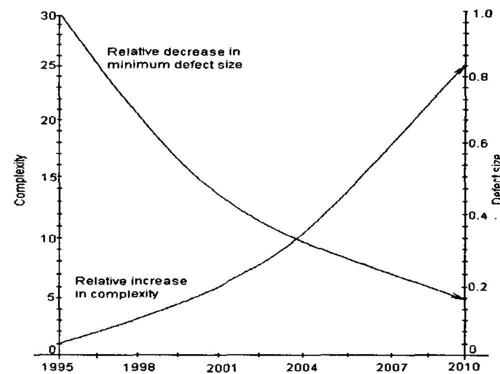

Figure 2. Projected increase in relative complexity versus minimum defect size

For example the photoresist may be shaded by a particle deposited directly on top of the photoresist during the exposition step. Such particles are among the most common reasons causing shorts. They are usually generated by the manufacturing equipment. The above illustration describes defects in the metal layer, but of course, exactly the same mechanism can produce spots of extra material in other IC layers.

Bridges have nonlinear or linear (ohmic) I-V properties with resistance from zero to >1 MΩ. Nonlinear BF includes most types of gate oxide shorts, soft p-n junctions, and transistor punchthrough. Ohmic shorts also occur in IC pattering defect that leave "bridges" of metal (or polysilicon) and in certain forms of gate oxide shorts. Bridge defect resistance is the dominant factor in a bridge detection method. Correct Boolean functionality exists for signal node bridge defect when the defect exceeds critical resistance. Critical resistance is a function of the contending transistor current drive strengths and therefore varies with circuit design, logic input levels and process variation. The value of the critical resistance R_b varies significantly due to the wide possibilities of the bridge mechanisms (usually this range is from 10Ω to 5 kΩ) [7].

A bridging fault (BF) is an undesired connection between two or more nodes within an integrated circuit. BF, typically, can not be modeled by the stuck-at approach. This paper uses a model of bridge defect as a resistive path between the two bridging nodes (see Figure 3) for the fault.

4. The description of the analyzed circuit

We analyzed the electrical effects of a resistive short located between two chains of two CMOS flip-flops and one inverter. The first chain had a steady high level state flip-flop and inverter (constant logic level «1») and the second chain had a steady low level state flip-flop and inverter (constant logic level «0»), [Fig. 4].

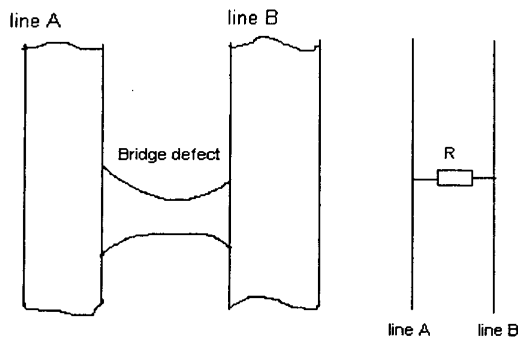

Figure 3. Bridging defect and its model

This is a DC analysis technique, which analyses the static behavior of circuits. AC analysis technique analyses the dynamic behavior of circuits when both the data and clock signals are changing together. We used this method for evaluation of BF defects influence on circuit operating in a dynamic mode.

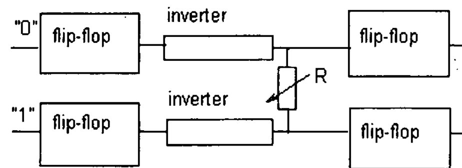

Figure 4. The electrical circuit for a bridging fault analysis (DC analysis)

All the simulations were carried out in the HSPICE environment in CADENCE. This is a special model, which includes the mobility degradation, velocity saturation and other short channel effects of transistor operation. In our work we performed circuit simulation for 0.25, 0.35, 0.5 and 1.5 μm CMOS technology.

5. Bridging Fault Analysis in sequential CMOS ICs

The first step was to detect the maximum frequency of analyzed circuit for four different CMOS technologies. Dimensions of transistors used for the simulations are shown in Table 1. We chose dimensions of transistors so that the ratio of width and length of n-channel and p-channel transistors is approximately similar for each technology.

We did not try to optimize the dimensions of transistors for the receiving of maximum possible frequency. We defined the maximum operating frequency (f_{max}) of analyzed IC with traditional dimensions of transistors for each technology. The attempt increases a clock frequency to break a normal circuit operation. The operating clock frequency ($f_{operating}$) was chosen as (0.5 - 0.7) * f_{max}, because we assumed that the circuit operated robustly at this frequency. The calculated results of maximum and operating frequencies are represented in Table 2.

The technological scaling improves circuit performance by reducing capacitance and potential swings. When ideal scaling is applied, all horizontal and vertical dimensions of transistors are scaled down by 1/S (S>1 - scaling factor), parasitic gate capacitance ($C_g=[\varepsilon_{ox}*W*L]/t_{g\ ox}$) decreases by 1/S and intrinsic gate delay improves by 1/S. This fact explains the increasing of CMOS IC operating frequency as a result of the reduction of feature size.

Table 1. Dimensions of transistors used for the simulations

CMOS technology	The size of n-MOS transistor, $K_n = (W/L)$	The size of p-MOS transistor, $K_p = (W/L)$	The ratio coefficient: $K = K_p/K_n$
0.25 μm	2.6 μm/0.25 μm = 10.4	4.4 μm/0.25 μm = 17.6	1.69
0.35 μm	6.3μm/0.35 μm = 18	10.8μm/0.35μm = 31	1.7
0.5 μm	6.8μm/0.6 μm = 11	10.8μm/0.6μm = 18	1.64
1.5 μm	16.5μm/1.5 μm= 11	27μm/1.5μm = 18	1.64

Table 2. Frequencies used for the simulations of IC with BF fault

CMOS technology	Maximum frequency, f_{max}, MHz	Operating frequency, $f_{operating}$, MHz
0.25 μm	2100	1500
0.35 μm	1350	750
0.5 μm	1050	650
1.5 μm	400	250

The next step of our research was the DC simulation of CMOS circuit (Fig. 3) when the resistor value was changed from 0Ω to 100 KΩ. For this simulation, data is fixed and clock is toggled at $f_{operating}$ in order to excite the bridging fault. We did simulations for three different conditions: 1) normal operating conditions - temperature T=25 °C, voltage supplier Vdd=2.5V (for 0.25 μm technology), Vdd=3.3 (for 0.35 and 0.5 μm technology) or 5 V (for 1.5μm technology); 2) best operating conditions - T=0 °C, Vdd=2.65, 3.5 or 5.3 V; 3) worst operating conditions - T=85°C, Vdd= 2.35, 3.1 or 4.7 V. On the basis of DC simulations, we plotted the dependence of logic swing and logic margin on the value of bridging resistor "R". These dependencies are shown in Figure 5 for 0.25 μm CMOS technology. From the plots we defined the value of resistance for each technology and each condition of circuit operation on which the logic level "0" or "1" is reduced by 10% from nominal value. The obtained results are given in Table 3. When the resistance of the MOSFET channels becomes very small the Vdd predominantly drops on the BF resistor, because R_{NMOS} and R_{PMOS} are very small (BF resistor, R_{NMOS} and R_{PMOS} are connected in series) [8]. The resistance of most defects is independent of the voltage applied, but the MOS transistors channel resistance is a function of V_{gs} and V_{ds} voltages.

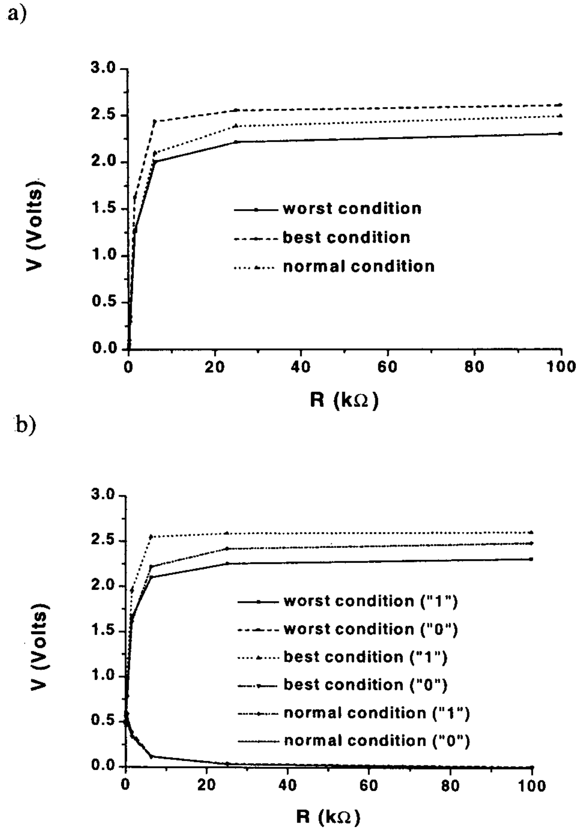

Figure 5. Logic swing (a) and logic margin (b) for 0.25 μm technology

This fact may explain the dependence of critical BF resistance value on disturbance of applied voltage supply. MOS transistor characteristics are strongly temperature dependent. The variation of channel conductance with temperature is due to the variation of the threshold voltage and of the inversion layer mobility. The channel conductance is defined by the expression: $G = \mu_{eff} * [W/L]*C_o*(V_G-V_T)$ [8]. The temperature dependent terms in G are the effective inversion layer mobility μ_{eff} and the threshold voltage V_T. MOSFET transistor generally is operating in the strong inversion mode, where an increase of the operating temperature results in an increase of the channel resistance. This fact may be explained by the dependence of critical BF resistance value on variations of operating temperature. The data in Table 3 shows that the transistors are becoming weaker at a result of technology scaling and a smaller defect resistance in smaller geometry causes the 10% reduction in the swing.

The last step of our research was the parametric simulation of CMOS circuit under AC conditions (dynamic behavior). In this case both data and clock are changing together.

Table 3. BF resistance values for difference technologies and conditions on which the logic levels are reduced by 10% from nominal value (DC analyses method)

CMOS Technology	Best Conditions	Normal Conditions	Worst Conditions
0.25 μm	1.2 KΩ	2.1 KΩ	2.7 KΩ
0.35 μm	1.5 KΩ	2.5 KΩ	3.4 KΩ
0.5 μm	2.2 KΩ	3.0 KΩ	4.1 KΩ
1.5 μm	4.2 KΩ	5.0 KΩ	5.9 KΩ

Clock signal had frequency as shown in Table 2 (see operating frequency). Data signal parameters were chosen from the circuit robust operating condition. Typically the data signal frequency was 0.5 * f_{max} (clock signal). We defined the critical BF resistance values when output signals of the circuit were totally degraded (circuit did not function). The obtained results are given in Table 4.

Table 4. Critical resistance values for different technologies and conditions (AC analysis method)

CMOS technolo-Gy	Best Conditions	Normal Conditions	Worst Conditions
0.25 μm	900 Ω	1100 Ω	1800 Ω
0.35 μm	700 Ω	750 Ω	950 Ω
0.5 μm	470 Ω	580 Ω	690 Ω
1.5 μm	450 Ω	550 Ω	660 Ω

Typically, the output voltage of the circuit is stable for high defect resistance but swings to the opposite value of the voltage range when the resistance is lower than a certain value. The resistance value where the voltage response crosses Vdd/2 is called critical resistance. Usually the output voltage is changed between V_T (or Vdd- V_T) and Vdd/2. In other cases, reducing BF resistor value more than threshold value results in a logic mistake and we accepted this value as critical resistance also.

The explanation of these results is not trivial. Probably, due to transistor scaling we observe two different processes. On one hand, the IC sensitivity to BF defects is increased (see the results of AC analysis in table 4). It means that the interval $[0:R_{critical}]$, when circuit does not work properly is increased under technology scaling. The preliminary results of technology scaling impact on BF defects in inverter chain were received in article [9]. On other hand, the downsizing of components in CMOS IC provides improvement of gate delay [4] (Figure 6). The total delay (gate and interconnect delay) is reduced while the scaling of feature size does not achieve of 0.25 μm technology. It may be the reason of partial compensation of logic levels degradation (as a result of BF influence) and the increase of CMOS IC robustness (critical resistance values for 0.5 μm technology and 1.5 μm technology are not very different).

Possibly the exact answer will be received from the results of circuit simulation for 0.18 μm technology. But

this is the subject of our future research.

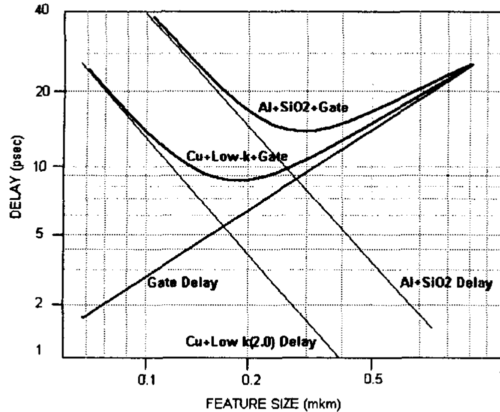

Figure 6. Gate and interconnect delay as a function of feature size: Cu+Low-k versus Al+SiO$_2$

6. Bridging Fault Analysis in combinational benchmark CMOS ICs

The simple example of combinational benchmark CMOS ICs is a 74X-series circuits. The ISCAS-85 circuits have well-defined, high-level structures and functions based on common building blocks such as multiplexers, ALUs, adders and decoders. As structural blocks for ISCAS-85 and ISCAS-89 circuits may be successfully used the 74X-series circuits [10]. For instance, part of the ISCAS-85 c3540 circuit realizes the same of logical and arithmetic functions as the 74181 ALU/function generator. Because the common 74181 ALU has a CLA (carry-look ahead) generator module, it is not surprising to find a similar module in the c880 (8-bit ALU). By this reason we choose the 74X-series circuits as the object of our research. The following circuits were tested 74182 (4-bit carry-look ahead generator), 74283 (4-bit adder) and 74181 (4-bit ALU). The gate-level schematic for these circuit was downloaded from the web site http://www.eecs.umich.edu/~jhayes/iscas/benchmark.html

The electrical circuit for a BF influence analysis in 74X-series circuits was the same as for sequential circuit (see Figure 4). But we substituted flip-flops on combinational benchmark circuits, which was created on the basis of standard logic gates library in Cadence. The maximum and operating frequencies (60-70 % from the maximum value) was detected for 0.35 μm and 0.25 μm technology. The calculated results of maximum and operating frequencies have shown in Table 5. The method of critical resistance value detection and resistance value detection under which the logic levels degraded to 10% from the nominal meaning for different operating temperature, voltages supply and feature technology size is described in section 4 of this article. The detected resistance values for case of DC analyzes are shown in Table 7 and Table 8.

The detected resistance values in case of AC analyzes (simulation was done on operating frequency) are shown in

Table 5. Frequencies used for the simulation of combinational benchmark CMOS ICs with BF defect

Kind of Circuit	Statistics	Maximum frequency	Operating frequency
74182 : 4-bit carry-look-ahead generator	9 inputs; 5 outputs; 19 gates; test vector: 000001111	0.35 μm technology: 300 MHz 0.25 μm technology: 450 MHz	0.35 μm technology: 200 MHz 0.25 μm technology: 250 MHz
74283 : 4-bit adder	9 inputs; 5 outputs; 36 gates; test vector: 011110000	0.35 μm technology: 300 MHz 0.25 μm technology: 450 MHz	0.35 μm technology: 200 MHz 0.25 μm technology: 250 MHz
74181 : 4-bit ALU	14 inputs; 8 outputs; 61 gates; test vector: 01010000111101	0.35 μm technology: 300 MHz 0.25 μm technology: 450 MHz	0.35 μm technology: 200 MHz 0.25 μm technology: 300 MHz

Table 7. DC analyses of BF in 74X-Series Circuits (0.35 μm technology)

Kind of Circuit	Normal Conditions	Best Conditions	Worst Conditions
74182 : 4-bit CLA	R (10%) = 15.8 Kohm $R_{critical}$ = 1150 Ohm	R (10%) = 13.7 Kohm $R_{critical}$ = 1040 Ohm	R (10%) = 17.5 Kohm $R_{critical}$ = 1270 Ohm
74283 : 4-bit adder	R (10%) = 16.3 Kohm $R_{critical}$ = 660 Ohm	R (10%) = 14.1 Kohm $R_{critical}$ = 580 Ohm	R (10%) = 18.0 Kohm $R_{critical}$ = 780 Ohm
74181 : 4-bit ALU	R (10%) = 16.7 Kohm $R_{critical}$ = 920 Ohm	R (10%) = 14.5 Kohm $R_{critical}$ = 850 Ohm	R (10%) = 17.5 KOhm $R_{critical}$ = 1020 Ohm

Table 9 and Table 10. The received results indicate that the sensitivity of both combinational and sequential circuits to BF defects is increased under technology scaling and deterioration of operating conditions (because the interval [0:$R_{critical}$], when circuit does not work, is increased in these cases). We can observe that the critical resistance values in case of AC analyses are higher than in case of DC analyses. Because BF can result in the same kinds of effect as delay faults. Typically, the delay of circuit with BF defect is higher than in fault-free circuit [11]. This fact may explain why the circuit becomes more sensitive to BF defect in case of AC analyses.

7. Future Research Directions

As we know, each process disturbance may cause a number of different changes in IC performance. And we call this change in behavior a fault. The performance faults can be divided into two classes: soft-performance faults and hard-performance faults. If IC is functionally correct but some performance measure lies outside the specified range, we say a soft-performance fault has occurred. If IC

does not function properly (e. g. some state transitions do not occur), we say a hard -performance fault has occurred.

Table 8. DC analyses of BF in 74X-Series Circuits (0.25 μm technology)

Kind of Circuit	Normal Conditions	Best Conditions	Worst Conditions
74182 : 4-bit CLA	R (10%) = 14.9 Kohm $R_{critical}$ = 1300 Ohm	R (10%) = 12.8 Kohm $R_{critical}$ = 1130 Ohm	R (10%) = 16.2 Kohm $R_{critical}$ = 1380 Ohm
74283 : 4-bit adder	R (10%) = 15.3 Kohm $R_{critical}$ = 890 Ohm	R (10%) = 13.2 KOhm $R_{critical}$ = 780 Ohm	R (10%) = 16.7 Kohm $R_{critical}$ = 930 Ohm
74181 : 4-bit ALU	R (10%) = 10.5 Kohm $R_{critical}$ = 1140 Ohm	R (10%) = 9.4 KOhm $R_{critical}$ = 1060 Ohm	R (10%) = 11.1 Kohm $R_{critical}$ = 1170 Ohm

Table 9. AC analyses of BF in 74X-Series Circuits (0.35 μm technology)

Kind of Circuit	Normal Conditions	Best Conditions	Worst Conditions
74182 : 4-bit CLA	$R_{critical}$ = 1250 Ohm	$R_{critical}$ = 1000 Ohm	$R_{critical}$ = 1360 Ohm
74283 : 4-bit adder	$R_{critical}$ = 720 Ohm	$R_{critical}$ = 640 Ohm	$R_{critical}$ = 830 Ohm
74181 : 4-bit ALU	$R_{critical}$ = 940 Ohm	$R_{critical}$ = 880 Ohm	$R_{critical}$ = 1060 Ohm

Table 10. AC analyses of BF in 74X-Series Circuits (0.25 μm technology)

Kind of Circuit	Normal Conditions	Best Conditions	Worst Conditions
74182 : 4-bit CLA	$R_{critical}$ = 1390 Ohm	$R_{critical}$ = 1230 Ohm	$R_{critical}$ = 1450 Ohm
74283 : 4-bit adder	$R_{critical}$ = 1050 Ohm	$R_{critical}$ = 900 Ohm	$R_{critical}$ = 1140 Ohm
74181 : 4-bit ALU	$R_{critical}$ = 1160 Ohm	$R_{critical}$ = 1080 Ohm	$R_{critical}$ = 1200 Ohm

In our work we considered a bridging fault as a hard - performance fault, which influences the behavior of digital CMOS IC. But spot defects (for example, extra metal defects) do not always occur as catastrophic faults (hard - performance faults). In future we are planning also to consider the influence of BF defects within logic structure of the circuit on its behavior. The object of our research will be ISCAS-85 and 74X-series benchmark circuits. This analysis will include the evaluation of critical BF resistance value as function of feature size scaling, operating temperature and frequency, and voltage supply. Within CMOS macro-gates resistive faults can establish undesirable current-paths between the power-supply and ground, as a consequence, the output signal line can assume intermediate voltage levels, always representing a significant problem because they induce degradation on the dynamic performance of the circuit and also lead to logic errors.

8. Conclusions

In this article we have shown that the sensitivity of CMOS IC to BFs is increased with the reduction of feature size of IC, voltage supply and the increase of operating temperature. Because the critical resistance value of BF (the resistance above which the defect cannot be detected) is increased, as our research show, the problem of CMOS ICs testing becomes more complicated. This resistance depends on the maximum frequency that a given test can measure. Many tests run at a base test cycle frequency that is substantially less than the systems clock frequency. The defect's effect on normal circuit operation depends on its operating frequency; thus, the defect has another resistance (higher) associated with operating frequency. Unfortunately, bridging defects are not 100% detectable by I_{DDQ} or Boolean methods only. In our research we used the DC and AC voltage test method (parametric method), which can successfully supplement the existing test methods of BF in CMOS IC. It defines the necessity and perspective of our research and this article.

9. Acknowledgement Authors gratefully acknowledge support of Communication and Information Technology Ontario (CITO) for this work.

10. References

[1] F. Joel Ferguson, John P. Shen "A CMOC Fault Extractor for Inductive Fault Analyses", IEEE Transactions on Computer Aided Design, Vol. 7, No. 11, November 1988

[2] The National Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, Calif., 1994

[3] G. Singer "The Future of Test and DFT", IEEE Design & Test of Computers, July-September, p.11, 1997

[4] T. Kikkawa "VLSI interconnect process integration", 1998 5th International Conference on Solid - State and Integrated Circuit Technology, Proceedings IEEE, p. 40, 1998

[5] D. P. Vallett "IC Failure Analysis: The Importance of Test and Diagnostics", IEEE Design & Test of Computers, July-September, p.76, 1997

[6] Doi J. A. et al. "Detection and Physical Characterization of Spot Defects in Metal IC Interconnections", 172 Meeting of The Electrochemical Society, p. 637, 1986

[7] H.Vierhaus, W. Meyer and U. Glaser "CMOS Bridges and Resistive Transistor Faults: I_{DDQ} versus Delay Effects", Int. Test Conf., p. 83, Oct. 1993

[8] N. Arora "MOFET Models for VLSI circuit simulation - Theory and Practice", Springer - Verlag, Wein and New York, 1993

[9] O.V. Maiuri, W.R. Moore "Implications of voltage and dimension scaling on CMOS Testing: the Multidimensional Testing Paradigm", VLSI test symposium, p.22, 1998

[10] M.C. Hansen, H. Yalcin and J.P. Hayes "Univeiling the ISCAS-85 Benchmarks: A case study in reverse engineering", IEEE Design & Test of computers, July-September, p.72, 1999

[11] S.D. Millman and J.H. Acken "Special Application of the voting model for Bridging Faults", IEEE Journal of Solid-State Circuits, vol. 29, No. 3, p. 263, March 1994