Impact of Technology Scaling on Bridging Fault Detections

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Abstract - It is well known that classical fault models (stuck-at, stuck-open, stuck-on) cover only partially the spectrum of failures in today's integrated circuits (IC). Some realistic failures occurred in the logic circuits have to be considered at physical level and include its electrical behavior. Among these failures, gate-oxide short, floating gate and bridging fault types may produce intermediate voltages difficult to interpretation at logic level. This work investigates the influence of bridging fault (BF) between two interconnection lines on logic margin and logic swing of IC and the sensitivity of IC realized on four different technologies (0.25 μm, 0.35 μm, 0.5 μm, 1.5 μm) to bridging fault. In this work we show that the sensitivity of IC to BF is increased with the technology scaling. The testing methodology was based on the use of voltage, temperature and frequency as parameters, which influence on the behavior of IC with BF.

Keywords - CMOS integrated circuits, bridging faults, logic margin, logic swing, technology scaling, VLSI testing.

1. Introduction

The IC manufacturing process involves a sequence of basic processing steps, which are performed on sets of wafers. The outcome of manufacturing operations depends on three major factors: the process route which describes the sequence of fabrication steps and the process controlling parameters, the geometry of the fabricated IC, or layout and some randomly changing environmental factors, called disturbances. The control of a manufacturing operation is the set of parameters, which can be manipulated in order to achieve some desired change in the fabricated IC structure. The disturbances are environmental factors that cause variations in the outcome of a manufacturing operation. The process disturbances that occur in the IC manufacturing process can be characterized in terms of the physical nature of the effects they have on IC performance. Effects on performance can be described in terms of changes in the electrical characteristics of the IC or in terms of changes in circuit connection.

This work is devoted to the research of a common cause of failure in CMOS digital ICs: the bridging fault (BF), which can be a major failure in ICs [1]. We describe the main technological reasons of BFs in ICs and their influence on the physical behavior of CMOS digital circuits. The parametric model of BFs to classify the BF resistance values was used. This is a general model, which can also include transistor stuck-on and stuck-at faults. We analyze the influence of BF on logic margin and logic swing of CMOS IC under different operating temperatures, power supply voltages and frequency and estimate the sensitivity of CMOS digital IC to BF under different technological layout sizes (0.25 μm, 0.35 μm, 0.5 μm, 1.5 μm). For the analyzed circuit we detected the value of critical resistance (R_b) and BF resistance under which the logic levels are reduced at 10% from the standard level. DC and AC analyzed methods were used for the estimation of critical resistance values in a circuit. In the case of AC method the circuit simulation was carried out on operating frequency, which reached 60-70% of the maximum value for the given technology.

2. Review and Motivation

The trend projections of design and test characteristics are regularly published in the National Technology Roadmap for Semiconductors [2]. This review shows that in the next decade transistors will scale down to 0.07-micron geometry, enabling the manufacture of fairly large memories and microprocessors. Another important factor is the increasing number of metal layers. It influences the types of tests and defects, which must be screened. The design and test for deep submicron IC will be dominated by interconnect. Gate delay and leakage currents will also have contribution to the total amount of defects but not so much [3].

The first problem is the development new fault models. The experimental data shows that there are many new failure modes in deep submicron space, where metal lines are becoming narrow and spacing is becoming smaller. Some of these failure modes are inductive and capacitive coupling of lines. Because the dielectric constants are not improving fast enough, capacitive coupling effects to dominate interconnect and delay. A new technological processes (for example the process of magnetron sputtering of complex metal films (Al-Ti-Si) influences on the metal layer properties for signal wiring and increases of defects probability in the connecting "signal to signal" lines (BF defects).

The second problem in the failure analysis is the fault localization. For instance, a microprocessor contains over five million transistors and five levels of wiring in a 196-mm^2 area [4]. But the size of nickel particle, which can be the causing of short between two nodes, may be a 0.3 x 0.4 μm. The failure analysis would locate and identify this defect, knowing only its electrical effects on the chip. Figure 1. illustrates the projected increase in device complexity versus the projected decrease in minimum defect size, both relative to 1995 levels. The complexity is the sum of the number of transistors and the total wiring length on the chip [2]. The decreasing of minimum defect size has the influence on accuracy of yield models, which are used to determine the probability that a manufactured semiconductor device performs its function correctly.

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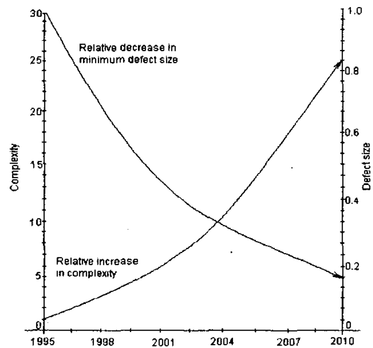


Figure 1. Projected increase in relative complexity versus minimum defect size

The problem with the concept of the critical area as a function of the defect size is that the defect size is a random variable and therefore the critical area is a random variable, as well. A typical distribution of the defect size is such that the vast majority of defects have small sizes, but the density of defects is sharply increased with the decrease of the defect size. But on other hand a small defects may, or may not cause failure (small size defects have small critical area). Consequently, inadequate estimation of the critical area for ultra deep submicron (UDSM) technology may lead to a large error in yield estimation.

A result of technology scaling of MOS transistor dimensions, transistor characteristics cannot be accurately modeled using the classical approach without recourse to a large number of empirical parameters. Various physical effects must be considered for UDSM modeling, such as quantization of the immersion layer carrier, mobility degradation, carrier velocity saturation and overshoot, vertical and lateral doping profiles. These physical effects define the sensitivity of IC to BF defects under the technology scaling of MOS transistor dimensions.

In our article, we show that the increasing of CMOS IC complexity as a result of feature size scaling from 1.5 μm to 0.25 μm to define the sensitivity of IC to BF defects. Thus the used DC and AC test methods of BF defects analyzes are important test tool for diagnostic of complex ICs.

3 The bridging fault in IC

The disturbances of technological processes can cause either global or local deformations. The deformations, which affect all IC elements, can be called global. Similarly, disturbances that cause only local deformations (affected regions are small compared to the total area of an IC chip) are the local disturbances. Pinholes, spikes, spot defects are examples of local deformations. Local process disturbances manifest as areas with extra missing or drastically changed material occurring in any IC layer forming spot defects. Traditionally, they are assumed to be produced by the lithography process and cause shorts or break in IC connections [5]. For example the photoresist may be shaded by a particle deposited directly on top of the photoresist during the exposition step. Such particles are among the most common reasons causing shorts. They are usually generated by the manufacturing equipment. Particles shade photoresist and cause a short. Other defect mechanism is caused by a particle deposited on the surface of the wafer during photoresist and metal layer etching. The deposited particle protects the surface of the metal causing a short. The above illustration describes defects in the metal layer, but of course, exactly the same mechanism can produce spots of extra material in other IC layers.

Bridges have nonlinear or linear (ohmic) I-V properties with resistance from zero to >1 MΩ. Nonlinear BF includes most types of gate oxide shorts, soft p-n junctions, and transistor punchthrough. Ohmic shorts also occur in IC pattering defect that leave "bridges" of metal (or polysilicon) and in certain forms of gate oxide shorts. Bridge defect resistance is the dominant factor in a bridge detection method. Correct Boolean functionality exists for signal node bridge defect when the defect exceeds critical resistance. Critical resistance is a function of the contending transistor current drive strengths and therefore varies with circuit design, logic input levels and process variation. The value of the critical resistance R_b varies significantly due to the wide possibilities of the bridge mechanisms (usually this range is from 10Ω to 5 kΩ) [6].

A bridging fault (BF) is an undesired connection between two or more nodes within an integrated circuit. This connection can be caused by an extra spot of conducting material or by a spot of missing insulating material. BF, typically, can not be modeled by the stuck-at approach. This paper uses a model of bridge defect as a resistive path between the two bridging nodes (see Figure 2) for the fault.

4. The description of the analyzed circuit

We analyzed the electrical effects of a resistive short located between two chains of two CMOS flip-flops and one inverter. The first chain had a steady high level state flip-flop and inverter (constant logic level «1») and the second chain had a steady low level state flip-flop and inverter (constant logic level «0»), see Figure 3.

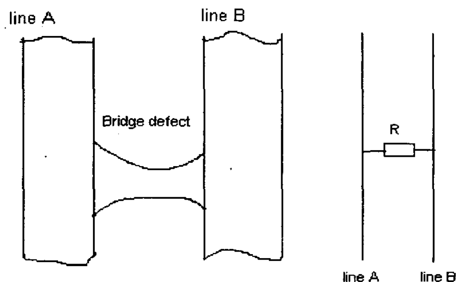


Figure 2. Bridging defect and its model

This is a DC analysis technique, which analyses the static behavior of circuits.

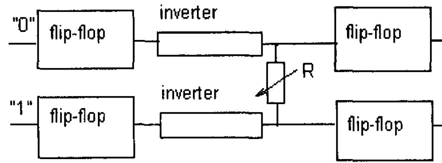


Figure 3. The electrical circuit for a bridging fault analysis (DC analysis)

AC analysis technique analyses the dynamic behavior of circuits when both the data and clock signals are changing together. We used this method for evaluation of BF defects influence on circuit operating in a dynamic mode.

All the simulations were carried out in the HSPICE environment in CADENCE. This is a special model, which includes the mobility degradation, velocity saturation and other short channel effects of transistor operation. In our work we performed circuit simulation for 0.25, 0.35, 0.5 and 1.5 µm CMOS technology.

5. Bridging Fault Analysis in CMOS ICs

The first step was to detect the maximum frequency of analyzed circuit for four different CMOS technologies. Dimensions of transistors used for the simulations are shown in Table 1. We chose dimensions of transistors so that the ratio of width and length of n-channel and p-channel transistors is approximately similar for each technology.

We did not try to optimize the dimensions of transistors for the receiving of maximum possible frequency. We defined the maximum operating frequency (f_{max}) of analyzed IC with traditional dimensions of transistors for each technology. The attempt increases a clock frequency to break a normal circuit operation. The operating clock frequency ($f_{operating}$) was chosen as (0.5 - 0.7) * f_{max}, because we assumed that the circuit operated robustly this frequency. The calculation results of maximum and operating frequencies are represented in Table 2.

Table 1. Dimensions of transistors used for the simulations

CMOS technology	The size of n-MOS transistor, $K_n = (W/L)$	The size of p-MOS transistor, $K_p = (W/L)$	The ratio coefficient: $K = K_p/K_n$
0.25 µm	2.6 µm/0.25 µm = 10.4	4.4 µm/0.25 µm = 17.6	1.69
0.35 µm	6.3µm/0.35 µm = 18	10.8µm/0.35µm = 31	1.7
0.5 µm	6.8µm/0.6 µm = 11	10.8µm/0.6µm = 18	1.64
1.5 µm	16.5µm/1.5 µm= 11	27µm/1.5µm = 18	1.64

The technology scaling improves circuit performance by reducing capacitance and potential swings. When ideal scaling is applied, all horizontal and vertical dimensions of transistors are scaled down by 1/S (S>1 - scaling factor), parasitic gate capacitance ($C_g=[\varepsilon_{ox}*W*L]/t_{g\,ox}$) decreases by 1/S and intrinsic gate delay improves by 1/S. This fact explains the increasing of CMOS IC operating frequency as a result of the reduction of feature size.

Table 2. Frequencies used for the simulations of IC with BF fault

CMOS technology	Maximum frequency, f_{max}, MHz	Operating frequency, $f_{operating}$, MHz
0.25 µm	2100	1500
0.35 µm	1350	750
0.5 µm	1050	650
1.5 µm	400	250

The next step of our research was the DC simulation of CMOS circuit (see Figure 3) when the resistor value was changed from 0Ω to 100 KΩ. For this aim the impulse power supplier (Data signal) was substituted for VDC power supplier and the simulations were produced on $f_{operating}$ clock frequency, which was detected on the first step (DC analysis method). We did simulations for three different conditions: 1) normal operating conditions - temperature T=25 °C, voltage supplier Vdd=2.5V (for 0.25 µm technology), Vdd=3.3 (for 0.35 and 0.5 µm technology) or 5 V (for 1.5µm technology); 2) best operating conditions - T=0 °C, Vdd=2.65, 3.5 or 5.3 V; 3) worst operating conditions - T=85°C, Vdd= 2.35, 3.1 or 4.7 V. On the basis of DC simulations we plotted the dependence of logic swing and logic margin on the value of bridging resistor "R". These dependencies are shown in Figure 4 for 0.25 µm CMOS technology. From the plots we defined the value of resistance for each technology and each condition of circuit operation on which the logic level "0" or "1" is reduced by 10% from standard meaning. The obtained results are given in Table 3.

These results may be explained by the following reasons. The scaling of MOS transistor dimensions influents on the output resistance value of transistor. The channel length reduction is accompanied by a total channel resistance reduction [7]. When the resistance of the MOSFET channels becomes very small the voltage supplier Vdd predominantly drops on the BF resistor, because R_{NMOS} and R_{PMOS} are very small (BF resistor, R_{NMOS} and R_{PMOS} are connected in series). The resistance of most defects is independent of the voltage applied, but the MOS transistors channel resistance is a function of V_{gs} and V_{ds} voltages. This fact may explain the dependence of critical BF resistance value on disturbance of applied voltage supply. MOS transistor characteristics are strongly temperature dependent. The variation of channel conductance with temperature is due to the variation of the threshold voltage and of the inversion layer mobility. The channel conductance is defined by the expression: $G = \mu_{eff} * [W/L]*C_o*(V_G-V_T)$ [7]. The

temperature dependent terms in G are the effective inversion layer mobility μ_{eff} and the threshold voltage V_T.

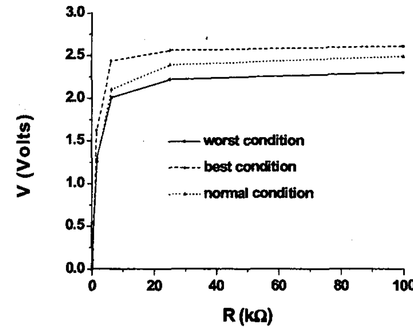
Table 3. BF resistance values for difference technologies and conditions on which the logic levels are reduced by 10% from standard meaning (DC analyses method)

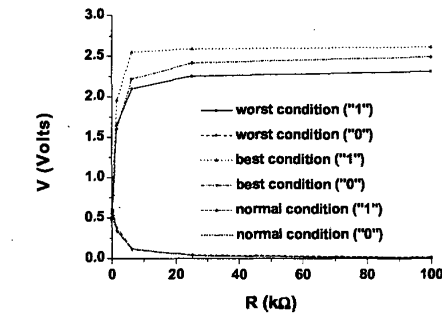
CMOS technology	Best Conditions	Normal Conditions	Worst Conditions
0.25 µm	1.2 KΩ	2.1 KΩ	2.7 KΩ
0.35 µm	1.5 KΩ	2.5 KΩ	3.4 KΩ
0.5 µm	2.2 KΩ	3.0 KΩ	4.1 KΩ
1.5 µm	4.2 KΩ	5.0 KΩ	5.9 KΩ

MOSFET transistor generally is operating in the strong inversion mode, where an increase of the operating temperature results in an increase of the channel resistance. This fact may be explained by the dependence of critical BF resistance value on variation of operating temperature. The data in Table 3 shows that the transistors are becoming weaker at a result of technology scaling and smaller defect resistance in smaller geometry causes the 10% reduction in the swing.

The last step of our research was the parametric simulation of CMOS circuit under AC conditions (dynamic behavior). In this case both data and clock are changing together. Clock signal had frequency as shown in Table 2 (see operating frequency). Data signal parameters was chosen from the circuit robust operating condition. Typically the data signal frequency was 0.5 * $f_{operating}$ (clock signal). We defined the critical BF resistance values when output signals of the circuit were totally degraded (circuit did not function). The obtained results are given in Table 4. The explanation of these results is not trivial. Probably, in result of transistor dimensions scaling we observe two different processes. On one hand the IC sensitivity to BF defects is increased (see the results of AC analysis in table 4). It means that the interval [0:$R_{critical}$], when circuit does not work properly is increased under technology scaling. The preliminary results of technology scaling impact on BF defects in inverter chain were received in article [8]. On other hand the downsizing of components in CMOS IC provides improvement of gate delay [9] (see Figure 5). The total delay (gate and interconnect delay) is reduced while the scaling of feature size does not achieve of 0.25 µm technology. It may be the reason of partial compensation of logic levels degradation (in result of BF influence) and the increase of CMOS IC robustness (critical resistance values for 0.5 µm technology and 1.5 µm technology are not very different). Possibly the exact answer will be received from the results of circuit simulation for 0.18 µm technology. But this is the subject of our future research.

a)





b)

Figure 4. Logic swing (a) and logic margin (b) for 0.25 µm technology

Typically, reducing BF resistor value more than th[illegible] value results in a logic mistake and we accepted this va[illegible] as critical resistance.

Table 4. Critical resistance values for difference technologies and conditions (AC analysis method)

CMOS technology	Best Conditions	Normal Conditions	Worst Conditions
0.25 µm	900 Ω	1100 Ω	1800 Ω
0.35 µm	700 Ω	750 Ω	950 Ω
0.5 µm	470 Ω	580 Ω	690 Ω
1.5 µm	450 Ω	550 Ω	660 Ω

6. Future Research Directions

As we know, each process disturbance may cause a number of different changes in IC performance. And we call this change in behavior a fault. The performance faults can be divided into two classes: soft-performance faults and hard-performance faults.

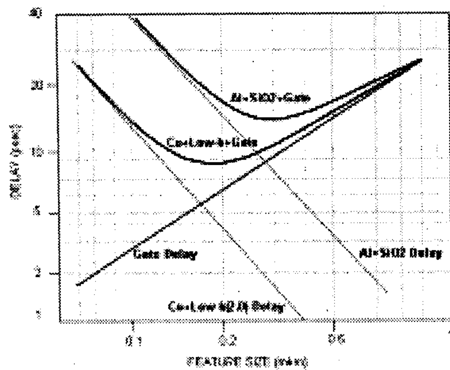


Figure 5. Gate and interconnect delay as a function of feature size: Cu+Low-k versus Al+SiO$_2$

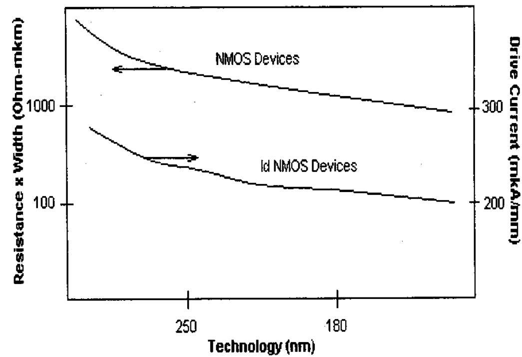


Figure 6. Resistance [11] and Drain current [12] variation of NMOS transistor under technology scaling

If IC is functionally correct but some performance measure lies outside the specified range, we say a soft-performance fault has occurred. If IC does not function properly (e. g. some state transition do not occur), we say a hard - performance fault has occurred. In our work we considered a bridging fault as a hard -performance fault, which influences the behavior of digital CMOS IC (D-flip-flops). In future, we are planning to consider the influence of BF defects within logic structure of ISCAS-85 benchmark circuits.

7. Conclusions

In this article we have shown that the sensitivity of CMOS IC to BFs is increased with the reduction of feature size of IC and voltage suppler and the increase of operating temperature. The Fig. 6 shows that resistance and drain current of transistor are reduced under the technology scaling. It means that voltage drop on transistors is reduced also and this increase of voltage drop on BF resistor, which is connected in series with NMOS and PMOS transistors. So the impact of BF defect on CMOS circuit parameters is increased. Because the critical resistance value of BF (the resistance above which the defect cannot be detected) is increased, as our research show, the problem of CMOS ICs testing becomes more complicated. This resistance depends on the maximum frequency that a given test can measure. Many tests run at a base test cycle frequency that is substantially less than the systems clock frequency. The defect's effect on normal circuit operation depends on its operating frequency; thus, the defect has another resistance (higher) associated with operating frequency. Unfortunately, bridges and most open circuit defects are not 100% detectable by I_{DDQ} or Boolean methods only. In our research we use the DC and AC (parametric) test method which can successfully supplement the existing test methods of BF in CMOS IS. Analysis of publications show unworthy attention of researchers to parametric test method with the exception of article [8] where authors described the Multidimensional Testing Paradigm (MTP) as useful method for BF testing. It defines the necessity and perspective of our research and this article.

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