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Impact of technology scaling on thermal behavior of leakage current in sub-quarter micron MOSFETs: perspective of low temperature current testing

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Abstract

The increase in the off-state current for sub-quarter micron CMOS technologies is making conventional I_{DDQ} testing ineffective. Since natural process variation together with low-V_{TH} devices can significantly increase the absolute leakage value and the variation, choosing a single threshold for I_{DDQ} testing is impractical. One of the potential solutions is the cooling of the chip during current testing. In this paper we analyze the impact of CMOS technology scaling on the thermal behavior of different leakage current mechanisms in *n*-MOSFETs and estimate the effectiveness of low temperature I_{DDQ} testing. We found that the conventional single threshold low temperature I_{DDQ} testing is not effective for sub-quarter micron CMOS technologies and propose the low temperature ΔI_{DDQ} test method. The difference between pass and fail current limits was estimated more than 200× for 0.13-μm CMOS technology. © 2002 Published by Elsevier Science Ltd.

Keywords: CMOS technology scaling; ΔI_{DDQ}Testing; Leakage current; Low temperature

1. Introduction and motivation

Current is a more effective parameter than voltage for defect detection in CMOS ICs, although both are necessary for complete testing. If ICs are properly designed and fabricated for low background current, then quiescent current testing (I_{DDQ}) is a relatively simple test technique with many benefits. Typically, I_{DDQ} testing is the effective test method for detection of gate oxide shorts, bridging faults and certain open-circuit defects [1,2]. However, with scaling of technology, a complex ICs may have several millions of transistors, then the total I_{DDQ}, which is the sum of all transistors' off current, will grow. The increase in transistor count and associated total junction leakage is not the main reason of higher leakage current. The primary cause of elevated off-state leakage is the lowering of transistor threshold voltage (V_{TH}) under technology scaling [3]. As a result, the sub-threshold (weak inversion) current is increased exponentially.

Different circuit and technology solutions have been proposed to contain the increased sub-threshold leakage and to keep the high effectiveness of I_{DDQ} testing for deep sub-micron CMOS technologies. These solutions include utilization of reverse body biasing (RBB) technique to reduce the sub-threshold leakage in the test mode [4–6], or utilization of multi-threshold transistors to contain the sub-threshold leakage [7]. However, these solutions have some limitations. For example, the effectiveness of RBB technique is diminished under technology scaling, because the body effect (γ) of deep sub-micron transistor is reduced with scaling of gate oxide thickness [8]. In addition, the impact of V_{TH} fluctuation due to process variation is higher in low V_{TH} MOS transistors than that in high V_{TH} MOS transistors [9]. A relatively small V_{TH} fluctuation in low V_{TH} MOS transistor results in a larger delay and leakage variations, and degradation of short channel effects (SCE). A comparative analysis of partially depleted SOI (PD-SOI) and bulk technologies have shown that the total energy consumption of SOI circuits can be reduced by ~30% for equal worst case delay in comparison with bulk circuits. However, this advantage of SOI over bulk is expected to reduce with technology scaling [6,10]. Besides, technology and circuit solutions, researcher tried to find test solutions for deep sub-micron I_{DDQ}. Several test techniques have been proposed to

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perform current measurements in high background leakage environment. Such techniques include, current signatures [11], Delta I_{DDQ}, transient current testing or I_{DDT} [12–14], and IR drop based I_{CCQ} test method [15].

In this article, we investigate the potential of I_{DDQ} testing using thermal properties of a MOS transistor. In weak inversion, diffusion is the dominant mechanism of charges transfer across the channel. Lower temperature reduces the rate of diffusion. Decreasing temperature from 22 to −55 °C reduces the off current by at least three orders of magnitude for a transistor with $V_{TH} = 0.3$ V [1]. Similar ideas were proposed by Williams et al. [16] to reduce the off state leakage. Szekely et al. [17] and Rencz et al. [18] extended the concept of low temperature I_{DDQ} testing as a means to increase the effectiveness of deep sub-micron current testing. In these investigations, current measurements on transistors of 0.25 and 0.35-μm were performed over −75 to 25 °C. The results of these investigations show that the off state leakage may be reduced by a factor 100–1000 depending on device feature size and operating conditions. At the circuit level, low temperature stand-by current testing was successfully used on 0.5-μm [19], and 0.20-μm [20] CMOS VLSIs. In Ref. [19] the current measurements were carried out at the room temperature and at −40 °C. The leakage current was reduced by a factor of 500 by lowering the temperature. Similarly, in Ref. [20] the measurements were carried out at the room and at −15 °C for a 0.20-μm microprocessor. The results show that leakage current is reduced to 1/3 of the original value.

The most of the previous investigations were performed for relatively long channel CMOS technologies. In this paper, we investigate the potential of low temperature I_{DDQ} testing for sub-quarter micron CMOS technologies and estimate the effectiveness of this test technique under technology scaling regime. Furthermore, the impact of ambient temperature reduction on different leakage current components of sub-quarter micron *n*-MOSFETs is analyzed in detail.

This paper is organized as follows. In Section 2, we present the device under test and discuss the possible ambient temperature conditions for current testing. The simulation results and the impact of ambient temperature reduction on different leakage mechanisms are analyzed in Section 3. In Section 4, the possible application of I_{DDQ} testing at reduced ambient temperature is discussed. The paper is concluded in Section 5.

2. Technology parameters

We simulated and analyzed the defect-free I_{OFF} current of *n*-MOS transistors implemented in three different CMOS technologies (0.35, 0.18 and 0.13-μm feature sizes), using a 2D device simulator, 'Microtec' [21]. In these simulations, the ambient temperature is changed from 127 to 0 °C. Table 1 illustrates the basic MOSFET parameters used for simulations. The results of these simulations (transistor DC characteristics) were compared with DC characteristics of silicon devices of the same technologies. The basic technology and electric parameters of analyzed MOSFETs were provided by several fabs.

As mentioned before, in our research, the operating temperature is changed from 400 K (127 °C) to 273 K (0 °C). The top limit of this interval is the typical temperature for burn-in testing [22]. Typically, a slow frequency test and leakage measurements are performed during the burn-in process. The role of burn-in is becoming crucial in sub-0.25-micron technologies owing to subtle defect mechanisms. The chosen lower temperature limit is somewhat arbitrary. However, our objective in this article to examine technology trends with scaling. Furthermore, there is some evidence that industry uses such temperature range in circuit operation and/or test [23,24].

3. Thermal impact on leakage components: simulation results

In our research, we segregated the total off current of analyzed MOSFETs on two groups:

Source–Drain current: it includes following leakage current components, (i) weak inversion (sub-threshold) current, (ii) punch-through current, and (iii) current due to DIBL effect.

Bulk (substrate) current: this component includes, (i) impact ionization effect, (ii) gate induced drain leakage (GIDL) current or surface band-to-band tunneling (BTBT) current, (iii) conventional *pn*-junction leakage and bulk BTBT current of *pn* junction.

Figs. 1 and 2 show the drain and bulk current components as a function of gate voltage for analyzed technologies. These plots confirm that the modeled MOSFETs are operating properly. Furthermore, the basic transistor parameters were extracted from these plots and were compared with the nominal parameters obtained from the fabs. This comparison is shown in Table 2.

We can observe the increase of drain current due to GIDL effect when the gate voltage is less than threshold voltage and high voltage is applied for the drain. This parasitic effect is increased with technology scaling and will discuss below.

3.1. Source-drain current

The simulation results of the source-to-drain current as a function of temperature are illustrated in Fig. 3 for analyzed technologies. It is apparent from the graph that the curves become increasingly flat as the technology is scaled. In other words, the temperature becomes less and less effective to reduce this leakage component. Secondly, this component is

Table 1
n-MOSFET parameters used for simulations

MOSFET Parameters	0.35-μm	0.18-μm	0.13-μm
Substrate doping (cm^{-3})	2×10^{15} (p type)	5×10^{15} (p type)	2×10^{16} (p type)
Source/Drain length (μm)	1.5	1.5	1.5
Source/Drain doping (cm^{-3})	9×10^{19} (n type)	2×10^{20} (n type)	6×10^{20} (n type)
V_{TH} adjusted doping (cm^{-3})	1.1×10^{18} (p type)	1.8×10^{18} (p type)	2×10^{18} (p type)
Anti-Punch-Through doping (cm^{-3})	4×10^{17} (p type)	5×10^{18} (p type)	3×10^{19} (p type)
L_{eff}/W (μm/μm)	0.24/5	0.13/5	0.06/5
Gate oxide thickness (Å)	65	41	32
Nominal V_{DD} (V)	3.3	1.8	1.2

increased significantly with technology scaling. In order to explain this tendency, we should consider the different leakage current components included in this group.

3.1.1. Weak inversion (sub-threshold) leakage current

Weak inversion or sub-threshold current between source and drain in a MOS transistor occurs when gate voltage is slightly smaller than V_{TH}. Weak inversion current typically dominates in modern device off-state leakage due to the low V_{TH} that is used in lower geometries. MOSFET SPICE model level 3 uses the following equation for sub-threshold current calculation [25]

$$I_{DS}\text{-OFF} = k\frac{W}{L}(\eta-1)V_t^2\exp\left[\frac{V_{GS}-VTH}{\eta V_t}\right]\left(1-e^{\frac{-VDS}{V_t}}\right) \quad (1)$$

where k is the process transconductance parameter ($k=\mu C_{ox}$, μ is the effective channel mobility, C_{ox} is the gate oxide capacitance); V_t is the thermal voltage, and η is a fitting constant (typical values of η range from 1 to 2 for sub-micron MOSFET). Since the threshold voltage is significantly reduced under technology scaling (Table 2), it results in the exponential increase in sub-threshold leakage (Eq. (1)). Furthermore, there are temperature dependent parameters in this equation influencing its thermal response. Mobility, μ, thermal voltage, V_t, and threshold voltage, V_{TH}, are temperature dependent parameters.

In the temperature range 200–400 K, the temperature dependence of low field mobility can be expressed as [25]

$$\mu(T) = \mu_0(300\text{ K})\left(\frac{T}{300\text{ K}}\right)^{-1.5} \quad (2)$$

This equation shows that the mobility is increased with lowering of temperature. The increased mobility should cause linear increase in weak inversion current. However, at the reduction in temperature, the V_{TH} is increased resulting in exponential decrease in weak inversion current. In our previous research, the temperature rate of change of threshold voltage under technology scaling was estimated

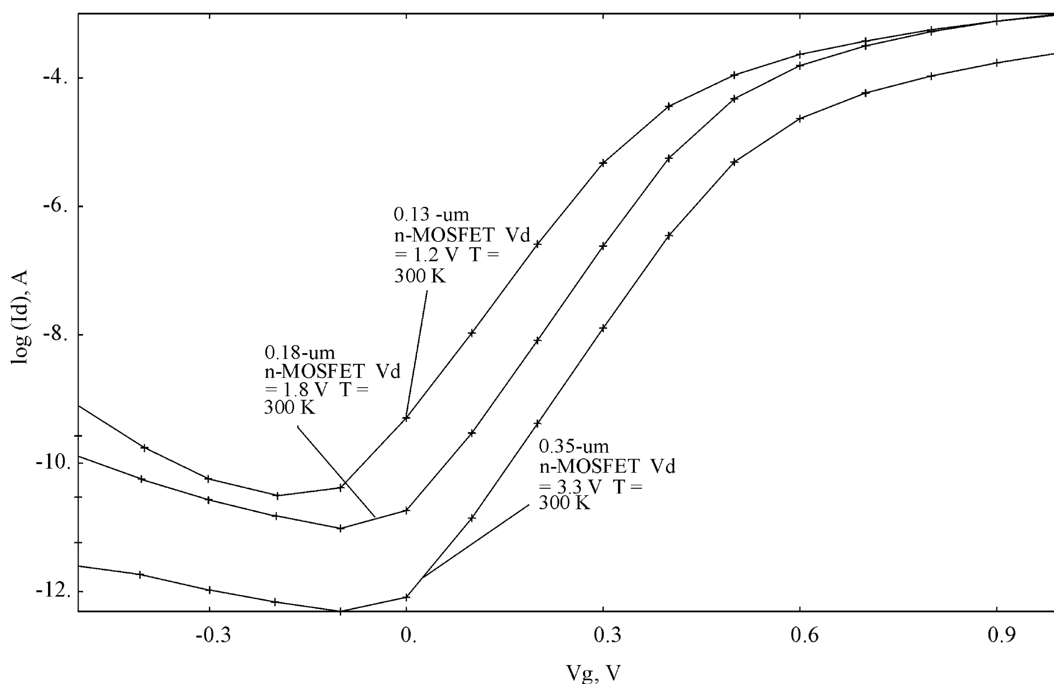

Fig. 1. Drain current vs. gate voltage (V) for different CMOS technologies ($T = 300$ K, drain voltage has the nominal value for the given technology).

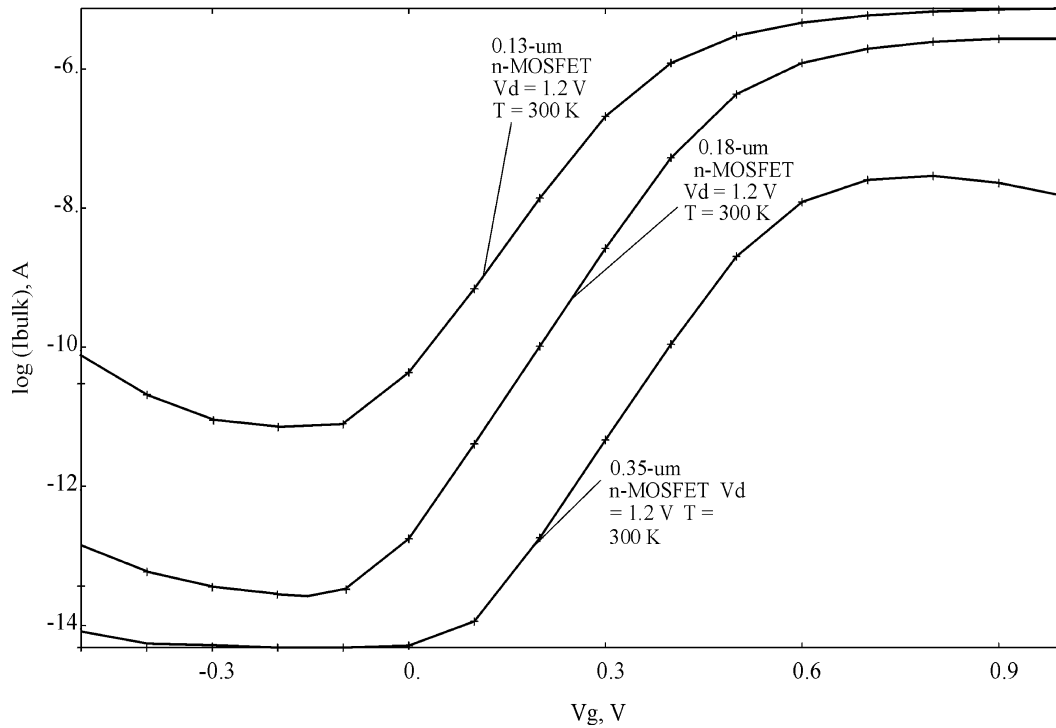

Fig. 2. Bulk (substrate) current vs. gate voltage (V) for different CMOS technologies ($T=300$ K, $V_D=1.2$ V).

[26]. It was found that $(dV_{TH}/dT)\approx -0.6$ mV/°C for 0.18-μm CMOS technology. However, long channel device has $(dV_{TH}/dT)\approx -2$ mV/°C for 2-μm CMOS technology [27]. Hence, the decrease of thermal sensitivity of threshold voltage under technology scaling is one of the major reasons of effectiveness decrease of weak inversion current reduction by cooling.

3.1.2. Punch-through leakage current

This current is between source to drain, and is due to a lowering of the source potential barrier at the channel surface under the influence of the applied gate bias. This corresponds to the situation when a MOSFET is on. When a MOSFET is off, this current travels beneath the surface under the influence of the applied drain voltage because of a 'punch-through' of the drain to source depletion layer [28]. When $V_{DS}\approx V_{DD}$ and $V_G=0$ V, the carrier concentration caused by the injection from the source becomes comparable to the channel doping concentration and the current becomes space charge limited (SCL). The basic expression for the SCL model current may be derived as [29]

$$I^0_{SCL}\approx \frac{9\epsilon_{si}\mu A}{8L^3}(V_{DS}-V^{SCL}_{DS})^2 \quad (3)$$

where μ is the channel mobility, A is the channel cross section, V^{SCL}_{DS} is the drain voltage at which the current is expected to become space-charge-limited and L is the channel length. Punch-through leakage current has a quadratic dependence on V_{DS}.

Punch-through leakage current is substantially reduced by the temperature lowering. This is due to the fact the punch-through current is mainly limited by the thermo-ionic emission over the barrier between source and drain. Hence, the thermal dependence of this current may be expressed by the model [30]

$$I_{\text{punch-through}}=I^0_{SCL}\exp\left(-\frac{\Phi}{kT}\right) \quad (4)$$

where Φ is the source-to-channel barrier height. Thus, the punch-through current is thermally activated and significantly reduces at low temperature. The simulation results in Fig. 4 confirm this conclusion. To minimize the weak inversion current and extract the bulk punch-through

Table 2
Extracted and nominal parameters of analyzed n-MOSFETs ($V_{bulk}=V_S=0$ V)

Parameters	0.35-μm	0.18-μm	0.13-μm
(Extracted/Nominal) V_{TH}, V ($V_{DS}=0.1$ V)	0.57/0.59	0.51/0.48	0.42/0.41
(Extracted/Nominal) Total I_{OFF} ($V_{DS}=V_{DD}$, $V_G=0$ V)	0.7/0.5 (pA/μm)	26/42 (pA/μm)	6.5/4 (nA/μm)
(Extracted/Nominal) I_{SAT}, mA/μm ($V_G=V_{DS}=V_{DD}$)	0.60/0.55	0.62/0.60	0.46/0.63

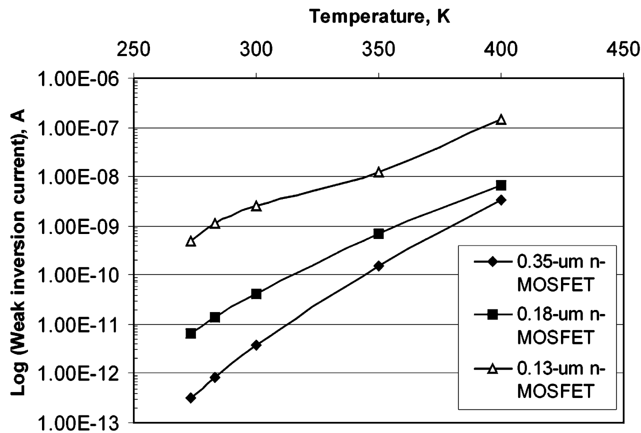

Fig. 3. Impact of technology scaling on weak inversion current as a function of temperature.

leakage current, a small negative voltage was applied for the gate terminal. Although, punch-trough current should increase under technology scaling (Eq. (3)), it can be successfully controlled using anti-punch-through doping (Table 1). Hence, the low temperature test may effectively reduce punch-through leakage current component.

3.1.3. Leakage current due to DIBL effect

For deep sub-micrometer MOSFETs, threshold voltage (V_{TH}) roll-off becomes the one of the main limitations. In the sub-threshold regime in short-channel devices, a drain voltage induces lowering of the energy barrier between the source and channel. This so-called drain-induced barrier lowering (DIBL) causes excess injection of charge carriers into the channel and gives rise to an increased sub-threshold current due to threshold voltage reduction. DIBL effect may be modeled as [31,32]

$$V_{TH} = V_{TH}^0 - \lambda_{DIBL} V_{DS} \tag{5}$$

where V_{TH}^0 is the threshold voltage at zero drain bias and λ_{DIBL} is the DIBL coefficient defined as

$$\lambda_{DIBL} = -\frac{\Delta V_{TH}}{\Delta V_{DS}} \tag{6}$$

Practically, the DIBL effect is defined as the vertical parallel shift of log (I_D) vs. V_G at a given drain voltage and elevated drain voltage in the sub-threshold regime, when V_G is grounded.

The published data indicate that the DIBL coefficient increases significantly as the channel length is reduced to the sub-quarter micron range [32,33]. As a result, the DIBL effect becomes more critical for these devices. The temperature dependence of DIBL effect in deep sub-micron MOSFETs was extensively investigated in literature. It was found that the DIBL coefficient is nearly insensitive to temperature reduction in the temperature interval from 300 to 50 K [34]. Our previous research shows that the DIBL coefficient may be increased (~2.5×) under temperature reduction from 150 to 25 °C [26]. The same tendency was observed in Ref. [32]. Hence, DIBL effect remains a serious issue for deep sub-micron MOSFETs even under cryogenic conditions, since it cannot be minimized by temperature reduction.

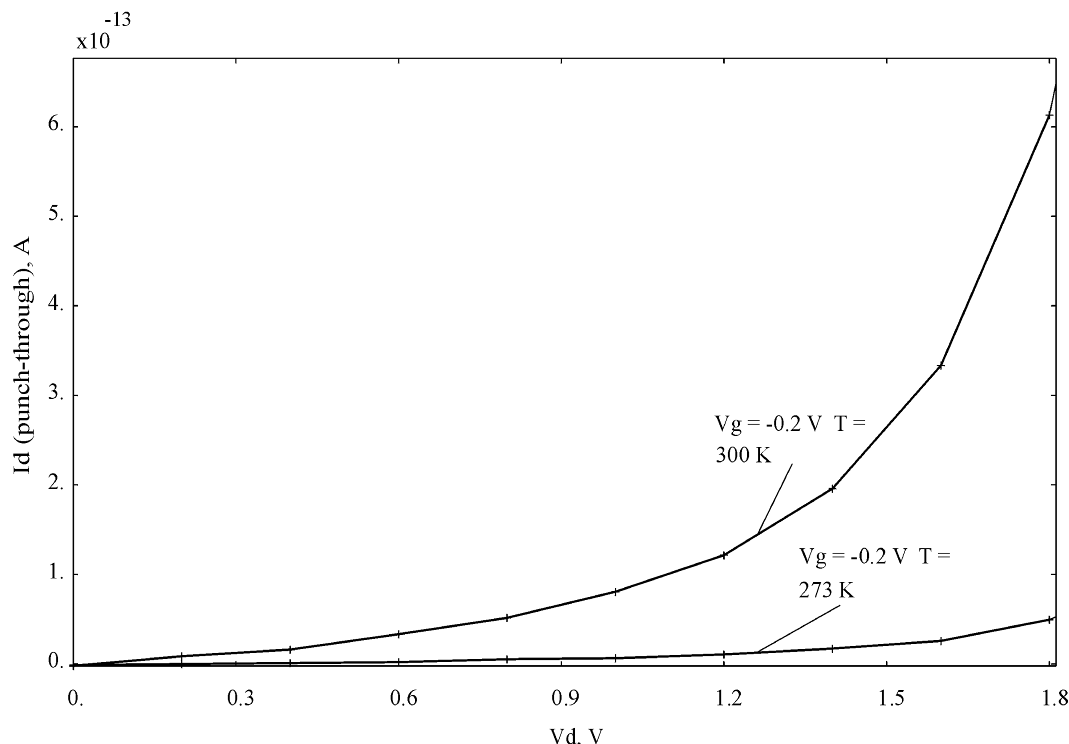

Fig. 4. Punch-through current vs. drain voltage (V) for different temperatures (0.18-μm n-MOSFET).

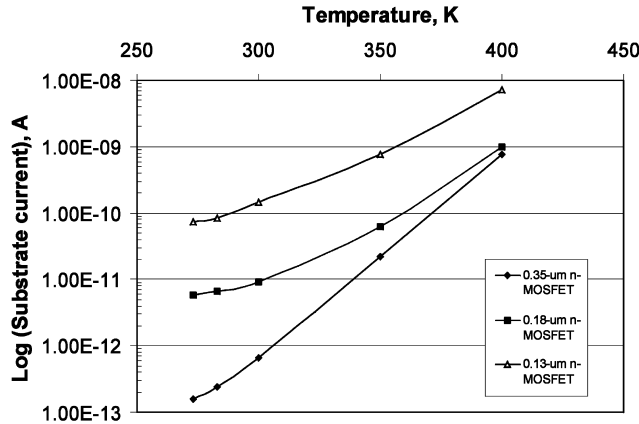

Fig. 5. Impact of technology scaling on substrate leakage current as a function of temperature.

3.2. Bulk (substrate) current

In this section we consider bulk leakage current due to (i) impact ionization effect, (ii) gate induced drain leakage (GIDL) current or surface BTBT current, (iii) conventional *pn*-junction leakage and bulk BTBT current of *pn* junction. These leakage components are included in a total bulk leakage current of analyzed transistors. The simulation results of impact of technology scaling and temperature reduction on the total substrate leakage are presented in Fig. 5.

This current component exhibits similar tendencies with that of drain–source current component. From Fig. 6, we can conclude that the substrate leakage current is significantly increased with technology scaling. Furthermore, the temperature dependence of this component is also reduced for scaled transistor. In order to explain these conclusions we should consider the impact of technology scaling and temperature reduction on the different components of bulk current.

3.2.1. Leakage current due to impact ionization effect

The impact ionization becomes more important as the channel length of MOSFETs devices is reduced into the deep sub-micron region. The increase of the electric field near the drain region and the increase of current density going through the high field region are key issues for sub-quarter micron devices. The generation hole current due to impact ionization leads to significant increase in substrate current. The analytical model of impact ionization current in weak inversion (sub-threshold) mode was proposed in Ref. [35]. This model is valid at gate voltage below V_{TH} and at drain voltage close to V_{DD}.

$$I_{\text{imp-ioniz}} = I_{ch}\frac{A_i}{B_i}V_{DS}\exp\left(\frac{-l_d B_i}{V_{DS}}\right) \tag{7}$$

Where I_{ch} is the channel current at sub-threshold region (Eq. (1)), A_i and B_i are impact ionization rate parameters and l_d is the characteristic length, which can be used as an adjustable parameter. Because the channel current is significantly increased under technology scaling, the substrate leakage component due to impact ionization is increased as well. This tendency was confirmed in Ref. [36].

The temperature dependence of impact ionization current on temperature was studied in Refs. [30,37,38]. It was found that the substrate current due to impact ionization is almost temperature independent in temperature interval from 300 to 77 K. Even though the electron–phonon scattering is reduced with temperature, the phonon generation remains largely the same. Furthermore, the impurity scattering is enhanced at low temperature [38]. Although, the channel current in Eq. (7) is reduced with the reduction in temperature, the coefficient A_i is monotonously increased as the temperature is lowered and the constant B_i is almost temperature independent [30]. Hence, this component is largely temperature independent from 300 to 77 K.

3.2.2. Surface and bulk band-to-band tunneling (BTBT) current

The surface BTBT current or gate-induced drain leakage (GIDL) current is due to the potential difference applied between drain and gate. When drain is biased at V_{DD} and gate is grounded, *n*-MOSFET is operating in off-mode. A strong depletion region is therefore formed under the gate-to-drain overlap region. The presence of a gate-induced high electric field causes twisting of energy bands. Hence, minority charge carriers can tunnel from one energy band to another. These minority carriers are transferred by the BTBT from the valence band to conduction band of silicon. The tunneling electrons flow into the drain; the holes created by the valence-band electrons flow into the substrate. The simple 1D BTBT current density model was presented in Ref. [39]

$$J_{GIDL} = A{\cdot}E_s \exp(-B/E_s) \tag{8}$$

where $B \approx 21.3$ MV/cm, and $E_s = (V_{dd} - E_g)/3T_{ox}$ is the transverse electric field at the silicon surface. E_g is the band bending potential (1.12 eV), which is the minimum necessary energy for BTBT to occur. A is the pre-exponential constant. Although, the supply rail voltage is reduced under technology scaling, the increase of operating temperature and doping concentration, and decrease of gate oxide thickness cause an increase of GIDL current in sub-quarter micron MOSFETs.

The temperature dependence of GIDL was studied in Ref. [40] in the temperature interval from 300 to 20 K. It was found that GIDL is a weak function of temperature. This current is monotonously decreased as the temperature is lowered. This is because the constant *A* is monotonically decreased. The exponential coefficient *B* is almost constant with temperature reduction.

The other major component of substrate leakage current in deep sub-micron MOSFET is the bulk BTBT current through the drain junction. The junction-tunneling current density depends on the substrate doping concentration

(N_{sub}), which must be increased to avoid punch-through current as device dimensions are decreased. The worst case of maximum electric field in the drain junction is defined by the supply voltage (V_{DD}) plus the built-in voltage (V_B):

$$E_{max} = \sqrt{\frac{2qN_{sub}(V_{DD} + V_{bi})}{\varepsilon_{Si}}} \quad (9)$$

The bulk tunneling current density as a function of the maximum electric field was obtained in Ref. [41], using the step-junction approximation and the junction built-in voltage $V_{bi} \approx 1.1$ V

$$J_{bulk\text{-}BTBT} \approx G_0 \cdot V_{DD} \frac{E_{max}}{E_0} \exp(-E_0/E_{max}) \quad (10)$$

where $E_0 = 2.9 \times 10^7$ V/cm and the pre-exponential factor is $G_0 = 3 \times 10^9$ A/(V cm^2). Because of the exponential dependence, $J_{bulk\text{-}BTBT}$ increases vary rapidly with the electric field E_{max}.

In our research, we extracted the GIDL and bulk BTBT current components from the simulation results of a total substrate leakage current for different CMOS technologies and temperature. The obtained results are presented in Fig. 6. From this figure, we can conclude that these leakage components are the weak function of temperature and significantly increased under technology scaling.

3.2.3. Conventional pn-junction leakage

The leakage current of *pn* junctions is one of the main parameters affecting the performance of devices such as dynamic random access memories (DRAM), charge coupled devices (CCDs) and integrated circuits (ICs) implemented with dynamic logic. The *pn*-junctions leakage current consists of three components, namely: diffusion, generation, and surface generation components [42].

The diffusion current is caused by electron-hole pair generation in the doped regions. The Shockley model of diffusion component is given as:

$$J_{diff,n} = qD_n \frac{n_i^2}{N_A L_n}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (11)$$

where q is the electron charge, D_n is the diffusion constant of electrons, n_i is the intrinsic carrier density, N_A is the acceptor density, and L_n is the diffusion length of electrons.

The generation current is caused by generation of electron-hole pairs in the depletion region and can be modeled as:

$$J_{gen} = q\frac{n_i}{\tau_g} W\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (12)$$

where τ_g is the generation lifetime and W is the depletion width.

Similarly the surface generation current is caused by electron-hole pair generation in the depletion region at the Si/SiO$_2$ interface, and can be described as:

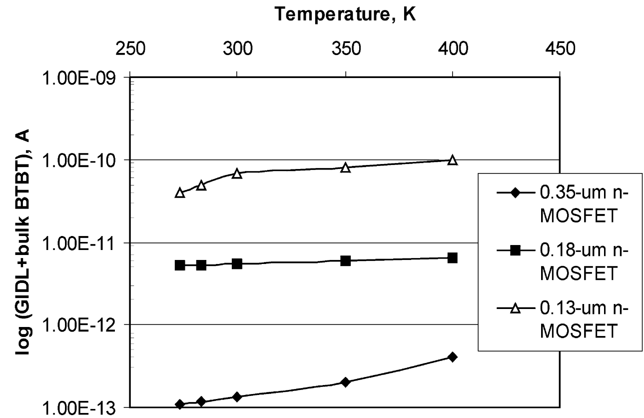

Fig. 6. GIDL and bulk BTBT currents as a function of technology scaling and temperature.

$$J_{surf\text{-}gen} = qS_0 n_i W_S\left[\exp\left(\frac{qV}{kT}\right) - 1\right]\frac{L}{A} \quad (13)$$

where S_0 is the surface recombination velocity and W_S is the depletion width at the Si/SiO$_2$ interface, L is the perimeter length of the junction, and A is the junction area.

From Eqs. (11–13) we can conclude that conventional *pn*-junction leakage current components are decreased exponentially with linear temperature reduction. Furthermore, this component will be reduced with technology scaling due to increased substrate/well and junction doping as well as due to reduced transistor geometries.

As it is apparent from the discussion in this subsection, the surface and bulk BTBT current component, and conventional *pn*-junction leakage current component are reduced with temperature. The impact ionization current component is largely independent of temperature. Fig. 5 illustrates the overall substrate leakage behavior with temperature.

4. Perspective of low temperature current testing

The simulation results of leakage current obtained for different CMOS technologies in temperature interval from 127 °C (400 K) to 0 °C (273 K) are summarized in Table 3. In this table, we estimate the effectiveness of temperature reduction during I_{DDQ} testing as a relative leakage current decrease at high and low temperatures.

The obtained results show that the effectiveness of

Table 3
Effectiveness of Source–Drain (S–D), substrate (sub) and total leakage currents reduction at temperature decrease for different CMOS technologies

Leakage currents ratio	0.35-μm	0.18-μm	0.13-μm
I_{S-D} (127 °C)/I_{S-D} (0 °C)	11,000	1,300	250
I_{sub} (127 °C)/I_{sub} (0 °C)	4,500	129	112
I_{tot} (127 °C)/I_{tot} (0 °C)	9,500	692	227

conventional low-temperature current testing proposed in Refs. [17,18] is significantly degraded with technology scaling. The temperature reduction alone in sub-0.25-micron technologies may not be enough to reduce the leakage below traditional I_{DDQ} limits (e.g. 10–100 μA.). Note that the sensitivity of substrate current to temperature reduction is essentially decreased under technology scaling. This is because GIDL and bulk BTBT currents are significant leakage mechanisms in substrate current of sub-quarter micron MOSFETs.

One of the possible solutions, which can increase the effectiveness of low-temperature current testing is ΔI_{DDQ} testing or low-temperature stand-by current screening (LTSC). This technique uses the different temperature dependence between the normal (defect-free) and abnormal leakage current [19]. Shimaya has shown that the activation energies for an abnormal leakage as a result of soft *pn* junction, MOSFET with broken gate oxide and sub-threshold leakage degradation are less than 0.1 eV, while normal leakage currents have higher activation energy values (~0.4–0.8 eV). This difference suggests that lowering the temperature increases the difference between the normal and the abnormal current levels. Typically, good devices may show the significant leakage current reduction as temperature decreases, while the bad devices will exhibit the weak dependence on temperature.

However, LTSC technique has the significant limitations for sub-quarter CMOS technologies. For example, if we want to reduce the bulk leakage current ~100 times for reliable pass/fail current threshold, we should reduce the testing temperature from room temperature to about −100 °C, because ΔT must be ~125–127 °C (Table 3). It is not easy to find the industrial equipment for this low temperature testing. For example, a thermoelectronic cooling is an optimal method for refrigeration that does not require the use of cryogenic gas or liquids, and therefore is an inexpensive method. However, the minimum cold temperature for this method is approximately −60 °C [43].

For high reliable sub-quarter micron CMOS VLSI, we propose to modify the LTSC test method: to perform current measurement at temperature 125–127 °C at the first step and then repeat the measurement at close to 0 °C at the second step. For defect-free chips we can expect the reduction of leakage current at least >200 times as shown by our simulation results (Table 3). To increase the reliability of low temperature ΔI_{DDQ} testing, the interval between pass and fail current levels should be increased. For this purpose, the low temperature ΔI_{DDQ} testing may be combined with some special techniques for defect-free background leakage current reduction, such as dual (multi-)-threshold technology [7,20] and vector control technique [44]. In a dual-V_{TH} technique, a higher threshold voltage can be assigned to some transistors in non-critical path so as to reduce leakage current, while the performance is maintained die to the low-threshold transistors in the critical path. Therefore, no additional transistors are required, and both high and performance and low power can be achieved simultaneously. It has been shown in Ref. [44] that defect-free leakage current can be reduced by more than 80% using dual-V_{TH} technique.

For each logic gate, the quiescent current depends on its input combinations. This makes the total leakage current of a circuit dependent on primary inputs. Hence, applying best-input vectors to some circuits can reduce the leakage current significantly. This is the principal idea of vector control technique, which can reduce the defect-free background leakage current by more than 50% for some CMOS benchmark circuits [44,45]. Hence, the low temperature ΔI_{DDQ} testing should be implemented at the best-input vectors for effective background leakage current reduction.

5. Conclusion

The scaling of device threshold voltage due to the scaling of supply voltage makes the defect-free I_{DDQ} current increase dramatically, threatening the feasibility of current testing for such low-voltage VLSI CMOS circuits. As designs grow larger and denser, the background current is expected to increase. Therefore, making it more difficult to screen marginal devices from good dies by I_{DDQ} testing. In this paper we analyzed the potential of low temperature I_{DDQ} testing, which may overcome the limitations of conventional I_{DDQ} testing. The impact of technology scaling and temperature reduction on the different leakage mechanisms of sub-quarter micron MOSFETs is investigated. On the basis of device simulation results and previous published data, the following conclusions are obtained for individual leakage current components:

(1) The absolute value of the sub-threshold leakage current is significantly increased with technology scaling. This component is reduced with reduction in temperature. However, the rate of leakage reduction with temperature is diminished with technology scaling. Note that the sub-threshold leakage current is the dominant leakage mechanism.
(2) Punch-through leakage current is increased with technology scaling, however, it can be significantly reduced by cooling and by anti-punch-through implantation.
(3) Leakage current due to DIBL effect is increased with scaling and is almost insensitive to the temperature.
(4) Impact ionization leakage current is increased with technology scaling and it is almost temperature independent in temperature interval from 300 to 77 K.
(5) GIDL and bulk BTBT currents are significantly increased with technology scaling and are almost temperature independent. These two components of substrate leakage current are the main obstacle for effective application of low temperature I_{DDQ} testing.
(6) Conventional *pn*-junction leakage is reduced by

cooling. This is the main reason of bulk leakage current reduction at reduced temperature.

The difference between pass and fail current limits should be increased as much as possible for reliable sub-quarter micron CMOS VLSI. The simulation results show that the total leakage current of 0.13-μm *n*-MOSFET may be reduced by more than 200× by cooling from 127 to 0 °C. For sub-quarter micron CMOS technologies we propose the low temperature ΔI_{DDQ} testing: $\Delta I_{DDQ} = I_{DDQ}(127\ ^\circ C) - I_{DDQ}(0\ ^\circ C)$. For defect-free chips this current difference should be more than two orders of magnitudes.

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