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Leakage Current in Sub-Quarter Micron MOSFET: A Perspective on Stressed Delta I_{DDQ} Testing

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Abstract. The effectiveness of single threshold I_{DDQ} measurement for defect detection is eroded owing to higher and more variable background leakage current in modern VLSIs. Delta I_{DDQ} is identified as one alternative for deep submicron current measurements. Often delta I_{DDQ} is coupled with voltage and thermal stress in order to accelerate the failure mechanisms. A major concern is the I_{DDQ} limit setting under normal and stressed conditions. In this article, we investigate the impact of voltage and thermal stress on the background leakage. We calculate I_{DDQ} limits for normal and stressed operating conditions of 0.18 μm n-MOSFETs using a device simulator. Intrinsic leakage current components of transistor are analyzed and the impact of technology scaling on effectiveness of stressed ΔI_{DDQ} testing is also investigated.

Keywords: CMOS integrated circuits, I_{DDQ} testing, quality, reliability, MOSFET leakage

1. Introduction and Review

The problems with current based test methods for deep sub-micron VLSIs are well known and well documented [1, 2]. The increased background leakage current and it variability of deep submicron devices threatens the practical application of the traditional I_{DDQ} testing. Recent projections suggest this leakage is expected to increase even further with the scaling [3]. Technology scaling results into two specific problems: (i) the increased background leakage amplitude also results into a larger variance or spread of I_{DDQ} distribution. As a result, setting pass/fail thresholds becomes increasingly difficult. (ii) detection of subtle defects becomes difficult in high background leakage environment.

Several solutions were suggested to perform effective current measurement in scaled geometries. Gattiker and Maly suggested that if I_{DDQ} vectors are sorted in ascending order, the presence of a discontinuity in quiescent current level indicates a defect [4]. A defective IC may have a different current signature compared to the one with no defect. They argued that the background leakage is not important. However, the underlying assumption is that a defect will cause enough leakage resulting in the discontinuity. Thibeault extended the concept of the current signature. He computed vector to vector difference in I_{DDQ} [5]. He called this delta I_{DDQ} technique and defined it as:

$$\Delta I_{DDQ}(i) = I_{DDQ}(i) - I_{DDQ}(i-1) \qquad (1)$$

where $I_{DDQ}(i)$ is the I_{DDQ} measurement at test vector i. From these differences in I_{DDQ} vectors, Thibeault computed the ΔI_{DDQ} distribution mean and variance. A probabilistic framework helped him compare the

probability of making a false decision based on I_{DDQ} and ΔI_{DDQ}. Thibeault applied this technique to Sematech data and demonstrated that the probability of making a false decision decreased by approximately two orders of magnitude. Miller also demonstrated the effectiveness of ΔI_{DDQ} [6]. He applied the ΔI_{DDQ} test technique on 100 SRAM and 197 Pentium microprocessor dies in wafer sort. The I_{DDQ} mean and standard deviation for SRAMs were 2.3 mA and 1.4 mA. Miller set the three-sigma pass/fail limit at 6.6 mA, and seventeen SRAM dies failed. Subsequently, he tested SRAMs with the ΔI_{DDQ} test technique. The mean and standard deviation were 43 μA and 94 μA. Miller set the pass/fail limit at 330 μA. Using this technique, thirteen devices failed, out of which 10 were common failures with the traditional I_{DDQ} test. Interestingly, the ΔI_{DDQ} test method did not catch 4 DC short failures (current $>$ 400 mA). This is understandable, since the difference between two current measurements was small. These failures were strong leakage failures and simple leakage I_{DDQ} measurements should fail these devices. Recently, delta I_{DDQ} testing was proposed for screening defective early fail IC parts due to points defects, which cause the small current increase and can be masked by increased chip background current [7].

These approaches, though effective, face measurement and instrumentation challenges. You must measure a precise value of I_{DDQ} for each vector. This method takes longer than comparing measured current values against a single threshold. Furthermore, current signature levels should be distinguishable beyond the measurement inaccuracies and noise.

2. Motivation

Despite instrumentation challenges, the delta I_{DDQ} technique can potentially perform current testing in high leakage environment [8, 9]. In this article, we explore the potential of stressed delta I_{DDQ} testing for high background leakage environment. The delta can be defined in several different ways, delta over test vectors, delta over voltage stress, and delta over thermal stress. The estimations of I_{DDQ} were carried out under nominal voltage and temperature conditions using 2-D device simulator. Subsequently, these simulations were repeated under stressed conditions. If these leakage estimations differed from pre-specified limits then a die was considered to be defective and was rejected.

The important question in these measurements is the appropriate delta value of current between nominal and stressed conditions. The outgoing quality of a given product is a function of delta current value. In this article, we investigate impact of voltage and thermal stress on the background leakage. We calculate these limits for normal and stressed operating conditions of 0.18 μm n-MOSFET and hypothetical single VLSI die using device simulator. Intrinsic leakage current components of transistor are analyzed. Furthermore, the impact of technology scaling on effectiveness of stressed ΔI_{DDQ} testing is also investigated.

3. Stressed Delta I_{DDQ} Testing: Concept and Measurement Technique

Conventional I_{DDQ} testing in deep submicron CMOS circuits is limited by the sub-threshold leakage current in MOS transistors. The cause of these leakage currents is the MOSFET threshold voltage reduction as a result of CMOS technology scaling. Table 1 compares MOSFET leakage current (I_{OFF}), threshold voltage (V_{TH}), power supply voltage (V_{DD}), gate oxide thickness (T_{OX}) and effective channel length (L_{eff}) for various technologies optimized for high performance applications and shows the increased leakage of smaller size in submicron transistors [10]. The data were obtained at room temperature.

In this paper, the ΔI_{DDQ} calculation was taken at stressed conditions (high operating voltage and temperature) and normal operating conditions (Eq. (2)). The test vector used for these measurements was the same.

$$\Delta I_{DDQ} = I_{DDQ}(V^1, T^1) - I_{DDQ}(V^0, T^0) \quad (2)$$

where, $I_{DDQ}(V^0, T^0)$ is the leakage current at nominal power supply and temperature and $I_{DDQ}(V^1, T^1)$ is leakage current at stressed conditions. I_{DDQ} is a

Table 1. Comparison of CMOS technologies [10].

Technology (μm)	V_{DD} (V)	T_{OX} (nm)	V_{TH} (V)	L_{eff} (μm)	I_{OFF} (pA/μm)
1.0	5	20	N/A	0.80	4.1E-4
0.8	5	15	0.60	0.55	5.8E-2
0.6	3.3	8	0.58	0.35	0.15
0.35	2.5	6	0.47	0.25	8.9
0.25	1.8	4.5	0.43	0.15	24
0.18	1.6	3	0.40	0.10	86

strong function of environmental conditions. Soden demonstrated the strong dependence of I_{DDQ} of failed circuits on temperature and voltage stress condition [11]. In this research 256 K SRAM circuits implemented in 0.5 um CMOS technology were tested under normal ($T = 25°C$, $V_{DD} = 3.3$ V) and stressed conditions ($T = 125°C$, $V_{DD} = 5.5$ V). It was found that the I_{DDQ} of individual ICs is approximately increased ten times under stressed temperature in comparison with normal operating temperature and the same V_{DD}.

4. Submicron MOSFET Leakage Current Mechanisms under Stressed Conditions: Simulation Results

The defect-free I_{DDQ} current of a static CMOS circuit is caused by the leakage current. Different physical phenomena contribute to this leakage. Depending on the physical phenomena causing the leakage these currents may be grouped in a several classes [12]:

(1) Tunneling leakage current through the gate oxide
(2) Subthreshold leakage current (weak inversion)
(3) Bulk punch-through leakage current
(4) Leakage current produced by drain-induced barrier lowering (DIBL) effect
(5) Reverse biased *pn* junction (drain-to-substrate) leakage current
(6) Gate induced drain leakage (GIDL) current

We analyzed these leakage current components of an n-MOSFET using the 2-D device simulator "Microtec" [13]. MOSFET parameters that were used for simulations, are given in Table 2.

These parameters allowed us to obtain the electric characteristics of modeled MOSFET corresponding to 0.18 μm CMOS technology. The nominal V_{DD} and threshold voltage for 0.18 μm CMOS technology are 1.8 V and 0.47 V respectively. These data were provided by the Taiwan Semiconductor Microelectronic Corporation (TSMC), which optimized this technology for high performance logic. The leakage current components are described in detail as functions of V_{DD} and temperature.

Table 2. *n*-MOSFET parameters used for simulations.

Substrate doping, cm^{-3}	5×10^{15} (*p*-type)
Source/Drain doping, cm^{-3}	1×10^{20} (*n*-type)
V_{TH} adjusted doping, cm^{-3}	1.8×10^{18} (*p*-type)
Punch - Trough doping, cm^{-3}	5×10^{18} (*p*-type)
L_{eff}/W, μm/μm	0.13/5
Gate oxide thickness, Å	41

4.1. *Tunneling Leakage Through the Gate Oxide*

Sufficient control of the surface potential with scaled down gate voltage requires that the gate oxide becomes thinner. Tunneling through ultra thin oxide produces the leakage current. Two physical mechanisms are identified. For thick oxides ($t_{ox} \sim$ 30–100 Å) the current is controlled by Fowler-Nordheim tunneling, while for thin oxides ($t_{ox} \leq 30$ Å) at voltage below about 3 V the current is due to direct quantum-mechanical tunneling [14]. Experiments shows that the gate oxide direct tunneling leakage current is significant when the gate oxide thickness is $\leq$30 Å at $V_{DD} \sim 2.5$ V [15]. For the 0.18 μm CMOS technology used in TSMC, the gate oxide thickness was $\sim$41 Å. Hence, we neglected the gate oxide leakage current in this paper. However, the oxide tunneling current may be a dominant leakage mechanism for the thinner oxides [10].

4.2. *Subthreshold (Weak Inversion) Leakage Current*

Weak inversion or subthreshold current between source and drain in a MOS transistor occurs when gate voltage is below V_{TH}. The carriers diffuse in a similar way as in the base region of bipolar transistor. Weak inversion current typically dominates the off-state leakage of modern devices due to the low V_{TH}. MOSFET SPICE model level 3 uses the following equation for subthreshold current calculation [16]

$$I_{DS\text{-}OFF} = k\frac{W}{L}(\eta - 1)V_t^2 \exp\left[\frac{V_{GS} - V_{TH}}{\eta V_t}\right]\left(1 - e^{\frac{-V_{DS}}{V_t}}\right) \quad (3)$$

Where k is the process transconductance parameter ($k = \mu C_{ox}$, μ is the effective channel mobility, C_{ox} is the gate oxide capacitance); V_t is the thermal voltage, and η is a fitting constant (typical values of η range from 1 to 2 for submicron MOSFET). The temperature dependent parameters are mobility, thermal voltage, and threshold voltage. We simulated the degradation of threshold voltage from temperature and voltage stress (Fig. 1). For threshold voltage calculation, we used the

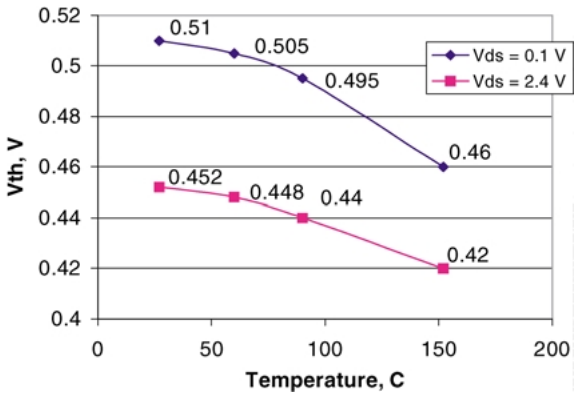

Fig. 1. Threshold voltage of n-MOSFET as a function of temperature.

conventional square root extraction method, when the threshold voltage is extracted by linear extrapolation of $(I_{DS})^{1/2} - V_G$ curve in the ON region to $I_{DS} = 0$.

The threshold voltage degradation is 12% when operating temperature is increased from 25°C to 150°C. The subthreshold or weak inversion current was obtained as a function of temperature and V_{DD} from the simulations is presented in Fig. 2.

The analyzed n-MOSFET had a subthreshold leakage current ~0.5 nA at $V_{DD} = 1.8$ V and $T = 25$°C (nominal operating conditions) and ~90 nA at $V_{DD} =$ 2.4 V and $T = 150$°C (stressed operating conditions). This current includes the following components: weak inversion current, bulk punchthrough current, and current due to the drain-induced barrier-lowering (DIBL) effect. These components could not be separated in the simulations. However, the bulk punchthrough current and DIBL effect were analyzed analytically as follows.

4.3. Bulk Punchthrough Leakage Current

Punchthrough in MOS transistors is a significant obstacle for microelectronics miniaturization scaling. This current goes from source to drain, due to a lowering of the source potential barrier at the channel surface under the influence of the applied gate bias. This corresponds to the situation when a MOSFET is on. When a MOSFET is off, this current goes beneath the surface under the influence of the applied drain voltage because of a "punchthrough" of the drain to source depletion layer [17].

In the off-mode, the punchthrough current may be described as follows. For small V_{DS}, the minimum potential of the electric field is located close to the middle of the gate, because the source and drain potentials have comparable magnitude. Increasing V_{DS} shifts the minimum potential towards the source and reduces the source potential barrier and so that the drain to source current is increased. This current is the bulk

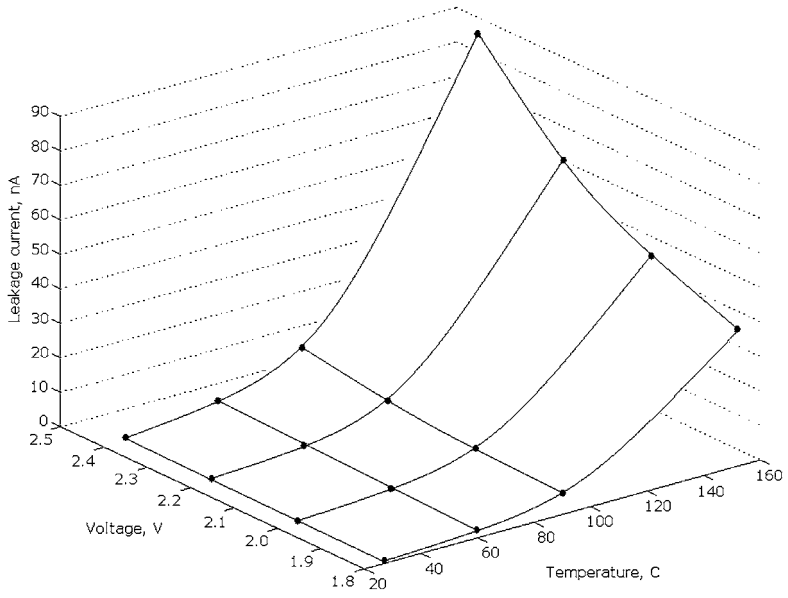

Fig. 2. The subthreshold current as a function of temperature and V_{DD}.

punchthrough current. For large V_{DS} the carrier concentration caused by the injection from the source becomes comparable to the channel doping concentration and the current becomes space charge limited (SCL). The basic expression for the SCL model current may be derived as [18]

$$I_{SCL} \approx \frac{9\varepsilon_{si}\mu A}{8L^3}\left(V_{DS} - V_{DS}^{SCL}\right)^2 \tag{4}$$

Where μ is the channel mobility, A is the channel cross section, V_{DS}^{SCL} is the drain voltage at which the current is expected to become space-charge-limited, and N_d is the source/drain doping.

$$V_{DS}^{SCL} = \frac{2}{k_d}\frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) \tag{5}$$

$$k_d = \frac{\varepsilon_{si}/L}{\eta C_{ox}} \tag{6}$$

η is a geometry-dependent fitting parameter.

The bulk punchthrough leakage current has a quadratic dependence on V_{DS} (Fig. 3). From the simulation data we found the gate voltage when bulk punchthrough leakage current is dominant. This voltage is $V_{GS} = -0.3$ V. For more negative gate voltages, the drain-to-source leakage current is reduced insignificantly at the given V_{DS}. We can neglect the weak inversion component of drain-to-source leakage current in the SLC mode.

The estimated values of bulk punchthrough leakage current are 2×10^{-13} A for nominal operating mode ($V_{DD} = 1.8$ V and $T = 25°C$) and 4.9×10^{-9}A for stressed operating mode ($V_{DD} = 2.4$ V and $T = 150°C$).

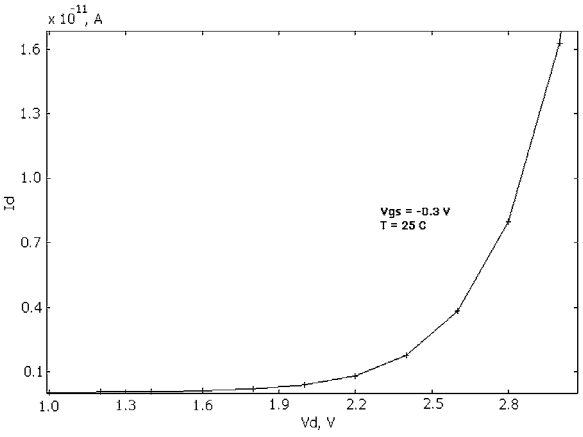

Fig. 3. Bulk punchthrough leakage current as a function of V_{dd}.

4.4. *Drain-Induced Barrier Lowering (DIBL) Effect*

The threshold voltage is strongly dependent on the potential distribution function under the gate and tends to decrease with the decrease of channel length. For submicron transistors, the threshold voltage is known to decrease linearly with the increase of drain voltage [19]. The main mechanism that reduces the threshold voltage is the decrease of the potential barrier in the depletion region under the gate due to the drain voltage. This is the Drain Induced Barrier Lowering (DIBL) effect. The threshold voltage degradation model due to DIBL effect may be described as

$$V_{TH} = V_{TH}^0 - \lambda_{DIBL} V_{DS} \tag{7}$$

Where V_{TH}^0 is the threshold voltage at zero drain bias and λ_{DIBL} is the DIBL coefficient defined as

$$\lambda_{DIBL} = -\frac{\Delta V_{TH}}{\Delta V_{DS}} \tag{8}$$

The change of threshold voltage at different applied drain bias and operating temperatures is shown in Fig. 4.

The DIBL coefficient was extracted from the data of Fig. 4 and presented as a function of temperature in Fig. 5. The temperature dependence of the DIBL coefficient was analyzed in [19]. It was observed that the DIBL coefficient decreases with increasing temperature. This behavior can be explained in terms of

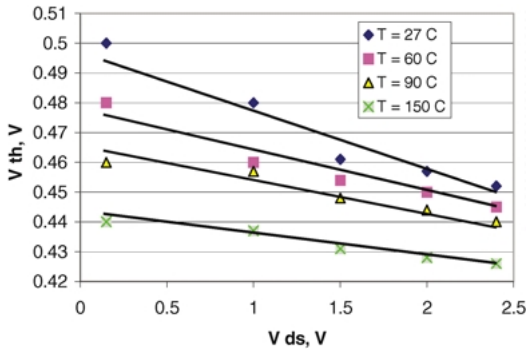

Fig. 4. The variation of threshold voltage with applied drain bias and operating temperature.

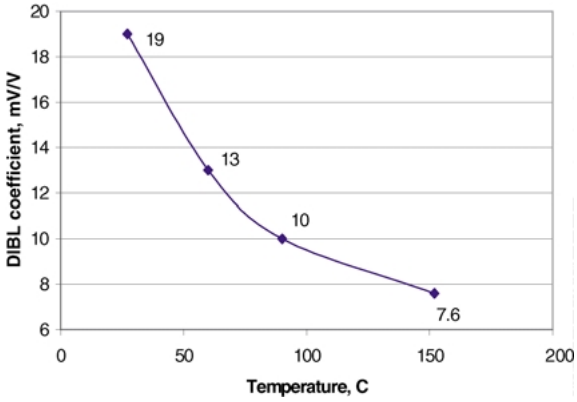

Fig. 5. DIBL coefficient vs. operating temperature for 0.18 um *n*-MOSFET.

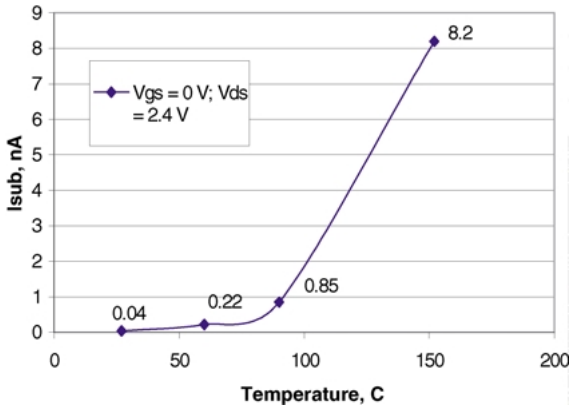

Fig. 6. Drain-to-substrate leakage current vs. temperature.

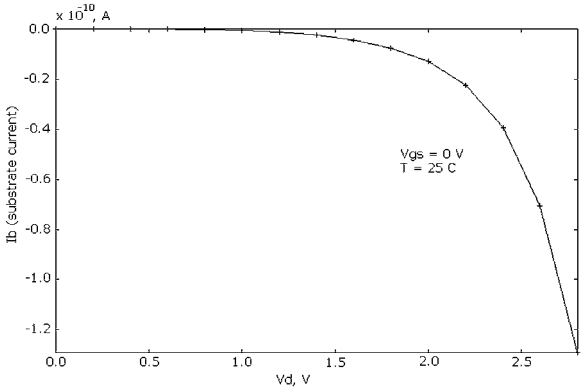

Fig. 7. Drain-to-substrate leakage current vs. drain voltage.

the variation of the surface potential at the source region that is related to the built-in potential between the source and substrate, and the Fermi potential. Both are temperature dependent [19].

It was measured in [20] that the DIBL coefficient was equal to 15 mV/V for n-MOSFET with the following parameters: $L_{\text{eff}} = 0.15$ μm, $T_{\text{OX}} = 40$ Å, channel doping $N = 4 \times 10^{17}$ cm^{-3}, junction depth $X_j = 0.12$ μm, and $T = 300$ K. The Microtec simulations give the DIBL coefficient value close to this reference.

4.5. *Drain-to-Substrate Leakage Current*

A one-sided p^+n junction has a reverse current [21]

$$I_R = qA\left(\frac{D_p}{\tau_p}\right)^{1/2}\left(\frac{n_i^2}{N_d}\right) + \left(\frac{qAn_i}{\tau}\right)\left(\frac{2\varepsilon V_R}{qN_d}\right)^{1/2} \tag{9}$$

Where A is the area of pn junction, q is the electron charge, N_d is the doping concentration of the n side, D_p and τ_p are minority carrier diffusion coefficient and lifetime on the n side, n_i is the intrinsic carrier concentration, ε is the dielectric constant of the semiconductor, V_R is the applied reverse bias voltage and τ is the space charge generation life-time. At high junction temperature, the first term in Eq. (9) that does not depend on the bias voltage is expected to be significant. At room and low temperature, the second term is expected to dominate.

The dependency of drain-to-substrate leakage current on operating temperature at fixed drain bias voltage (stressed condition) is shown in Fig. 6. Fig. 7 shows the drain-to-substrate leakage current versus drain bias voltage at room temperature. These simulation results were obtained for the following conditions

- Substrate doping is 5×10^{15} cm^{-3} (p-type)
- Drain doping is 9×10^{19} cm^{-3} (n-type)
- Drain pn junction area is (5 μm $\times$ 1.5 μm)

The drain-to-substrate pn junction leakage current was 7×10^{-12} A for nominal operating mode ($V_{\text{DD}} =$ 1.8 V and $T = 25$°C) and 8.2×10^{-9} A for stressed operating conditions ($V_{\text{DD}} = 2.4$ V and $T = 150$°C).

4.6. *Gate Induced Drain Leakage (GIDL) Current*

GIDL current is attributed to the tunneling, that occurs in the deep depleted drain region underneath the gate region. Several mechanisms have been proposed to

describe the behavior of GIDL current such as the indirect band-to-band tunneling model presented in [22] and the band-trap-band tunneling model explained in [23]. However, the band-to-band tunneling was identified as the major leakage mechanism based on qualitative agreement between experiments and theory [24, 25]. In case of band-to-band tunneling ($V_{GS} \leq 0$ V, $V_{DS} > 0$ V), the electrons emitted at the surface of the deep depletion layer in gate-to-drain overlap region are collected by the drain, thus increasing drain current and holes move towards the substrate increasing substrate leakage current. A simple 1-D band-to-band tunneling current model was presented in [22]. The theory of tunneling current predicts

$$I_{\text{GIDL}} = A \cdot E_s \exp(-B/E_s) \tag{10}$$

Where A is a constant [22]

$$A = \frac{q^2 \cdot m_r^{1/2}}{18 \cdot \pi \cdot h^2 \cdot E_{\text{gap}}^{3/2}} \tag{11}$$

B is a constant defined as follows [22]

$$B = \frac{\pi \cdot m_r^{1/2} \cdot E_{\text{gap}}^{3/2}}{2\sqrt{2} \cdot q \cdot \hbar} = 21.3 \text{ MV/cm} \tag{12}$$

with $m_r = 0.2 \cdot m_0$ (electron effective mass). E_{gap} is the direct energy gap of silicon ($\sim$3.5 eV). E_s is the vertical electric field at silicon surface.

Fig. 8 illustrates the GIDL effect in n-MOSFET in logarithmic-linear scale.

The slope of the current for $V_G < 0$ in curve (2) shows the increase in GIDL current since the electric field in the gate and drain overlap region is increasing with negative V_G. The simulated GIDL current for nominal operating conditions ($V_{DD} = 1.8$ V, $T = 25^\circ$C) is 1.7×10^{-10} A and for stressed operating conditions ($V_{DD} = 2.4$ V, $T = 150^\circ$C) is 0.4×10^{-7} A.

5. Impact of Technology Scaling on the Thermal Stress Effectiveness

The trend in CMOS technology is to Ultra Large Scale Integration (ULSI) whereby transistor physical dimensions are being significantly scaled down. To maintain a reasonable threshold voltage value for the given CMOS technology, the device physical dimensions are reduced, so the substrate impurity concentration must be increased. In [26] it is shown that the $dV_{\text{TH}}(T)/dT$

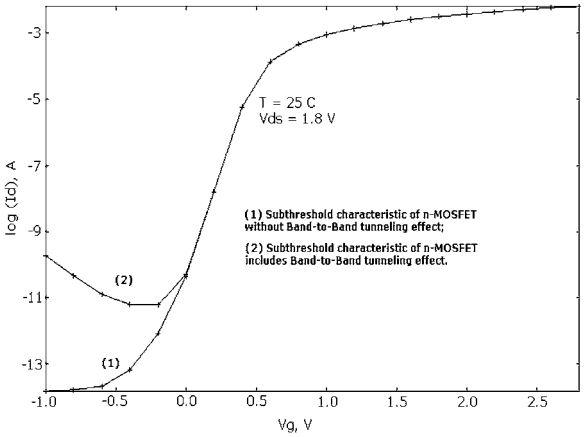

Fig. 8. Subtreshold characteristics of n-MOSFET. GIDL current is observed below threshold voltage.

decreases with downscaling, from 3.5 mV/°C for 6-μm process to 2 mV/°C for 2-μm process. We estimated the $dV_{\text{TH}}(T)/dT$ parameter for deep submicron technologies (0.18- and 0.35-μm) using a 2-D device simulator. The results are shown in Fig. 9. The data for 6-, 4- and 2-μm technologies were adopted from [26].

The $dV_{\text{TH}}(T)/dT$ parameter is significantly reduced with the technology scaling and agrees with theoretical prediction of this effect with decreasing oxide thickness, increasing body doping concentration, or both [26]. It means that the sensitivity of the threshold voltage variation to the temperature increase is reduced and the effectiveness of current testing at high temperature may also be reduced. For example, a reduced threshold voltage (lower than the nominal value) due to an error of threshold adjusting ion implantation may be

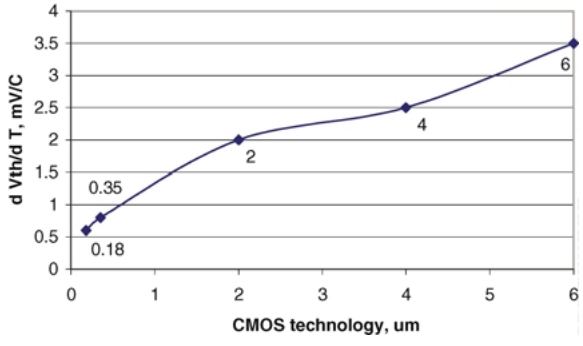

Fig. 9. Temperature rate of change of threshold voltage vs. CMOS technology scaling.

manifested weaker in a submicron technology than for long channel technology for the given test temperature.

6. Acceleration Factors: A Role of Voltage and Temperature in Stressed I_{DDQ} Testing

Reliability prediction often affects major decisions in system design. It is based on the assumption that systems fail as a result of failures of component parts and those parts fail partly as a result of exposure to application stress [27]. Typically, the stress voltage and temperature are two main stress factors that are used in reliability prediction models.

6.1. The Temperature Acceleration Factor

The device temperature dependency is assessed by the effect of temperature stress on dominant device failure mechanisms. The temperature dependency of microelectronic reliability is more complex than is represented by the Arrhenius equation. Microelectronics reliability depends on various forms of temperature stress other than steady state temperature, including temperature cycle magnitude, spatial temperature gradient, and time dependent temperature change. However, standard reliability-prediction procedures typically use an Arrhenius model to calculate a temperature acceleration factor (π_T). π_T is calculated using the reference (junction) temperature (T) and the activation energy (E_a). In this paper we used the Mil-Hdbk-217 procedure for π_T calculation. This procedure was developed by the US Department of Defense for the assistance to military departments, federal agencies, and industry. It is used by the electronic manufactures supplying devices to the military [28]. The formula for π_T calculation is [29]

$$\pi_T = 0.1 \exp\left(\left(\frac{-E_a}{K_B}\right)\left(\frac{1}{T} + 273\right) - \left(\frac{1}{298}\right)\right) \tag{13}$$

Where E_a is the activation energy (eV), K_B is the Boltzmann constant (eV/K) and T is the temperature of semiconductor die.

The activation energy can have wide values depending on different failure mechanisms. It means that the time to failure, predicted by the Arrenius model, is very sensitive to the value of activation energy. Typically, the dominant failure mechanism of submicron CMOS IC is not known in advance and we should assume that the average activation energy is defined as [29]

$$E_{a-ave} = \sum_{i=n} w_i \frac{E_{ai}}{n} \tag{14}$$

Where E_{ai} is the activation energy for the given failure mechanism, n is the number of failure mechanisms, and w_i is the weight coefficient. The main failure mechanisms for CMOS technology are presented in Table 3. w_i is assigned to the activation energy of each failure mechanism. This parameter is defined specially for the given technology and failure mechanism on the basis of statistical analysis of device fault reasons. In our investigation we assume that the w_i coefficient is unity. It means that all failure mechanisms have the same probability of occurrence. The calculated temperature acceleration factor as a function of temperature is shown in Fig. 10.

Finally, the Arrhenius model only estimates the temperature acceleration factor, because many failure mechanisms have a temperature threshold, below which failure will not occur. In other cases, a high temperature can actually inhibit or de-accelerate a failure mechanism, which will occur at the lower temperature [29], such as hot carriers injection.

6.2. Voltage Acceleration Factor

Historically, high voltage stress (HVS) testing was proposed for reliable rejection of weak insulation spots such as gate oxide and interlayer dielectric breakdown. However, the recent research found that metal sliver defects and polysilicon filaments may be successfully detected using HVS testing [31].

Table 3. Activation energy for different failure mechanisms [29, 30].

Failure mechanism	Activation energy, (eV)
Hot electrons	−0.06
Inter-metallic growth	2
Electromigration	0.35–0.85
Gate-oxide breakdown (electrostatic discharge)	0.3–0.4
Time dependent dielectric breakdown (TDDB) (Fowler-Nordheim tunneling model)	0.28
Stress-driven diffusive voiding of die metallization	1.0–1.4

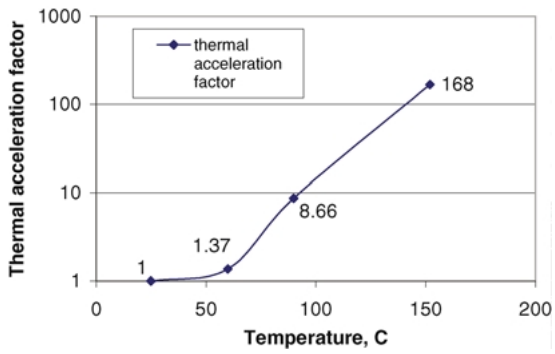

Fig. 10. Temperature acceleration factor as a function of temperature (Mil-Hbdk-217E model).

Typically, in all the reliability prediction procedures, the voltage stress factor, π_v is unity for all IC technologies except CMOS [32]. The value of π_v in CNET procedure (National Center for Telecommunication Studies, France) depends on the applied voltage (V_A) and the device junction temperature (T) [32]

$$\pi_v = A_3 \exp[A_4 V_A (T/298)] \tag{15}$$

The constants A_3 and A_4 depend on the voltage and range from 0.2 to 2.2. In our investigation we assumed $A_3 = 0.25$ and $A_4 = 0.21$ as it is used in NTT procedure (Nippon Telegraph and Telecom Corporation). The results of voltage acceleration factor calculation using Eq. (15) are shown in Fig. 11. The stressed voltage was 2.4 V. The voltage acceleration factor at 27°C was set to unity and voltage acceleration factors for other temperatures were calculated from that point.

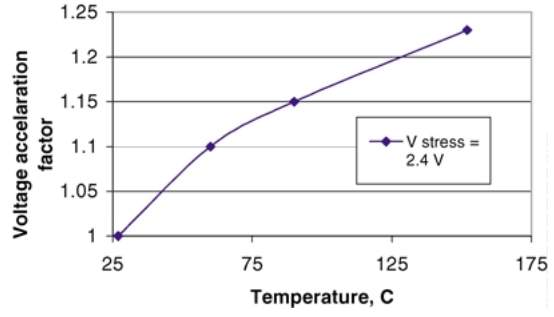

Fig. 11. Voltage acceleration factor as a function of temperature.

7. I_{DDQ} Limit Setting

We estimated the I_{DDQ} limits under normal and stressed conditions. An n-MOSFET with parameters shown in Table 2 was simulated in the Microtec device simulator under normal ($V_{DD} = 1.8$ V, $T = 25$°C) and stressed ($V_{DD} = 2.4$ V, $T = 150$°C) environmental conditions. These stressed conditions are often used in industry [33]. The overall off current is given by the following equation:

$$I_{\text{off-total}} = I_{\text{weak-inversion}} + I_{\text{substrate}} + I_{\text{GIDL}} + I_{\text{bulk-punchthrough}} \tag{16}$$

In this equation, $I_{\text{weak-inversion}}$ includes the subthreshold leakage current component and leakage current component due to DIBL effect. A physical device simulator, such as Microtec, calculates these components together. The tunneling current through the gate oxide is fairly small for 0.18 μm CMOS technology and is neglected in this equation. The total leakage in normal conditions, $I_{\text{off-totalN}}$, was found to be 6.8×10^{-10} A for the transistor. Similarly, the total leakage in stressed conditions, $I_{\text{off-totalS}}$, was found to be 1.4×10^{-7} A. Dividing these values by the transistor width gives us the I_{off} total per micron. For stressed ΔI_{DDQ} testing, the difference of leakage current at normal and stressed condition is required. The Fig. 12 shows the variation of leakage current components of analyzed n-MOSFET for normal and stressed operating modes. We can conclude from Eq. (16) that the defect-free die should have a difference of leakage current between stressed and normal operating conditions more than two orders of magnitude.

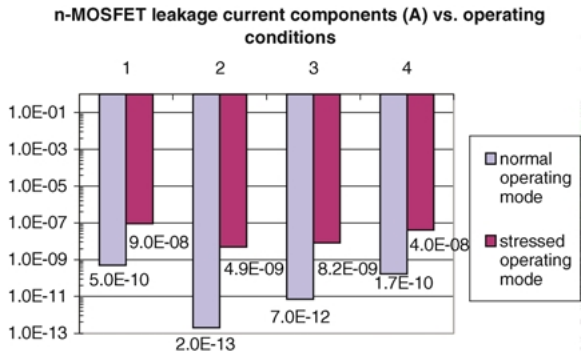

Fig. 12. n-MOSFET ($W/L_{\text{eff}} = 5$ μm/0.13 μm) leakage current components vs. operating conditions. 1–weak inversion current, 2-bulk punchthrough current, 3-drain-to-substrate current, 4-GIDL current.

At normal operating conditions, weak inversion and GIDL currents have comparable values and dominate in a total leakage current. At stressed operating conditions these currents dominate also, but other two components are significantly increased and their part in a total leakage is essential. The typical method of GIDL current reduction was lightly doped drain (LDD) regions formation. However, this technique is not effective for deep submicron technologies, because highly doped source/drain (HDD) extensions are used today in the logic CMOS circuits for suppression of source/drain parasitic resistance and short-channel effect [34]. The possible solution for GIDL reduction is the advanced channel and source/drain engineering [35].

Now let us consider a hypothetical VLSI with one million core transistors. Assuming it is a fully static design, half of the transistors are in off state and other half being in linear mode. These off transistors are equally distributed between n- and p-MOSFETs. The overall chip leakage current (I_{DDQ}) will be determined by the off transistors. Furthermore, assuming each n-MOSFET is 0.5 micron wide and each p-MOSFET is 1.5 micron wide. Finally, assuming that off state leakage per micron width is the same for n- and p-MOSFETs, we can compute I_{DDQ} by following equation

$$I_{\mathrm{DDQ}} \approx \frac{N}{2} \times I_{\text{off-total}} \times [W_n + W_p] \qquad (17)$$

Where N is the number of MOSFETs in a VLSI, $I_{\mathrm{off-total}}$ is the n-MOSFET leakage current per unit micron width, W_n and W_p are the widths of n-MOSFETs and p-MOSFETs, respectively. Given these parameters, I_{DDQ} can be calculated under normal and stressed conditions. For example, the nominal and stressed condition I_{DDQ} for above mentioned VLSI is estimated to be 0.13 mA and 28 mA respectively. Therefore, ΔI_{DDQ} in this particular case is approximately 28 mA for defect free case.

The resolution of ΔI_{DDQ} testing may further be increased by several techniques. First, the initial measurements should be taken under stressed conditions. Subsequently, measurements should be repeated under normal conditions. The Δ should be computed as before. This order of measurements has certain benefits. Subtle defect mechanisms are accelerated under stressed conditions before the nominal measurements are taken. Therefore, I_{DDQ} measurements of defective VLSI are likely to be higher than the calculated value. In these test conditions, if the Δ value is smaller than the pre-determined value (i.e., the reduction in current is smaller), the VLSI is considered as defective. On the other hand, if the Δ is higher than pre-determined value, a VLSI may be considered defect-free. Secondly, the resolution of the ΔI_{DDQ} technique may be enhanced by reducing the thermal and voltage stress values. As a consequence the defect-free values may become smaller and the stability of stressed temperature may be better controlled. Further research is necessary to determine optimum stress conditions for ΔI_{DDQ} testing. Finally, the resolution of ΔI_{DDQ} testing may also be increased by partitioning the core logic in several I_{DDQ} testable domains [36]. This can be achieved by providing extra power supply pads or by creating power down modes for I_{DDQ} testing.

8. Future Work

We look forward to further investigate various aspects of stressed ΔI_{DDQ} testing. Firstly, it will be informative to analyze the behavior of different kinds of defects under stressed operating conditions. The subthreshold leakage current, which is the dominant leakage current mechanism in sub-quarter micron MOSFETs, is exponentially dependent on temperature and V_{DD}. On the other hand, leakages caused by resistive bridges between metal lines, or permanently ON transistors due to punchthrough effect or resistive gate oxide shorts, shows little dependence on temperature. Typically, the leakage current from these defects shows the sub-exponential dependency on temperature [37]. However, the research is required to investigate these issues in detail.

Secondly, the impact of L_{eff}, W_{eff}, V_{TH} process variation on I_{off} of MOSFETs may be different under normal and stressed operating conditions and hence the process variation can have the significant influence on the sensitivity of stressed ΔI_{DDQ} testing. The obtained simulation results presented in Fig. 13 show that the leakage current of MOSFET has exponential dependency on L_{eff} variation under normal operating conditions. However, it has super exponential dependency on L_{eff} variation under stressed operating conditions for abnormal short channel transistors.

Finally, further research is required to determine practical I_{DDQ} limits for stressed and normal operating conditions. One of the possible solutions is to define statistically the I_{DDQ} limits as three-sigma values of leakage current distributions from different test

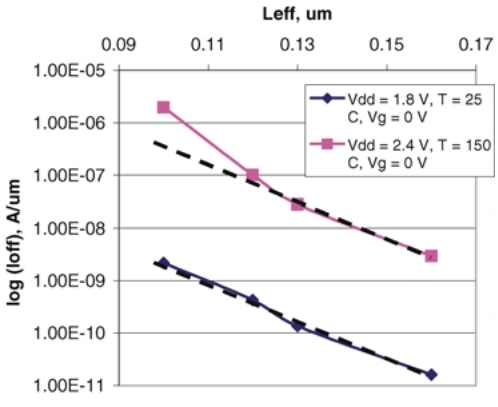

Fig. 13. Impact of n-MOSFET channel length variation on leakage current under normal and stressed operating conditions.

patterns under normal and stressed operating conditions for chips which passed burn-in testing [6, 7].

9. Conclusion

We analyzed and estimated intrinsic leakage current components of an 0.18 μm n-MOSFET for ΔI_{DDQ} testing. Δ was calculated as the difference of currents under stressed and normal operating currents. The calculated I_{DDQ} values for normal ($V_{DD} = 1.8$ V, $T = 25^{\circ}$C) and stressed ($V_{DD} = 2.4$ V, $T = 150^{\circ}$C) for one million transistor VLSI was estimated to be 0.13 mA and 28 mA, respectively. Δ is a strong function of applied stresses and can be optimized for defect acceleration and detection. The thermal and voltage acceleration parameters increase with increased stress conditions. Therefore, a high stress is desirable. However, as the stress value is increased, the Δ value of the current is also increased which results in diminished defect detection capability.

The effectiveness of ΔI_{DDQ} testing can be enhanced by first taking the I_{DDQ} measurements under stressed conditions and subsequently performing I_{DDQ} measurements under nominal conditions. Similarly, logic partitioning may also increase the effectiveness of ΔI_{DDQ} testing.

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