Sub-quarter Micron SRAM Cells Stability in Low-Voltage Operation: A Comparative Analysis

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ABSTRACT

Comparative analysis of the conventional 6T and recently proposed loadless 4T CMOS SRAM cells is performed. Based on HSPICE simulations for 0.18-μm technology, we compared the stability of the aforementioned cells to temperature and process (V_{TH}, L_{eff}, T_{OX}) variations as well as the cells robustness in low-voltage operation. We found that at V_{DD} = 1.2 V the loadless 4T cell has a 20% higher static noise margin (SNM) and 1.5 times lower sensitivity to the V_{TH} fluctuations than the 6T cell. On the other hand, the 4T cell has a stronger read current degradation at reduced V_{DD}. The analytical model for SNM calculation of the loadless 4T CMOS SRAM cell has been developed.

Keywords – CMOS SRAM cell stability, static noise margin, process fluctuations.

I. Introduction and Motivation

Scaled down SRAM cells are constrained to operate at low supply voltage (V_{DD}), since scaled down MOSFETs require low bias voltage to reduce power dissipation in circuits and to realize high reliability against hot carrier degradation and gate oxide dielectric breakdown.

However, as the memory is scaled down, the noise margin for the cell decreases due to reduction in MOSFET transconductance (g_m) caused by the mobility degradation and by parasitic resistances such as contact resistance [1]. Furthermore, the noise margin due to process variations and soft errors does not scale down with the supply voltage. Thus, it is necessary to design the SRAM cell at low V_{DD} with sufficient noise margin compared to the SRAM cell at nominal V_{DD}.

Generally, cell stability is defined by static-noise margin (SNM). SNM have been expressed analytically and investigated by computer simulations for conventional 6T SRAM [Fig. 1 (a)] and 4T resistor-load SRAM cells in [2,3]. Recently, a new loadless 4T SRAM cell [Fig. 1 (b)] was proposed for ultra-high density SRAM Macro [4,5]. This cell size is 50-65% smaller than a cell size of conventional 6T SRAM cell, when compared with the same access speed and has comparable SNM with conventional cell. However, the impact of technology parameters variation, such as threshold voltage (V_{TH}), effective channel length (L_{eff}), gate oxide thickness (T_{ox}), as well as V_{DD} scaling and operating temperature increase on stability of loadless 4T SRAM cell in comparison with a conventional 6T SRAM cell was not widely investigated in literature.

This paper is organized as follows. In section II, we discuss the SRAM cells design, which are included in our comparative analysis. The impact of operating voltage reduction and chip temperature increase on SNM of SRAM cells is analyzed in section III. In section IV, we investigate the impact of technology variation of transistor channel length (L_{eff}) and threshold voltage (V_{TH}) on SRAM cells stability. The proposed analytical model for SNM of loadless 4T SRAM cell is discussed in section V. The paper is concluded in section VI.

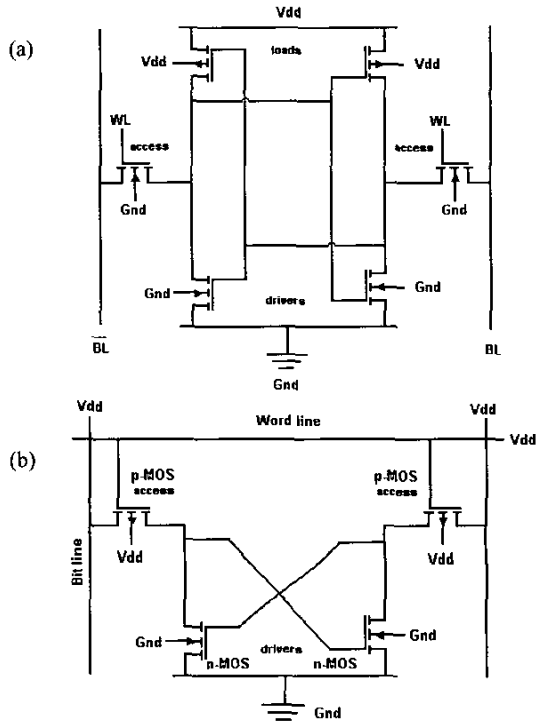

Figure 1. SRAM cells design: (a) conventional 6T SRAM and (b) loadless 4T SRAM in stand-by mode [4].

II. SRAM Cell Design

Seevinck et al. [3] showed that the SNM of an SRAM cell depends only on the magnitude of V_{TH}, V_{DD}, the ratio of the transconductance factors of the driver and access transistors ($r=\beta_{driver}/\beta_{access}$) referred to as the *cell ratio r*, and the $q=\beta_{load}/\beta_{access}$ ratio. It does not depend on the absolute values of the β's. In our case, the optimized 6T SRAM and loadless 4T SRAM cells have SNM ≈ 600 mV at the nominal operating conditions for 0.18-um CMOS technology. The transfer characteristics of the analyzed cells and used transistor ratios (*q* and *r*) are shown in Fig. 2. All simulations of analyzed SRAM cells in this paper were performed in Cadance (HSPICE

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MOSFET model level 49) using 0.18-μm CMOS technology parameters.

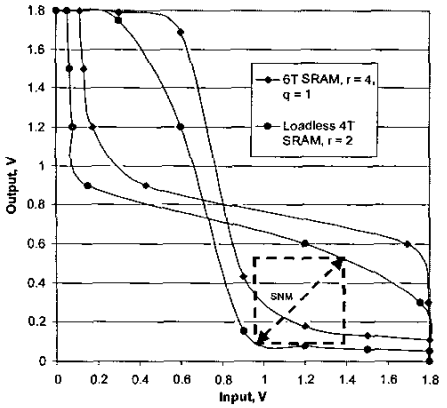

Figure 2. SNM of analyzed SRAM cells at nominal operating conditions (V_{DD} = 1.8 V, T = 300 K). Here, SNM is the diagonal of maximized area of a square inside of inverter characteristic loop.

III. Impact of Operating Voltage Reduction and Temperature Increase on SNM of SRAM Cell

Due to the increasing demand in low power battery-operated devices, the operating voltage (V_D) of VLSI circuits is constantly decreasing. With the technology scaling, the transistor density in a chip is approximately doubled for each new technology generation. As a result, the average operating temperature of the chip has increased. This tendency is observed for ICs with high transistor density, such as memory and microprocessors [6]. The operating temperature increase and V_{DD} reduction induce the significant degradation of SNM of SRAM cells [2,3]. The simulation results of SNM versus V_{DD} at different temperatures are presented in Fig. 3. As can be seen, the loadless 4T SRAM cell has 20% higher SNM at low V_{DD} (1.2 V) and a room temperature than the conventional 6T SRAM cell. However, the SNM of the loadless 4T cell is considerably more sensitive to the increase of the operating temperature than the SNM of the 6T cell. K. Takeda, et al. observed the strong temperature dependence of SNM of loadless 4T SRAM cells in 4-Mb SRAM Macro chip [7]. Hence, the SNM of loadless 4T SRAM cell is highly sensitive to mismatching of threshold voltages in the cell at elevated temperature in comparison with conventional 6T SRAM cell. The read current degradation due to V_{DD} reduction is depicted in Fig. 4. As can be seen, the read current of the loadless 4T SRAM cell degrades faster approximately 2.1X with the decreasing V_{DD} from 1.8 V to 1,2 V than the read current of conventional 6T SRAM cell. It means that although a loadless 4T SRAM cell may operate at low V_{DD}, it demands a careful design of memory chip with a minimal parasitic capacitance of a bit line and low leakage current of non-active memory cells.

IV. Impact of Technology Variation of Transistors Length and V_{TH} on SNM of SRAM Cell

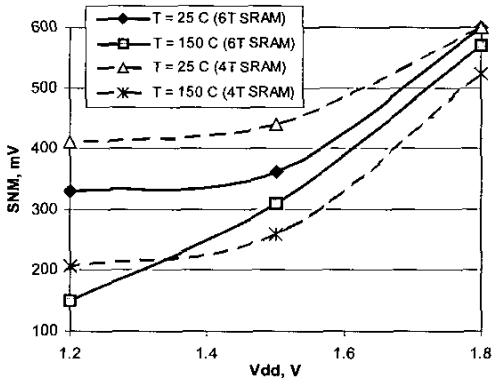

Figure 3. SNM versus supply voltage at different temperature.

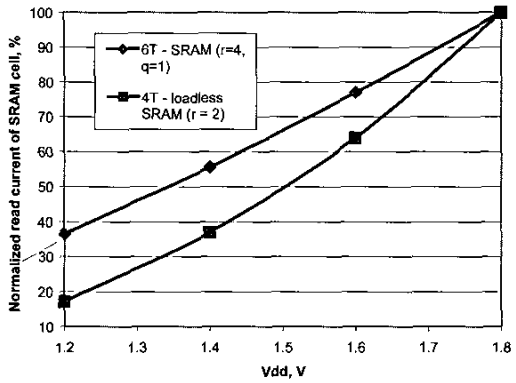

Figure 4. Normalized read current of analyzed SRAM cells vs. V_{DD}.

Successful scaling of MOSFETs to sub-quarter micron feature size for use in high density and low power applications will require understanding of effect of process variations on SRAM cell stability. There are several technology dependent transistor parameters, which define reliable operation of transistors within a SRAM cell, such as effective channel length, gate oxide thickness and channel doping. The effective channel length variation may be the result of lithography equipment limitations and improper masks shifting [8]. The average concentration of channel doping is quite well controlled by ion implantation and annealing processes. However, these processes lead to randomness at the atomic scale in the form of spatial fluctuations in the local doping concentration, which cause the device-to-device variation in MOSFET threshold voltages. The impact of this effect on stability of conventional 6T SRAM cells was investigated in [9].

Recently, severe technology variation of the gate oxide thickness (T_{OX}) in 0.18-μm CMOS technology was reported [10]. For device with 2.5 nm T_{OX} at the center of the channel, the physical T_{OX} is ranged from 1.8 nm to 4.2 nm for various positions of the channel. It was found that this variation is the result of different oxide growth rates determined by the orientation and stress conditions of the local Si surface, especially at the rounded corners of the shallow-trench isolation (STI). In additional, poly-Si intrusion from the gate electrode also causes local T_{OX} thinning [10]. Both T_{OX} thickening and

T_{OX} thinning impact on the gate oxide reliability by reducing of time to breakdown and the threshold voltage variation.

Since the SNM of SRAM cell depends on the transistor size ratios (r and q), the L_{eff} variations of drive and load transistors in 6T cells and drive transistors in loadless 4T cells represent the impact of channel length variation on the SRAM cell stability. In the simulations, the gate length of a specific transistor was intentionally varied around its nominal value, while other transistor parameters of the cell remained unchanged. When the noise margin of a scaled-down CMOS memory cell is analyzed, the graphical approach (Fig. 2) using the input-to-output transfer characteristics of the internal equivalent inverter is effective [1,11]. Using simulations of equivalent inverters of the analyzed memory cells, we found that a loadless 4T SRAM cell has ~1.9 times stronger SNM dependence on the L_{eff} than the 6T SRAM cell (Fig. 5).

Based on the HSPICE simulations, we estimated the SNM dependence on the V_{TH} variations of each transistor in equivalent inverters of the analyzed SRAM cells. In the simulations, the threshold voltage of a specific transistor was intentionally varied around its nominal value by applying the appropriate body bias, while parameters of the other transistors of the equivalent inverter remained unchanged. This technique imitates the V_{TH} process variation. We found that the SNM of loadless 4T SRAM cell is less dependent on the V_{TH} variations within a cell than the conventional 6T SRAM cell, which SNM is ~1.5 times more sensitive to the V_{TH} fluctuations (Fig. 6).

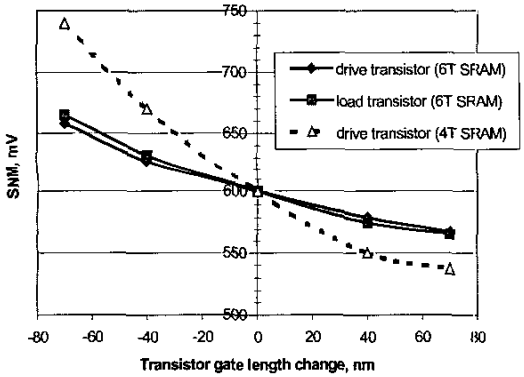

Figure 5. SNM of analyzed SRAM cells versus MOSFETs lengths change at V_{DD} = 1.8 V and T = 25 °C.

V. Analytical model for SNM of loadless 4T SRAM cell

The analytical model for SNM calculation of conventional 6T SRAM cell was proposed by E. Seevinck, et al. [3]. They used transistor drain current equations for linear and saturation modes which are valid for long channel MOSFETs and assumed that p-MOSFET and n-MOSFET have the same threshold voltage value. However, these equations can not be applied for sub-quarter micron SRAM cell, because they neglect short-channel effects. The proposed in this paper analytical model of SNM for loadless 4T SRAM cell is based on the short-channel α-power law model of MOSFET [12].

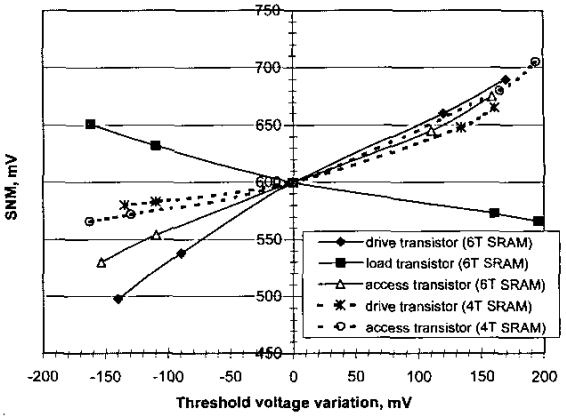

Figure 6. SNM of analyzed SRAM cells versus V_{TH} transistors variation at V_{DD} = 1.8 V and T = 25 °C.

According to the conventional α-power law model, MOSFET current can be expressed as:

$$I_D = \begin{cases} 0, \text{ in cutoff} \\ K_l \left(V_{GS} - V_{TH}\right)^{\frac{\alpha}{2}} V_{DS}, \text{ in linear} \\ K_s \left(V_{GS} - V_{TH}\right)^{\alpha}, \text{ in saturation} \end{cases} \quad (1)$$

Where

$$K_l = \frac{I_{D0}}{V_{D0}\left(V_{DD} - V_{TH}\right)^{\frac{\alpha}{2}}} \quad \text{, and} \quad K_s = \frac{I_{D0}}{\left(V_{DD} - V_{TH}\right)^{\alpha}}$$

In α-power law model, I_{D0} is the drain current at $V_{GS}=V_{DS}=V_{DD}$, V_{D0} is the drain saturation voltage at $V_{GS}=V_{DD}$, V_{TH} is the respective threshold voltage of a transistor and α is the velocity saturation index.

Table 1 represents the extracted parameters of α-power law model from SPICE simulations of 0.18-um MOSFETs used in SRAM cell. The values of α for n-MOS and p-MOS transistors are obtained from fitting the calculated V_{GS} vs. I_D ($V_{DS} = V_{DD}$ = 1.8 V) α-power model curves to the SPICE simulated ones.

Table 1. α - power law MOSFET model parameters for V_{DD}=1.8 V.

Model parameters	**n-MOSFET,** W/L=1μm/0.18μm	**p-MOSFET,** W/L=0.5μm/0.18 μm
α_{lin}	1.2	1.4
α_{sat}	1.15	1.4
V_{D0}, V	0.98	0.98
V_{TH_lin}, V (V_{DS}=0.1 V)	0.490	0.522
V_{TH_sat}, V (V_{DS}=1.8 V)	0.489	0.488
I_{D0}, mA	0.646	0.123

In the proposed analytical model, we assumed that (V_{OL}, V_{IH}) and (V_{OH}, V_{IL}) points on the transfer characteristics of equivalent inverter are the points where the curve slope equals –1 [13]. SNM is the diagonal of a rectangle with apices at (V_{OL}, V_{IH}) and (V_{OH}, V_{IL}). This interpretation of SNM [14] is graphically presented in the inset of Fig. 7.

$$SNM = \sqrt{\left[\left(\frac{K_{l\_p}}{\alpha_{s\_n}K_{s\_n}}\right)^{\frac{1}{\alpha_n-1}}\left(V_{DD}-V_{THp}\right)^{\frac{\alpha_{l\_p}}{2(\alpha_{s\_n}-1)}} - \frac{K_{s\_p}\left(V_{DD}-V_{THp}\right)^{\alpha_{s\_p}}}{K_{l\_n}\left(V_{IH}-V_{THp}\right)^{\frac{\alpha_{l\_n}}{2}}} + V_{THn}\right]^2 + \left[V_{DD}+V_{THn} - \frac{K_{s\_n}\left(V_{IL}-V_{THn}\right)^{\alpha_{s\_n}}}{K_{l\_p}\left(V_{DD}-V_{THp}\right)^{\frac{\alpha_{l\_p}}{2}}} - \left(\frac{2K_{l\_n}}{\alpha_{l\_n}K_{s\_n}}\right)^{\frac{2}{\alpha_{l\_n}+2}}\left(V_{DD}-V_{THp}\right)^{\frac{2\alpha_{s\_p}}{\alpha_{l\_n}+2}}\right]^2} \quad (2)$$

The mentioned definition of SNM allows its mathematical calculation. Whereas the SNM, defined as the diagonal of the maximum square embedded in the inverter characteristic loop can be easily applied for graphical extraction of SNM, it cannot be derived mathematically. To find V_{OL} and V_{IH}, we equated the I_D equation in linear mode for n-MOSFET and I_D equation in the saturated mode for p-MOSFET. In turn, to find V_{OH} and V_{IL}, we equated the I_D equation in saturated mode for n-MOSFET and I_D equation in linear mode for p-MOSFET using drain current models from Eq. 1. The final equation for the SNM calculation of 4T SRAM cell is given by Eq. 2. In this equation, α_{s_n} is α for saturated n-MOSFET, α_{l_n} is α for linear n-MOSFET, α_{s_p} is α for saturated p-MOSFET and α_{l_p} is α for linear p-MOSFET. Note that the proposed model allows to calculate SNM of loadless 4T SRAM cell in respect that the threshold voltages of n-MOSFET and p-MOSFET may be different. Fig. 7 presents the calculated and the simulated SNM vs. V_{DD} of the 4T loadless SRAM cell using "-1" slope SNM definition. The average error of the proposed model with respect to the simulated data is ~14-15%.

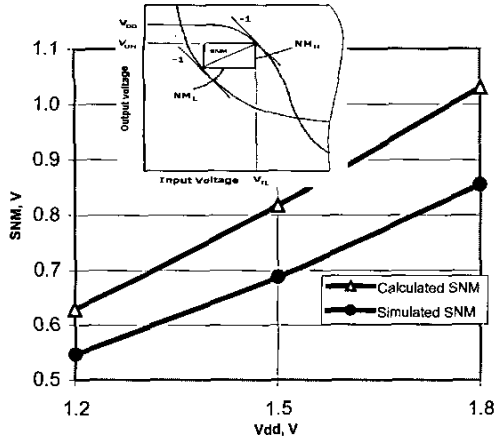

Figure 8. SNM of the 4T loadless SRAM cell. $(W/L)_{driver}$=1 μm/0.18 μm, $(W/L)_{access}$=0.5 μm/0.18 μm (simulations and calculations results).

VI. Conclusion

In this paper we performed a comparative analysis of stability of the conventional 6T SRAM cell and a recently proposed loadless 4T SRAM cell to the temperature and process (V_{TH}, L_{eff}, T_{OX}) fluctuations, and developed an analytical model for calculation of the SNM for a 4T loadless SRAM cell. Basing on HSPICE simulations, we conclude that:

- the loadless 4T SRAM cell has 20% higher SNM than the conventional 6T SRAM cell at V_{DD} = 1.2 V and T = 25°C. However, the loadless 4T SRAM cell is more sensitive to the operating temperature increase and has 2.1X stronger read current degradation than the 6T SRAM cell as V_{DD} is reducing from 1.8 V to 1.2 V.
- the loadless 4T SRAM cell has 1.5X less SNM sensitivity to the V_{TH} fluctuations and 1.9X stronger dependence on L_{eff} than the conventional 6T SRAM cell.
- the loadless 4T SRAM cell can be successfully used in low-voltage SRAM circuits. However, its implementation demands a careful circuit design with a minimized parasitic capacitance of the bit lines and low leakage current of non-selected memory cells due to the considerable read current degradation as V_{DD} is reducing from 1.8 V to 1.2 V.

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