Impact of Technology Scaling on Bridging Fault Modeling and Detection in CMOS Circuits

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical Engineering

Waterloo, Ontario, 2001

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Acknowledgements

I wish to express my extreme gratitude to my supervisor, Dr. M. Sachdev, for his guidance and support throughout my university career, especially during my graduate research, and helpful advice during the writing of this thesis.

I also wish to thank Dr. Michael S. Obrecht for many useful comments and conversations regarding my research, and my thesis readers for their helpful comments and constructive critiques.

I would like to thank the members of the VLSI Research Group at the University of Waterloo for their assistance.

Dedication

This thesis is dedicated to my mother and wife, and in memory of my father, who began my education in microelectronics area and who motivated me to continue it.

Abstract

CMOS technology scaling allowed to reduce MOSFET dimensions from 10 μm in the 1970's to a present day size of 0.13 μm. The ability to improve performance consistently with decreasing power consumption has made CMOS technology the dominant technology for integrated circuits. The scaling of the MOS transistor has been the primary factor driving improvement in microprocessor performance. However, recent developments and future trends in CMOS process and design technologies are introducing new levels of complexity in testing. For example, the consequent reduction of MOSFET threshold voltage and the increase of leakage current are decreasing the effectiveness of quiescent current testing (I_{ddq}) because the reduced ratio between the MOSFET "on" and "off" currents is making this testing technique impracticable for deep submicron technologies.

In this thesis we investigate the behavior of bridging faults (BF) in CMOS digital integrated circuits and analyze the impact of BFs on logic margin and logic swing of sequential and combinational CMOS circuits under different operating conditions and technology feature sizes. The BF model in CMOS digital circuits was developed. This model explains the impact of technology scaling on effectiveness of BF detection using logic test method and has a good agreement with HSPICE simulation results. The developed model allows to find the critical BF resistance values for different CMOS technologies.

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Chapter 1: Introduction and Background

1.1 Introduction

Economic and functional needs stimulate a progressive increase of the number of transistors integrated on a single chip. Until now the electronic technologies have been able to satisfy these needs through dimension scaling and reliability improvement of electronic components. An increasing complexity of testing is the result of the moving from VLSI (vary large-scale integration) to ULSI (ultra large-scale integration) for CMOS digital circuits. The complex expressions describing the MOS transistor behavior make it difficult to understand the reasons for high test escape. Such test escapes have to be reduced to continue elevated quality levels. The support of high fault coverage, which provides better reliability, is very expansive and difficult task in case of ULSI CMOS technology.

In this thesis we analyze the impact of technology scaling on bridging fault (BF) modeling and detection in deep submicron CMOS circuits. A poor understanding of transistor behavior in different regions of operation and the gap between model parameters and physical quantities are significant barriers to the development of more effective testing methods. Nowadays analytical models of transistors can be used with notable success to better understanding of impact of submicron technologies on IC testing, and to find new ways to improve fault detectability. This thesis analyses the behavior of important class of defects, the BFs, to demonstrate the inadequacy of conventional test methods (current and logic testing) for advanced combinational and sequential CMOS circuits. Current testing techniques are very useful in detecting many types of defects, however only a combination of both current and Boolean voltage-

sensing techniques is essential to guarantee high quality, because "Mix" testing may significantly increase the BF defect coverage. The sensitivity of conventional current testing of deep submicron CMOS IC is reduced dramatically because of a high value of intrinsic defect-free leakage current of short-channel MOSFETs. Hence, the role of logic testing is increased and the main task of research is to find the optimal test conditions (frequency, temperature and voltage supplier value) to increase the BF coverage. In this research we tried to estimate the impact of operating conditions on BF coverage in logic testing.

The structure of this thesis is as follows. Chapter 1 consists of a brief review of the CMOS technology and interconnects scaling trends, and principal limitations of this process. The discussion of main defect classes in digital CMOS circuits is also presented in Chapter 1. Chapter 2 describes the current testing technique of BF and explains the limitations of this test method for deep submicron CMOS circuits. The impact of CMOS technology scaling on *BF detection* in sequential and combinational circuits is discussed in Chapter 3. The behavior of BF under different operating conditions is analyzed using HSPICE simulations in Cadance and the recommendations for coverage increase of BF detection in advanced CMOS circuits using logic testing are obtained. Chapter 4 deals with the impact of CMOS technology scaling on *BF modeling*. The developed BF model uses key technology parameters and allows to explain the simulation results, which were derived in the previous chapter. Finally, the summary of the research and conclusions are presented in Chapter 5.

1.2 CMOS Technology Trends and Limits

Conventional scaling of gate oxide thickness, source/drain extension (SDE), junction depths, and gate lengths have enabled MOS gate dimensions to be reduced from 10 μm in the 1970's to a present day size of 0.1 μm. To enable further transistor scaling in the 21st century, new solutions such as high dielectric constant materials for gate insulation and ultra low resistivity junctions need to be developed. The traditional SiO_2 gate dielectrics will reach fundamental leakage limits, due to tunneling, for an effective thickness less than 2.3 nm [1]. Experimental data and simulations show that, although conventional scaling of junction depths is still possible, but increased resistance for junction depths below 30 nm results in performance degradation [1]. Because of these limits, it will not be possible to improve short channel effects further. This will result in either unacceptable off-state leakage current or strongly degraded device performance for channel lengths below 0.1 μm. The fundamental scaling limits for conventional MOS devices are presented in Table 1.1. MOS transistor will possibly reach to its limits for 0.13 μm process technologies in 2002. Because of these problems, new solutions need to be developed for continued transistor scaling.

New-generation process technologies generally come out every three years and provide roughly a 0.7x reduction in minimum feature size [2]. Using 0.7x as the scale factor S, each generation gives a transistor area improvement of 0.49x, a gate delay improvement of 0.7x, and an power reduction of 0.34x. Figure 1.1 shows how transistor parameters have scaled over the last six generations of Intel microprocessor technology.

Feature	Limit	Reason
Oxide Thickness	2.3 nm	Leakage (I_{GATE})
Junction Depth	30 nm	Resistance (R_{SDE})
Channel Doping	V_{th} = 0.25 V	Leakage (I_{OFF})
Channel Length	0.06 μm	Leakage (I_{OFF})
Gate Length	0.10 μm	Leakage (I_{OFF})

Table 1. 1: *Fundamental scaling limits for conventional MOS devices.*

Minimum feature size and gate oxide thickness (T_{OX}) have been scaled down by ~0.7x with every generation, while supply voltage (V_{DD}) has been scaled down only for the last three generations. Until the 0.8 μm CMOS technology, 5 V was the industry standard supply voltage and since power and reliability were not yet important issues, there was no concern to justify deviating from the standard supply voltage. But beginning with the 0.5 μm CMOS technology, chip power and gate oxide reliability issues, forced adoption of scaled supply voltage with every new technology generation. From this period, transistor performance, measured by inverter circuit delay, has improved by ~0.7x per generation. So indeed, MOS transistor scaling has served us well by providing continued improvements in density, performance, and power.

Gate Oxide Scaling

Gate oxide thickness scaling has been instrumental in controlling short channel effects as MOS gate dimensions have been reduced from 10 μm to 0.1 μm. Gate oxide thickness must be approximately linearly scaled with channel length to maintain the same amount of gate control over the channel to ensure good short channel behavior.

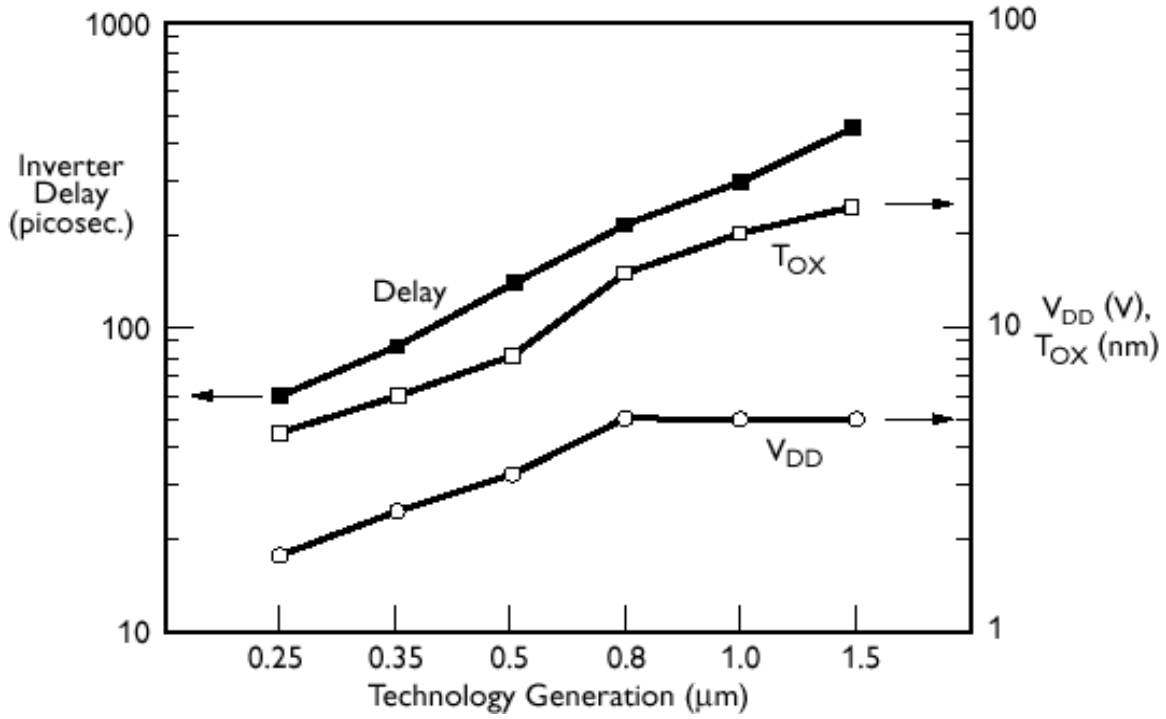


Figure 1.1: *Transistor parameters trends [2]*.

Figure 1.2 shows the Semiconductor Industry Association (SIA) road map for scaling of gate dielectric thickness. This roadmap predicts that continued gate dielectric scaling will require a new gate dielectric material for 0.1 μm CMOS technology and below [3]. Alternative high dielectric constant materials will be the key to continued MOSFET scaling beyond 0.1 μm gate dimensions. Table 1.2 lists the leading alternative dielectrics and their status.

Dielectric	**Dielectric Constant [ε (SiO_2) = 4]**	**Status**
Si_3N_4	7	Close to be ready
Ta_2O_5	25	Early stages
TiO_2	50	Very early stages

Table 1.2: *Alternate high dielectric constant materials [4]*.

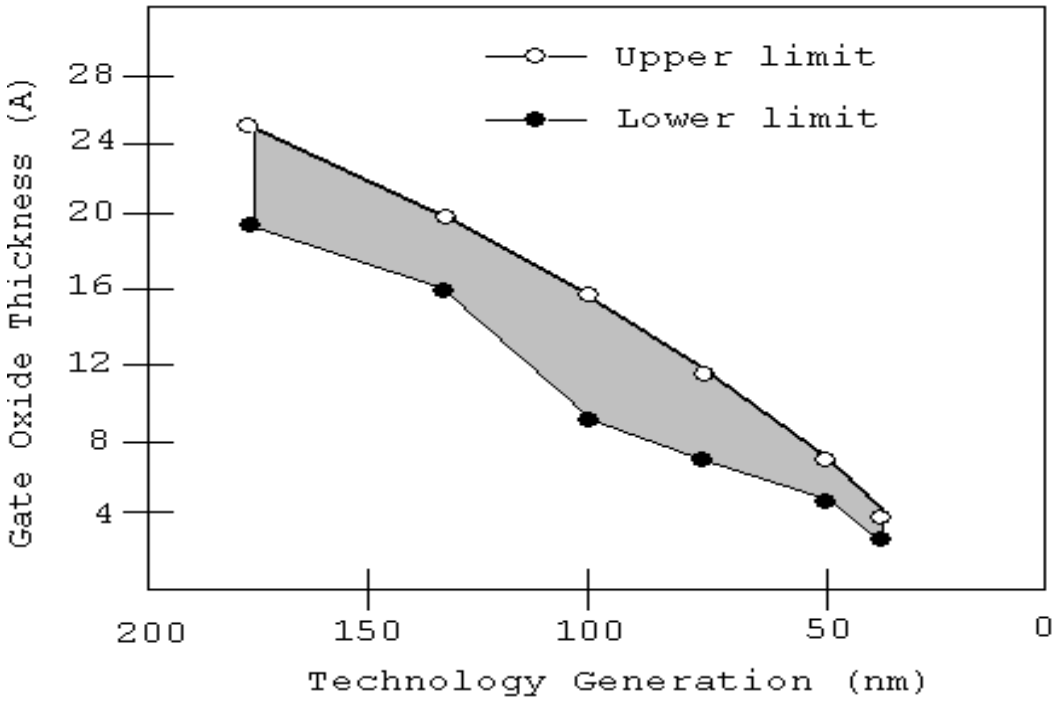


Figure 1.2: *Scaling trend of gate dielectrics as predicted in 1998 SIA roadmap [3]*.

Source/Drain Engineering

Reducing source/drain junction depths will improve device short channel characteristics by reducing the amount of channel charge controlled by the drain. However, shallow silicided junction leads to unacceptable junction leakage, and increases the contact-junction resistance. For high performance sub-100 nm CMOS technology, a selective epitaxial growth (SEG) process was developed. By utilizing the SEG process, the suppression of short channel effect, junction leakage current, and parasitic resistance are realized [5]. Junction depths are currently 50-100 nm for 0.25 μm CMOS technology and are predicted to be as low as 10 nm for future deep sub-micron devices (Figure 1.3).

Channel Engineering

One of the effective techniques to improve short channel characteristics is channel engineering. The goal is to optimize the channel profile to minimize the off-state leakage

while maximizing the linear and saturated drive currents. Super Steep Retrograde Wells (SSRW) and halo implants have been used as a mean to scale the channel length and to increase the transistor drive current without causing an increase in the off-state leakage current [6]. Typically, retrograde channel doping and halo drain/source architecture improve the short channel effect such as V_{th} roll-off, DIBL, and surface punchthrough leakage current.

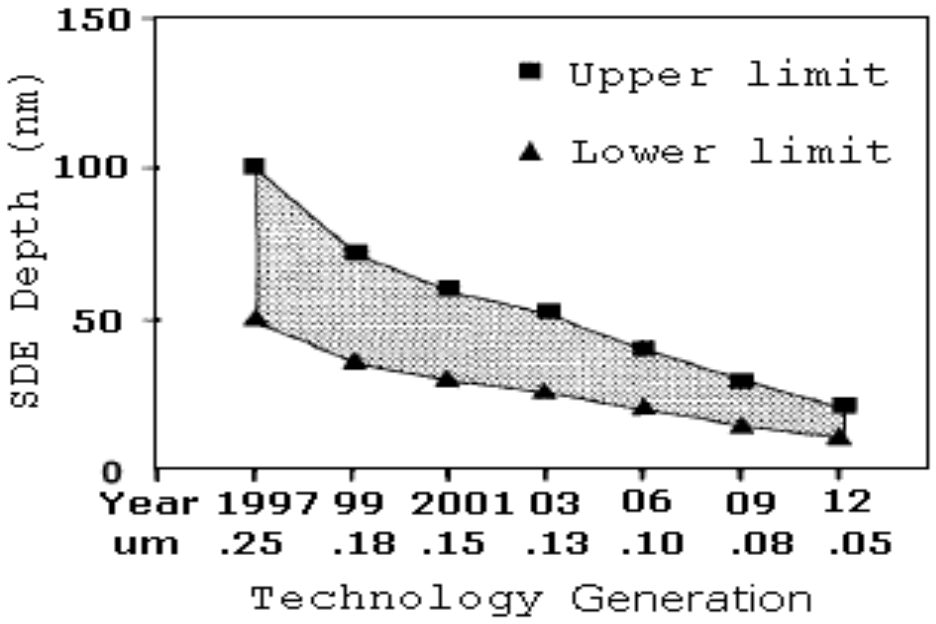


Figure 1.3: *SIA roadmap for junction depth [1]*.

Figure 1.4 is a schematic representation of the transistor regions that are affected by the different types of well engineering. Retrograde well engineering changes the 1D characteristics of the well profile by creating a retrograde profile toward the Si/SiO_2 surface. Typically, SSRW well profiles are created by indium (NMOS) and arsenic (PMOS) implantation and they have a lower doping atom concentration at the surface of MOSFET channel. The halo architecture creates a localized 2D dopant distribution near

the S/D extension regions. Channel doping optimization and halo architecture can improve circuit gate delay by ~10% for a given technology and support an off-state leakage current of 1nA/μm for a wide range of threshold voltages [1].

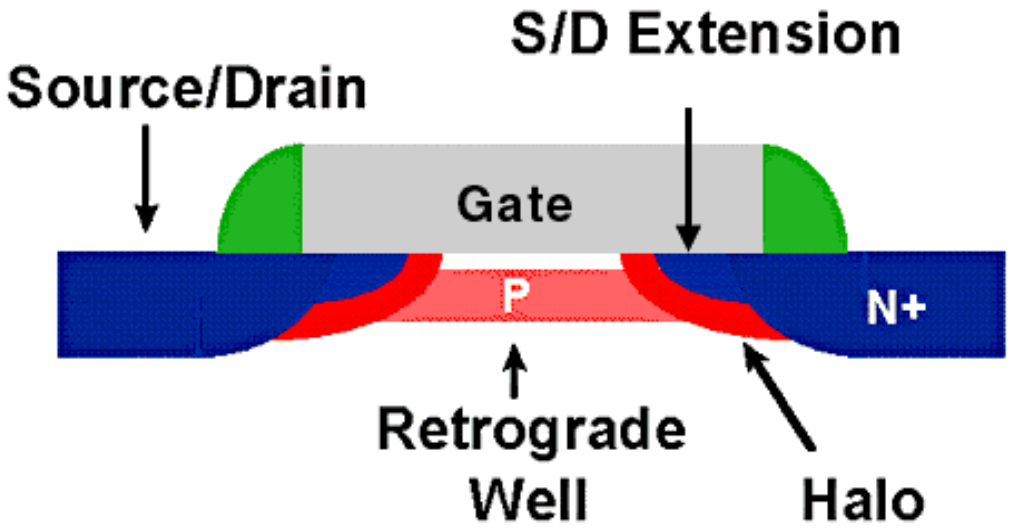


Figure 1.4: *Schematic representation of retrograde channel engineering and halo engineering.*

Power Supply (V_{dd}) and Threshold Voltage (V_{th}) Scaling

The choice of V_{dd} and V_{th} will be critical in determining whether the performance of 0.1 μm transistors can continue to be scaled. These parameters strongly affect chip active power, chip standby power, and transistor performance. The loss in the gate over drive (V_{dd} - V_{th}) is becoming so severe that this trend cannot continue without substantial lost in device performance. Figure 1.5 shows power supply and threshold voltage trends for Intel microprocessor process technologies. As seen, the power supply is decreasing much more rapidly than threshold voltage. This has strong implications for device performance. Transistor drive current and therefore circuit performance is proportional to gate over

drive (V_{dd} - V_{th}) raised to the power of "n", where "n" is between 1 and 2 [$(V_{dd} - V_{th})^n$]. In Figure 1.5, the gate over drive is shown to be rapidly decreasing for deep sub-micron devices, thereby strongly degrading device performance. As discussed previously, aggressive oxide scaling, Source/Drain and channel engineering are used to overcome the loss in gate drive and to maintain the historical rate of transistor improvement. Other fundamental limitation of threshold voltage scaling is sub-threshold leakage current. To maintain acceptable leakage values, the V_{th} of transistor need to increase by > 0.25 V [2].

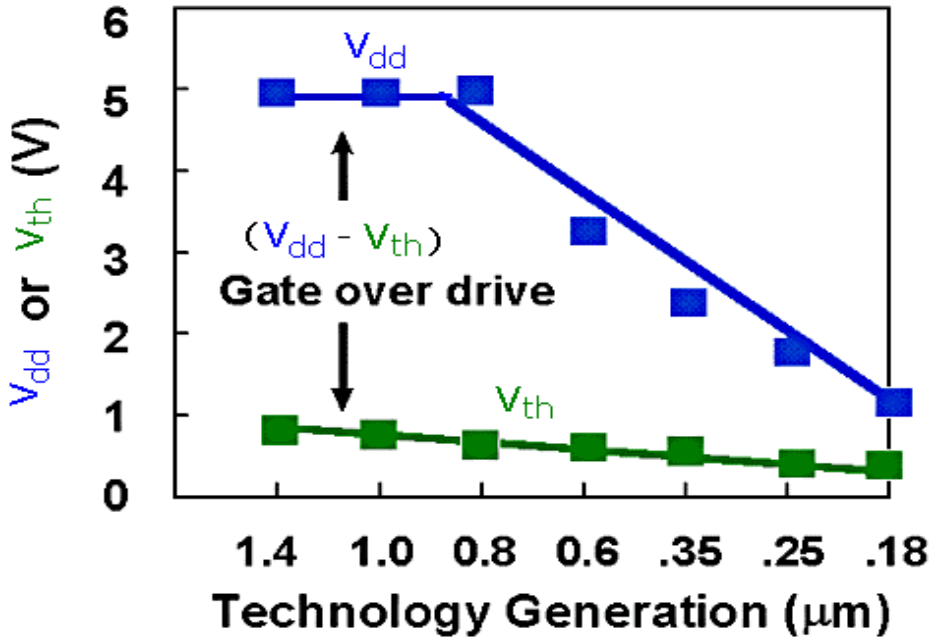


Figure 1.5: *Power supply and threshold voltage scaling trend [1].*

1.3 Interconnect Technology Scaling and Reliability

Downsizing of components in ultra large scale integrated (ULSI) circuits has continuously driven the progress of ULSI capability in terms of information processing density and complexity as shown in Figure 1.6. Transistor scaling provides improvement in processing speed of ULSI circuits. However, interconnect scaling provides higher

interconnect density at the cost of degraded interconnect delay as shown in Figure 1.7. Interconnect delay had not been an issue when the feature size was greater than 0.5 μm. However, the interconnect delay is now a significant fraction of clock cycle time due to the increase of coupling capacitance and interconnect length. This results in a significant impact on overall chip performance. Therefore, advanced interconnect technologies are necessary to overcome the interconnect delay.

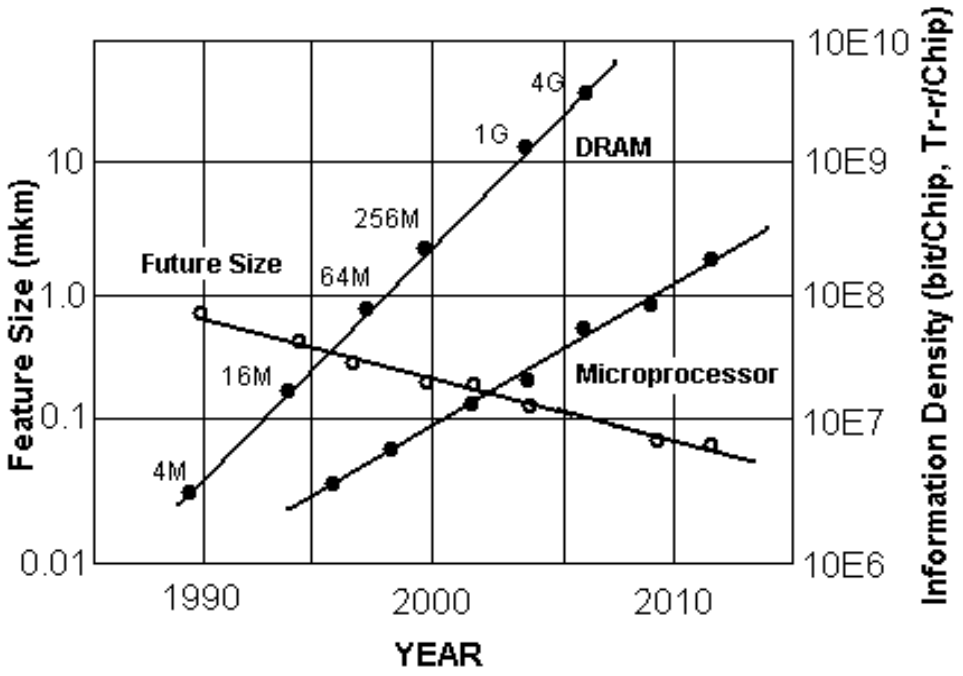


Figure 1.6: *ULSI trends of feature size and information density in DRAM and microprocessors [7]*

A simple first-order model can be used to estimate interconnect RC delay. Assuming that the minimum metal pitch equals twice the metal width, and assuming that the dielectric thickness above and below a metal line equals the thickness of the metal line, the following equation can be used to estimate RC delay [8]:

$$RC = 2\rho\varepsilon\varepsilon_0\left(4L^2/P^2 + L^2/T^2\right) \tag{1.1}$$

Where

R = total line resistance [Ohm]; T = metal thickness [m]; ε = dielectric constant;

ρ = metal resistivity [Ohm-m]; C = total line capacitance [F]; ε_0 = permitivity of free

L = line length [m]; P = interconnect pitch [m]; space [F/m].

Reducing the inter level dielectric constant (ε) will improve interconnect delay and reduce AC (dynamic) power consumption. Silicon dioxide (SiO_2), which has a dielectric constant of 4, is the standard dielectric, which is used today.

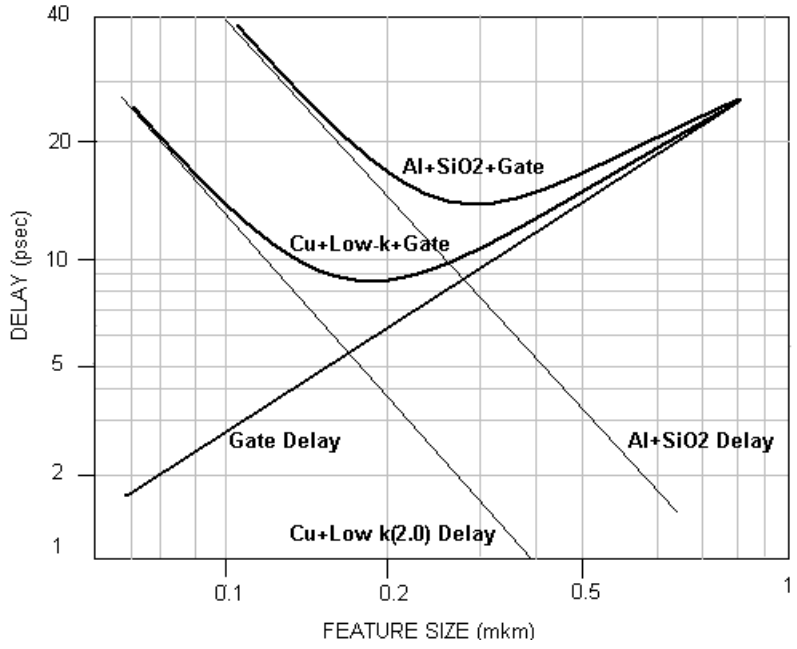


Figure 1.7: *Gate and interconnect delays as a function of feature size: Cu+Low-k versus Al+SiO_2 [7]*

Many low-ε alternatives are being investigated, including fluorine-doped SiO_2 (ε = 3.2 - 3.5), polymers (ε = 2.2 - 2.4) and aerogels (ε ~ 2.1), with the best, providing almost a factor of 2 reduction in ε [4]. Interconnect delay is directly proportional to the dielectric

constant, so being able to reduce ε from 4 to 2 can have a significant impact on overall circuit performance.

Copper is an attractive substitute for standard aluminum interconnects due to its lower resistivity and improved electromigration resistance. The resistivity of pure Cu is 1.7 μOhm-cm compared to 3.0 μOhm-cm for Al - 0.5%Cu alloys typically used. Cu interconnects have also demonstrated electromigration resistance in the order of 10x better than Al interconnects [9]. As shown in Figure 1.7 only the use of Cu as a conductor and low-k dielectric as the dielectric material can provide the significantly lower delay time required for advanced circuits and save ~ 2 - 4 layers of interconnects [8].

Interconnects Reliability

Modern IC metals use aluminum (Al) alloys with line widths, heights, and spacing ranging from 1 μm down to a leading edge of 0.2 μm. Al interconnects are typically lined on the top and bottom by a thin protective layer of tungsten (W) or titanium nitride (TiN) metal, referred to as a liner, cap, or barrier metal. Advanced ICs may have seven levels of metal and total number of vias can reach 100 millions [10]. Metal must be made without defects and must not fail over time. One of the main reasons of metal line degradation is electromigration (EM). EM is the net movement of metal under the influence of electron flow and temperature gradient. EM failure modes can be opens, bridges, or high series resistance in the line. Figure 1.8 shows typical failure sites in chemical vapor deposited (CVD) Cu lines. Many void-hillock pairs are widely distributed along the line, with a distance of 10-20 μm separating the void and hillock in a pair [11].

Metal failure due to EM is measured as the average time to failure (T_F) of a group of metal test structures and is estimated using Black's Law [12]:

$$T_F = \frac{A}{j_e^2} \exp\left(E_a / kT\right) \quad (1.2)$$

Where E_a is failure activation energy, k is Boltzmann's constant, T is temperature (K), j_e is electron current density, and A is a technology-dependent constant. Historically, a DC design rule kept $j_e < 1$ mA/μm^2 [10]. Black's Law predicts that recent IC trends of high operating temperature will weaken metal reliability. E_a is an indicator of metal quality, identifying probable diffusion paths. Typically, E_a variation from 0.4 to 0.6 eV indicates poor metal quality and that grain boundary diffusion may be dominant for that metal. Measurements and calculations with pure Al crystals give $E_a \approx 1.48$ eV [12].

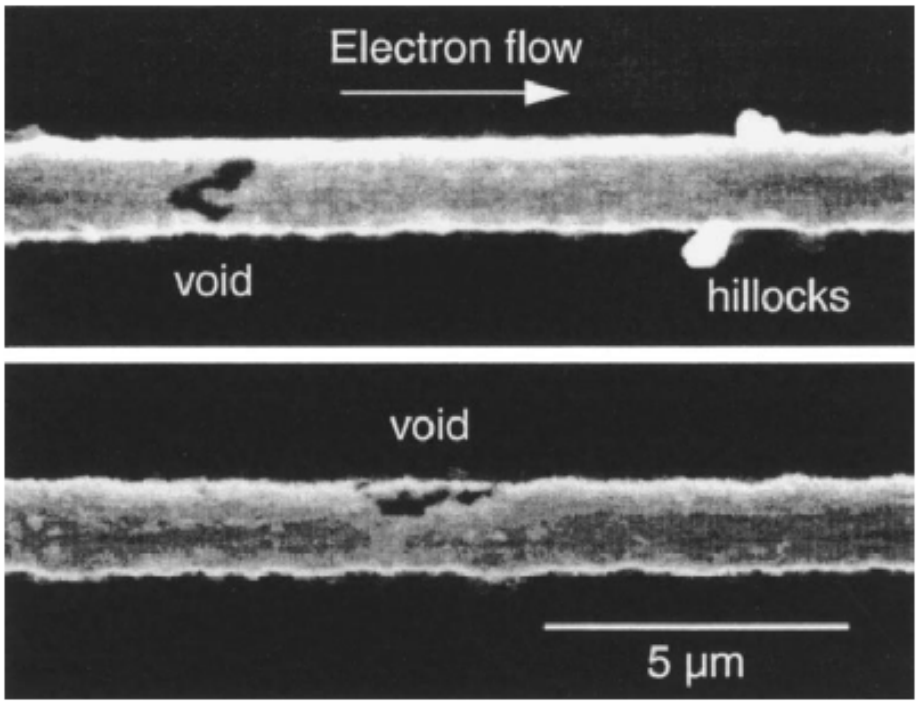


Figure 1.8: *SEM micrographs of failure sites in CVD Cu lines stressed at 238 C with current density of 8 MA/cm^2 [10].*

New IC package temperatures may be around T ≈ 100 C, with even hotter spots on the die. High operating temperature is significant, since diffusion is the transport mechanism for EM failure modes. The temperature at any location on the die is a

function of the instantaneous circuit activity and its thermal impedance. Low-k dielectric material is good for speed, but have poor thermal conductivity. High temperature is bad for Al and Cu lines (Figure 1.9).

Interconnect metals are dynamically sensitive to electron current density, temperature, dissimilar material interface, and grain structure. The dominance of metal structure in new IC designs makes this an exciting subject. Test engineers need innovative techniques to detect these subtle metal defects.

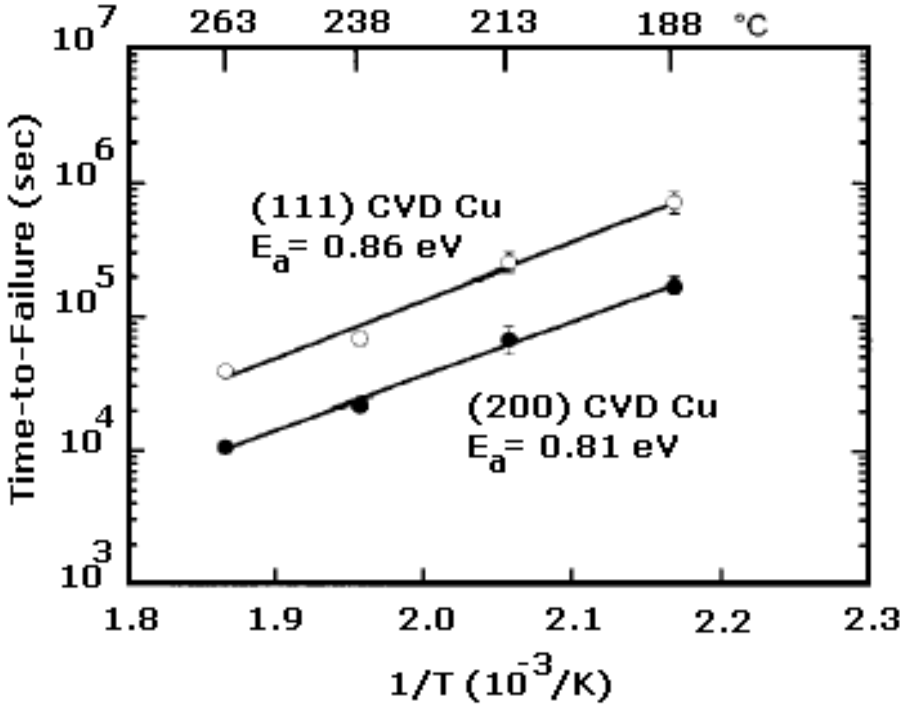


Figure 1.9: *Arrhenius plot of Time-to-Failure for (111) and (200) textures of CVD Cu. The stress current density is 8 MA/cm^2 [10].*

1.4 Defect Classes in CMOS Circuits

This section presents data on the electrical behavior of defect classes, which then form the basis for an optimal test strategy. Three general categories of defect classes are

bridge, open circuit, and parametric defects causing delay that may not be bridge or open circuit defects.

Bridge Defects

Bridge defects at transistor nodes, logic gate I/O, and power bus circuit hierarchies may occur in a combinational or sequential circuit. Bridge defects include all defects and failure mechanisms that cause unintended electrical connections across two or more circuit nodes. Bridges have nonlinear or linear (ohmic) I-V properties with resistance from near zero to > 1 MOhm [13]. Nonlinear bridge defects include most types of gate oxide short, soft p-n junctions, and transistor punch-through. Ohmic shorts also occur in IC patterning defects that leave "bridges" of metal (or polysilicon) and in certain forms of gate oxide shorts. Bridge defect resistance is the dominant factor in bridge detection methods. Correct Boolean functionality exists for signal node bridge defects when the defect exceeds a critical resistance. Critical resistance is a function of the contending transistor current drive strength and therefore varies with circuit design, logic input levels to contending logic gates, and process variation. Critical resistance may lie in a range as low as 10 Ohms to about 5 KOhms [13]. There are several bridge defect classes: transistor node shorts, signal node to power bus, power bus to power bus, shorts inside of logic gate, and shorts between two logic gates. The last kind of bridge defect is presented in Figure 1.10 and it will be analyzed in details in the next two chapters. Typically, voltage and current test methods are used for bridging fault detection.

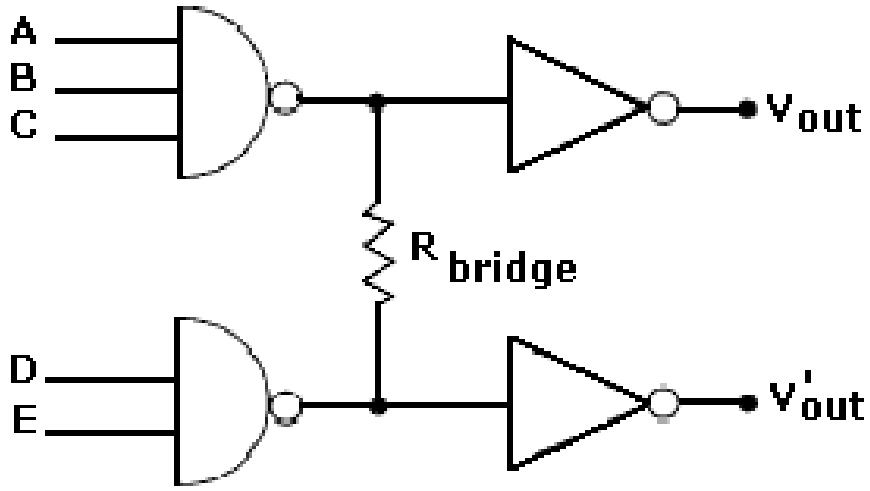


Figure 1.10: *3-NAND to 2 NAND bridge defect.*

Open Circuit Defect Class

Open circuit defects are unintentional electrical discontinuities. They can cause behavior that may be very difficult to predict. These defects include open contacts (missing metal or unopened oxide), metallization opens (patterning, improper etching, electromigration, or stress voiding), or opens in diffusion or polysilicon (mask or fabrication errors). Open circuit defect properties depend primarily on defect size, defect location, local electrical structure, and process variable.

Figure 1.11 shows the effect of defect location when the open circuit (node V_{def}) is in the gate of a single transistor. The logic gate output voltage V_{out} is a function of the signal drive to the complementary transistor and the bias state of the defective transistor. This defect was analyzed with test chip in [14]. An open to a single transistor allows strong capacitive coupling between the drain, gate, and the source. The single transistor open circuit mentioned here has an I_{ddq} increase in one logic state and is 100% detectable by

I_{ddq} test method. However, Open-drain and Open-source defects have the probability of detecting using I_{ddq} testing is rather low.

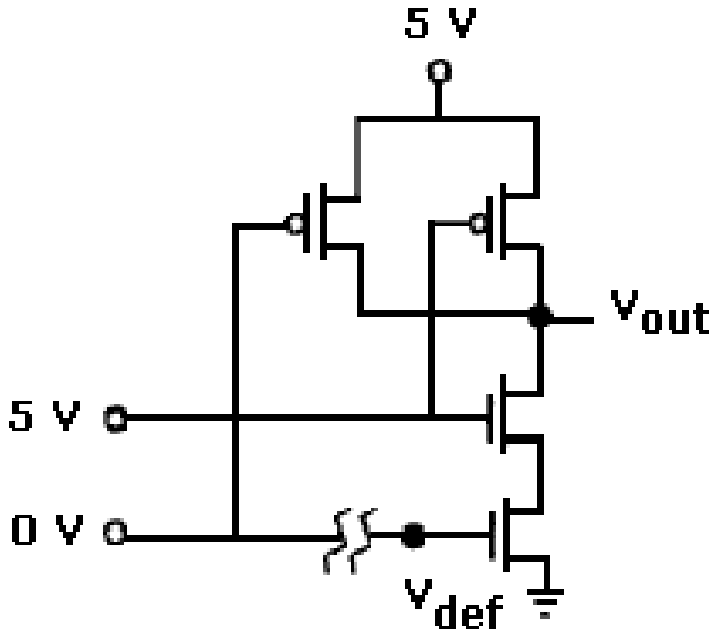


Figure 1.11: *Open gate defect.*

Parametric Delay Defect Class

"Parametric Delay Defects" defines a class of delay defects that typically is neither in the category of bridges or opens, although many open and bridge defects cause delay. It is difficult to detect the defects in this class. Defects cause delay in CMOS ICs in two ways: (1) weakening of logic levels, (2) alteration of parameters in signal transmission paths such as via resistance, transistor threshold, W/L variation of MOSFET, etc.

Figure 1.12 (a) shows a 3-inverter circuit in which the logic level drive on node V1 was weakened by adjusting V_{dd1} of the first inverter. Figure 1.12 (b) shows SPICE simulation result of the increased propagation delay versus weak voltage drive on V_1 [13].

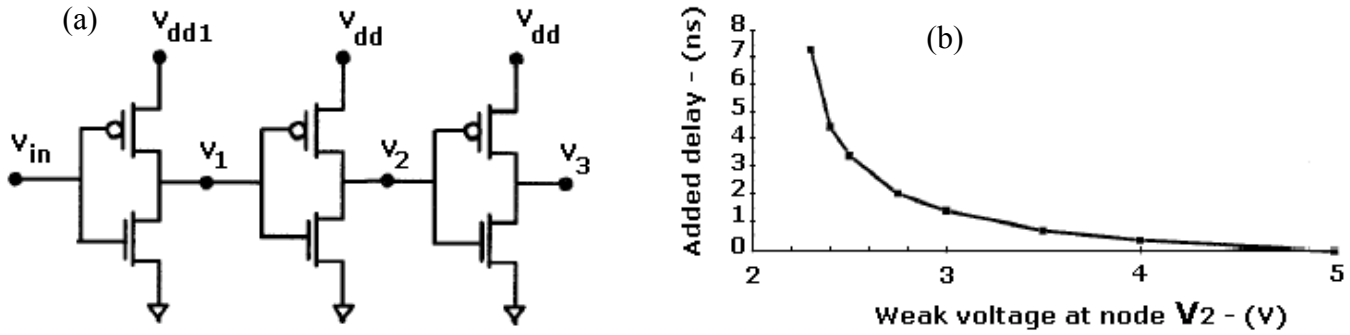


Figure 1.12: *(a) - 3-inverter circuit with weak voltage at V_1; (b) - additional propagation delay time versus weak voltage for 3-inverter [13].*

I_{ddq} test method will detect this defect when the weak voltage drive gets into subthreshold region since both transistor pairs will be in a conduction state. Parametric delay defect detection with a Boolean delay fault simulator is possible in principle, but many defects in this class are not detected by existing voltage sensing and delay test methods. This defect class has either too low an error signal or too high a computational complexity when all possible defect sites are considered. Estimated coverage for this class will remain elusive until more creative test approaches are proven that can examine specific defect sites, such as via integrity. Nontarget tests, such as at-speed Boolean methods, are the available tests. Other tests, such as the transient power supply current test, I_{ddt}, require further research to describe their capabilities [15].

1.6 Conclusion

Aggressive MOS transistor scaling is offering benefits in density, speed, and power. Additional layers of metal are helping to meet the increasingly important need for interconnect density and performance. New conductor and dielectric materials, as well as improved device and circuit design techniques will be needed to meet future ULSI

interconnect requirements. However, the reliability of advanced material is not well characterized yet. Thus there is increased risk that new failure modes will be discovered, which require new reliability solutions and novel test-detection techniques. Increases in transistor count and die size mean lower die yield and higher costs. Fast CMOS technology scaling reduces the effectiveness of conventional test techniques such as logic and current testing because of the reducing logic margin and defect-free leakage current. In addition, design and testing for deep submicron circuits will be dominated by interconnect delays, gate delays and leakage currents. Therefore, we will need to change and improve the way we test chips.

Controlling manufacturing and test equipment costs is a big challenge for the industry as well as scaling transistors and interconnects. Process complexity, test and process equipment costs are growing rapidly due to rigorous technical requirements and increased operating frequency of advanced CMOS circuits. In this situation, the defect density reduction and advanced test methods need to achieve economical die yields.

Chapter 2: Current Testing of Bridging Faults: Possibilities and Limitations

2.1 I_{ddq} testing: Basic concepts

A large class of frequent defects causes a significant increase of the quiescent current in digital CMOS technologies with low supply quiescent current. This fact is the basic principle allowing the discrimination between defective and non-defective chips by comparing the current consumed by the chip with a pre-selected I_{ddq} test threshold. If the circuit under test (CUT) consumes less quiescent current than this threshold level the CUT is accepted. Otherwise, it is rejected. In Figure 2.1, the quiescent current histogram for the chips of a production lot is shown [16].

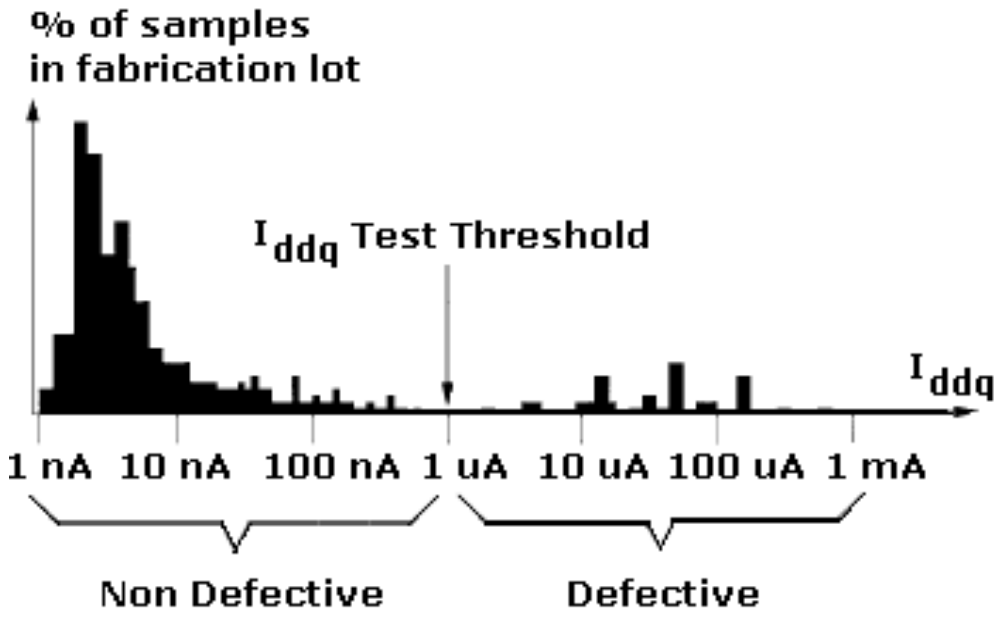


Figure 2.1: *I_{ddq} histogram of a fabrication lot.*

Note that some defective chips show high consumption above the I_{ddq} threshold whereas others have acceptable reduced consumption. The detection of abnormal quiescent consumption requires special sensing circuitry to perform the required comparison. A

wide spectrum of solutions is currently being used, ranging from off-chip sensors to built-in current sensors (BICS). Off-chip sensors have advantages in terms of no area overhead, nor delay degradation but their testing speed is limited and the detection of defective devices is reduced as the chip size increases. Consequently, test engineers should give careful consideration to the possible alternatives to decide on the best I_{ddq} testing strategy.

2.2 Bridging fault and its model

A bridging defect appears when two or more lines are, in an undesired way, electrically connected within an integrated circuit. The origin of a bridging defect may appear during the process fabrication or may appear during circuit operation. Two different bridging defect mechanisms can appear, independently of the origin of the defect. The first type of bridge is the vertical bridging defect connecting the bottom layer with the upper layer. The second type of bridge is the horizontal bridging defect producing a connection between two nodes at the same layer.

The bridging defect, typically, cannot be modeled by the stuck-at model approach, since a bridge often does not behave as a permanent stuck node to a logic value [17]. In technologies used in the past, some bridges were modeled as a wired-AND or as a wired-OR function between the two or more undesired connected nodes [18]. In present CMOS technology, this model can not be always applied because of the faulty node voltage dependence on the topology of the resistive network for each input pattern. Bridging defect has impedance value, which in general, is not purely resistive, however, most of them present the resistive component as the predominant. The advanced bridging defect model represents the fault as a resistive path connecting the two bridging nodes (see

Figure 1.10 in chapter 1). The value of bridging resistance may vary significantly due to the wide possibilities of the bridge mechanisms (gate oxide shorts, soft p-n junctions, transistor punchthrough, physical bridge shorts) [19].

2.3 I_{ddq} testing of bridging faults

A bridging defect connecting two nodes within a particular CMOS circuit may produce an abnormally high quiescent current consumption. The example in Figure 2.2 (a) illustrates two CMOS gates with a bridging defect connecting nodes n_A and n_B. In order to create a high I_{ddq} value, one condition must be satisfied as reported in [20]: the bridging nodes have to be driven to opposite logic values. Depending on the resistance value of the defect (R_b), the current consumption may vary (see Figure 2.2 (b), where $n_A = 0$ and $n_B = 1$).

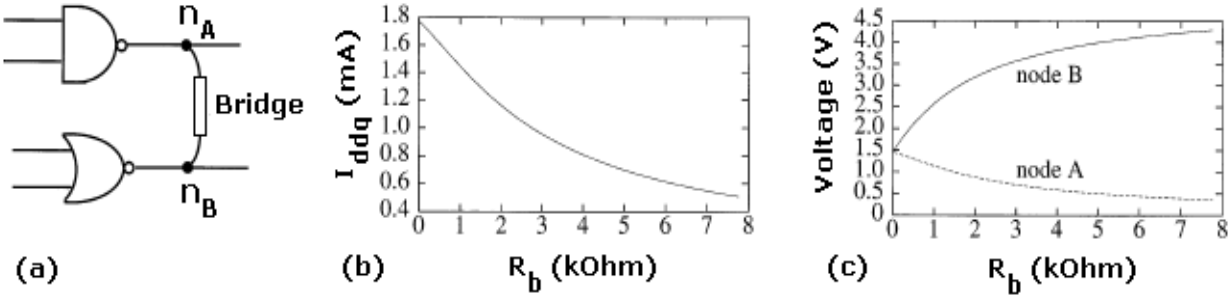


Figure 2.2: *(a) Bridge connecting nodes n_A and n_B of two different CMOS gates and its (b) I_{ddq} consumption and (c) output node voltages [21].*

The prediction of the logical effect of the defect is not needed for the I_{ddq} test technique, although it is useful to estimate the contribution to the quiescent consumption of the next defect-free stages. However, the effect of the bridge on the output voltage of the defective gates may present an intermediate value as shown in Figure 2.2 (c).

In a combinational CMOS circuits, if the bridged nodes are not logically independent, a feedback loop may appear in the defective circuit. The feedback may introduce memory elements or ring oscillations depending on the number of logical inversions in the feedback loop and depending on the transistor sizes driving the bridged nodes [22].

In case of the bridge affecting a sequential circuit, the defect has been shown to be able to invalidate an I_{ddq} testing under certain conditions [23]. In these sequential defective circuits, the bridging defect may cause the change of the memorized state in a memory element and thus mask the controllability of the bridged nodes. To solve this limitation, it was proposed I_{ddq} testable flip-flop configurations [24].

2.4 Intrinsic Leakage Current in Deep Submicron CMOS Circuits: Limitation of I_{ddq}

Technology scaling impacts on the testability of deep submicron CMOS integrated circuits, causing high intrinsic leakage variables. This challenges the effectiveness of current based test techniques such as I_{ddq} testing. Table 2.1 compares MOSFET leakage current (I_{off}) for various technologies and shows the increasing leakage of smaller sized deep submicron transistors. This data was obtained under room temperature. Higher clock speed and reduced noise margins reduce coverage of I_{ddq} and other current-based testing methods. This is the serious problem for testing complex ICs like high performance microprocessors.

In this section, the main component of transistor leakage current is characterized - weak inversion current, by simulating this current as a function of channel length, threshold voltage, voltage supply and temperature. The simulation data was obtained

from n-MOSFET simulation in 2-D device simulator "Microtec" [26]. MOSFET parameters, which were used for simulations, are given in Table 2.2.

Technology, µm	**V_{dd}, V**	**T_{ox}, nm**	**V_{th}, V**	**L_{eff}, µm**	**I_{off}, pA/µm**
1.0	5	20	N/A	0.80	4.1E-4
0.8	5	15	0.60	0.55	5.8E-2
0.6	3.3	8	0.58	0.35	0.15
0.35	2.5	6	0.47	0.25	8.9
0.25	1.8	4.5	0.43	0.15	24
0.18	1.6	3	0.40	0.10	86

Table 2.1: *Comparison of process technologies [25].*

Substrate doping, cm^{-3}	5×10^{15} (p - type)
Source/Drain doping, cm^{-3}	9×10^{19} (n - type)
V_{th} adjusted doping, cm^{-3}	1.8×10^{18} (p - type)
Punch - Trough doping, cm^{-3}	5×10^{18} (p - type)
L_{eff}/W, µm/µm	0.12/5
Gate oxide thickness, A	41

Table 2.2: *n-MOSFET technology parameters used for n-MOSFET simulations.*

Subtreshold (Weak Inversion) Leakage Current

Weak inversion or subthreshold conduction current between source and drain in a MOSFET transistor occurs when the gate voltage is below V_{th}. This current typically dominates in modern device off-state leakage due to the low V_{th} [25]. MOSFET SPICE Model Level 3 uses the following equation for subthreshold current calculation [27]:

$$I_{dsoff} = k \frac{W}{L}(\eta - 1)V_t^2 \exp\left(\frac{V_{gs} - V_{th}}{\eta V_t}\right)\left(1 - e^{\frac{-V_{ds}}{V_t}}\right) \qquad (2.1)$$

Where k is the process transconductance parameter ($k = \mu C_{ox}$); V_t is the thermal voltage and η is the constant (typical values of η range from 1 to 2 for submicron MOSFETs). Physically, η signifies the capacitive coupling between the gate and silicon surface. In a common case, η depends on interface trap density capacitance (surface state capacitance, C_{it}), gate oxide capacitance (C_{ox}) and depletion layer capacitance (C_d). Since the gate voltage of MOSFETs is reduced under voltage supply scaling, the depletion layer capacitance is not constant and correction factor (η) is changed. Parameter η is defined as [27]:

$$\eta = 1 + \frac{C_{it}}{C_{ox}} + \frac{C_d}{C_{ox}} = 1 + \frac{\gamma}{2\sqrt{2\phi_s + V_{sb}}} \tag{2.2}$$

Where $2\phi_s$ is the surface potential in a strong inversion mode, V_{sb} is the substrate voltage, γ is the body factor. The source-to-drain (subthreshold) leakage current as a function of temperature and V_{dd} obtained from simulations is presented in Figure 2.3. The analyzed n-MOSFET has subtreshold leakage current ~ 0.5 nA at V_{dd} = 1.8 V and T = 25 C. However, the operating temperature of advanced microprocessors today is increased because of the increased number of transistors in the chip. In this case, the defect free MOSFET may have leakage ~ 2 nA at 60 C and the effectiveness of current test methods is reduced, because the pass/fail current limit is very difficult to detection. An interesting technique takes advantage of the temperature properties of the weak inversion current. Charges move across the channel in the weak inversion state by diffusion whose rate is reduced as temperature is lowered. A calculation using weak inversion model equation showed that I_{off} can be reduced by three to four orders of magnitude for V_{th} = 0.3 V if the measurement temperature is reduced from 22 C to -55 C. Hence the normal I_{ddq} values of

1 - 100 mA can be shrink to 100 nA - 10 μA for the I_{ddq} testing [28]. However, low temperature I_{ddq} testing demands special test equipment.

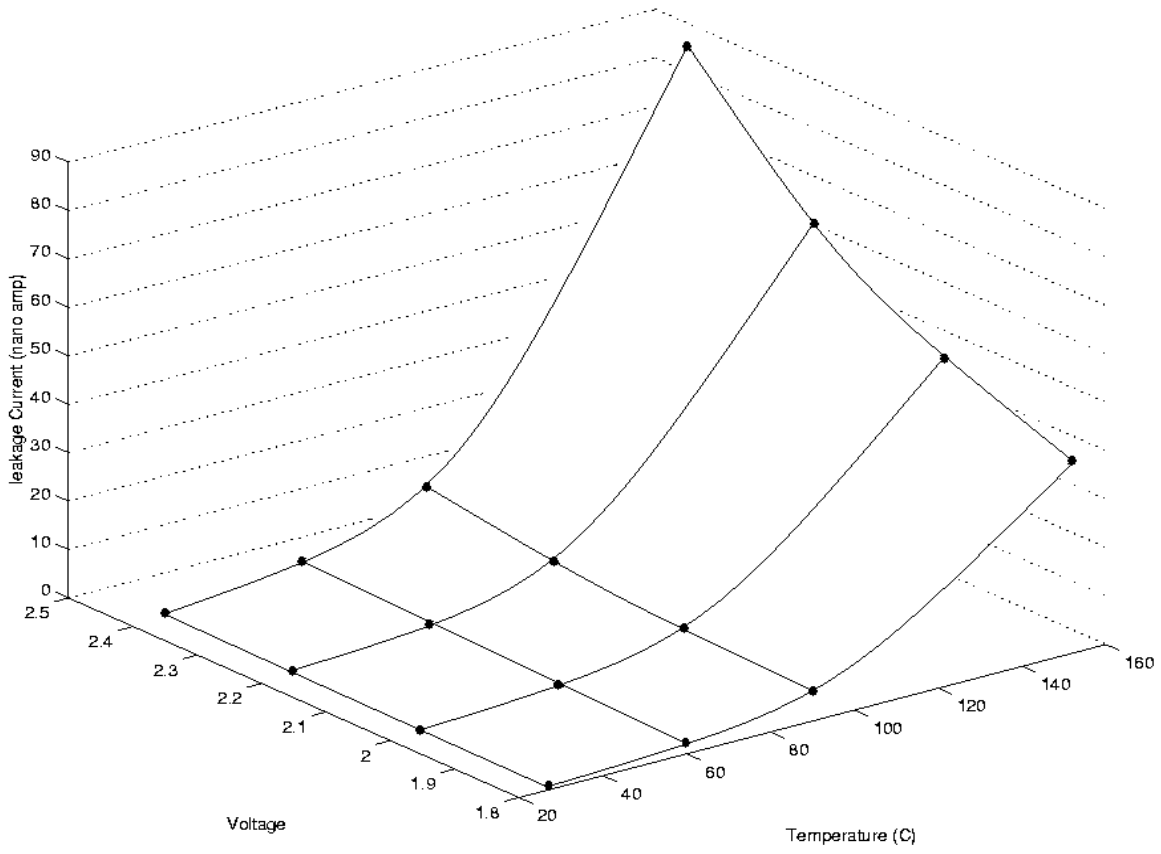


Figure 2.3: *The source-to-drain (subthreshold) leakage current as a function of temperature and* V_{dd}.

2.5 Conclusion

Studies of large numbers of CMOS ICs for last 20 years shown that I_{ddq} testing improves the defect coverage and may detect unique failures, not detectable by any other method. On the other hand, I_{ddq} testing has also some intrinsic limitations:

1) No DC consumption in the IC is allowed. This constrain requires special care by the designer to avoid any high quiescent consumption in the IC which has to be disabled when performing the I_{ddq} test;

2) Slower test application time due to the wait for the I_{ddq} level to settle and then perform the sensing and the comparison of the current level with a I_{ddq} test threshold value;

3) Yield loss due to the rejection of leaky IC's. In future deep submicron technologies, the discriminability of defective and defect-free I_{ddq} currents is expected to decrease and, as a consequence, a new techniques will be required in order to avoid yield loss and, at the same time, reject the defective circuits [16].

However, the main problem of I_{ddq} testing is the significant increase of non-defective I_{ddq} currents, when scaling down the technology will make the test for defective devices more difficult. Especially in high performance circuits, which are typically high leaky circuits, the defective chip I_{ddq} current may have similar quiescent current as the defect free. The mentioned limitations of I_{ddq} testing stimulate the development of logic testing approach for deep submicron CMOS ICs.

Chapter 3: Impact of CMOS Technology Scaling on Bridging Fault (BF) Detection in Sequential and Combinational CMOS Circuits

3.1 Introduction

The IC manufacturing process involves a sequence of basic processing steps, which are performed on sets of wafers. The outcome of manufacturing operations depends on three major factors: the process route which describes the sequence of fabrication steps and the process controlling parameters, the geometry of the fabricated IC, or layout and some randomly changing environmental factors, called disturbances. The control of a manufacturing operation is the set of parameters, which can be manipulated in order to achieve some desired change in the fabricated IC structure. The disturbances are environmental factors that cause variations in the outcome of a manufacturing operation.

This chapter is devoted to the research of a common cause of failure in CMOS digital ICs: the bridging fault (BF), which can be a major failure in ICs [29]. We describe the main technological reasons of BFs in ICs and their influence on the physical behavior of CMOS digital circuits. The parametric model of BFs was used to classify the BF resistance values. This is a general model, which can also include transistor stuck-on and stuck-at faults. We analyze the influence of BF on logic margin and logic swing of CMOS sequential IC under different operating temperatures, power supply voltages and frequencies and estimate the sensitivity of CMOS digital IC to BF under different technological layout sizes (0.25 μm, 0.35 μm, 0.5 μm, 1.5 μm). Combinational CMOS benchmark 74X-Series Circuits was analyzed also for 0.25 μm and 0.35 μm technology.

For each analyzed circuit we detected the value of critical resistance (R_b) and BF resistance under which the logic levels are reduced at 10% from the standard level. These values were detected for different operating temperatures, voltage supply values and technological feature sizes. DC and AC analysis methods were used for the estimation of critical resistance values in a circuit. In the case of AC method the circuit simulation was carried out on operating frequency, which reached 60 - 70% of the maximum value for the given technology.

The trend projections of design and test characteristics are regularly published in the National Technology Roadmap for Semiconductors [30]. This review shows that in this decade transistors will scale down to 0.07-micron geometry, enabling the manufacturing of large memories and microprocessors. Another important factor is the increasing number of metal layers. It influences on the types of tests and defect screening methods. The design and test for deep submicron IC will be limited by interconnects. Downsizing of components in ULSI scaling has continuously driven the progress of ULSI capabilities in terms of information processing density and complexity.

The first problem is the development of new fault models. The experimental data shows that there are many new failure modes in deep submicron space, where metal lines are becoming narrow and spacing is becoming smaller. Some of these failure modes are inductive and capacitive. Because the dielectric constants are not improving fast enough, capacitive coupling effects dominate the interconnect delay.

A new technology processes (for example, the process of magnetron sputtering of complex metal films Al-Ti-Si) influences on the metal layer properties for signal wiring and increases probability of BF defects in the connecting lines. The second problem is the

fault localization. For instance, a microprocessor contains over five million transistors and five levels of wiring in a 196-mm^2 area [31]. But the size of nickel particle, which can cause a short between two nodes, may be a 0.3 x 0.4 μm. The failure analysis would locate and identify this defect, knowing only its electrical effects on the chip. Figure 3.1 illustrates the projected increase in device complexity versus the projected decrease in minimum defect size, both relative to 1995 levels. The complexity is the sum of the number of transistors and the total wiring length on the chip [31].

The decreasing of minimum defect size has the influence on accuracy of yield models, which are used to determine the probability that a manufactured semiconductor device performs its function correctly. The problem with the concept of the critical area as a function of the defect size is that the defect size is a random variable and therefore the critical area is a random variable, as well. A typical distribution of the defect size is such that the vast majority of defects have small sizes, but the density of defects is sharply increased with the decrease of the defect size. But on other hand, small defects may, or may not cause failure. Consequently, inadequate estimation of the critical area for ultra deep submicron (UDSM) technology may lead to a large error in yield estimation. As a result of technology scaling of MOS transistor dimensions, transistor characteristics can not be accurately modeled using the classical approach without recourse to a large number of empirical parameters. Various physical effects must be considered for UDSM modeling, such as quantization of the immersion layer carrier, mobility degradation, carrier velocity saturation and overshoot, and vertical and lateral doping profiles.

In this chapter, we show that the scaling of technology not only increases the sensitivity of IC to bridging defects but also their detection becomes harder. Thus using AC test method of BF defects is important for high performance testing of complex ICs.

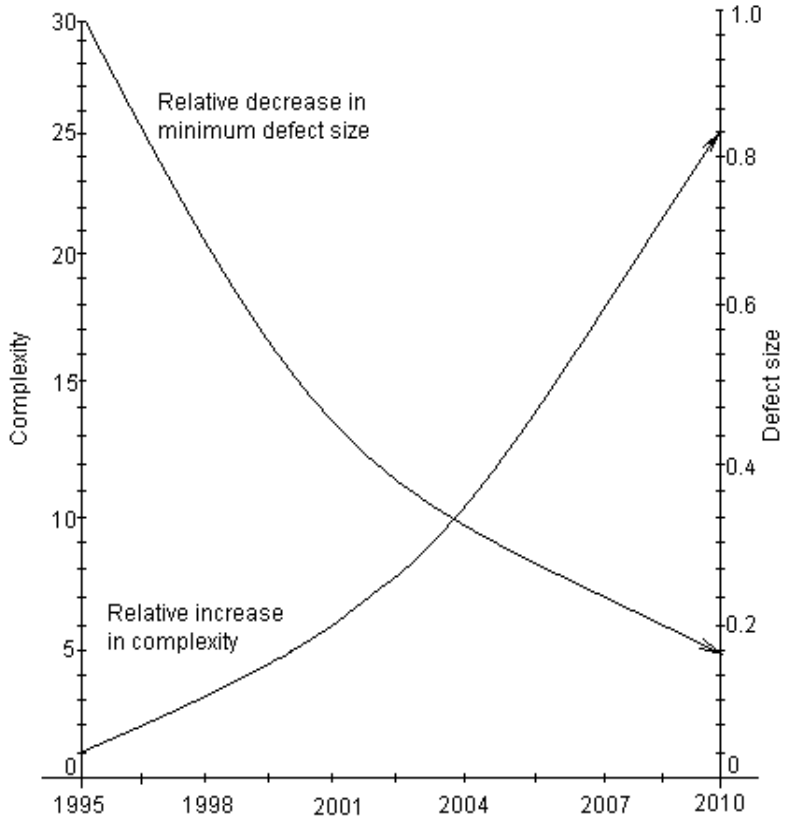


Figure 3.1: *Projected increases in relative complexity versus minimum defect size.*

3.2 The Description of the Analyzed Circuit

We analyzed the electrical effects of a resistive short located between two chains of two CMOS flip-flops and one inverter. The first chain had a steady high level state flip-flop and inverter (constant logic level «1») and the second chain had a steady low level state flip-flop and inverter (constant logic level «0»), as shown in Figure 3.2. This is a DC analysis technique, which analyses the static behavior of circuits. AC analysis

technique analyses the dynamic behavior of circuits when both the data and clock signals are changing together. We used this method for evaluation of BF defects influence on circuit operating in a dynamic mode. The schematic of static D-flip-flop, which was used in analyzed circuit, is presented in Figure 3.3.

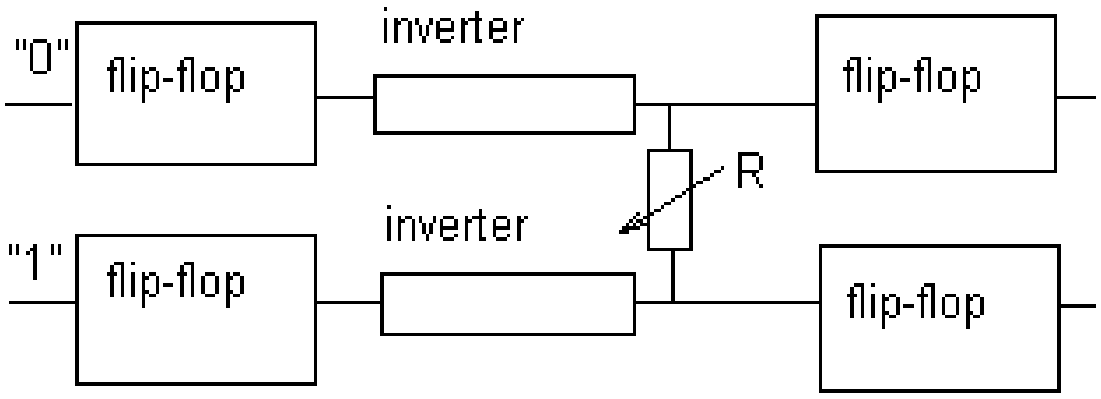


Figure 3.2: *The electrical circuit for a bridging fault analysis (DC analysis).*

All simulations were carried out in the HSPICE environment in CADENCE. This is a special model, which includes the mobility degradation, velocity saturation and other short channel effects of transistor operation. We performed circuit simulation for 0.25, 0.35, 0.5 and 1.5 μm CMOS technology.

3.3 Bridging Fault Analysis in Sequential CMOS ICs

The first step was to detect the maximum operating frequency of analyzed circuit for four different CMOS technologies. Dimensions of transistors used for the simulations are shown in Table 3.1. We chose dimensions of transistors so that the ratio of width and length of n-channel and p-channel transistors are approximately similar for each technology.

We did not try to optimize the dimensions of transistors for the receiving of maximum possible frequency. The maximum operating frequency (f_{max}) of analyzed IC with traditional dimension of transistors was defined for each technology. The operating clock frequency ($f_{operating}$) was chosen as (0.5 - 0.7) * f_{max}, because we assumed that the circuit operated robustly at this frequency. The calculated results of maximum and operating frequencies are represented in Table 3.2.

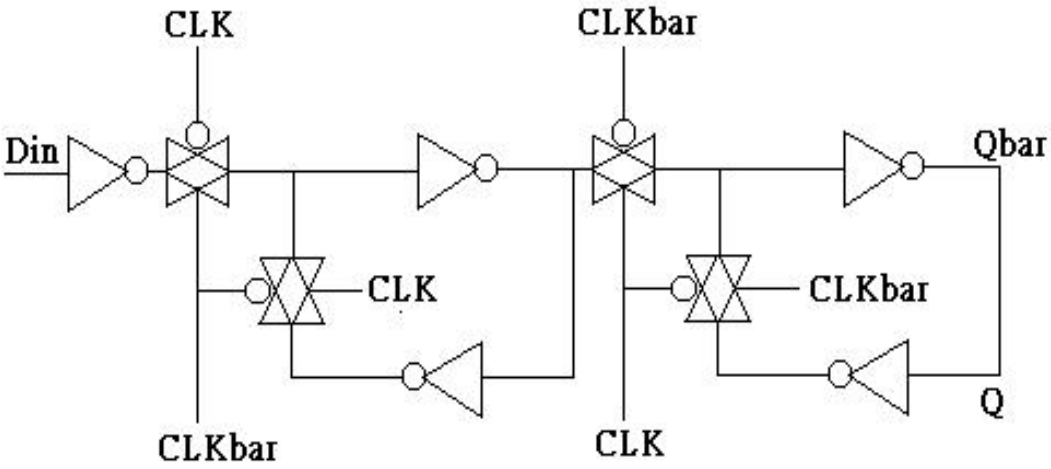


Figure 3.3: *Schematic of static D-flip-flop, which was implemented in analyzed circuit.*

CMOS technology	**The size of n-MOS transistor, K_n = (W/L)**	**The size of p-MOS transistor, K_p = (W/L)**	**The ratio coefficient: $K = K_p/K_n$**
0.25 µm	2.6 µm/0.25 µm = 10.4	4.4 µm/0.25 µm = 17.6	1.69
0.35 µm	6.3µm/0.35 µm = 18	10.8µm/0.35µm = 31	1.7
0.5 µm	6.8µm/0.6 µm = 11	10.8µm/0.6µm = 18	1.64
1.5 µm	16.5µm/1.5 µm= 11	27µm/1.5µm = 18	1.64

Table 3.1: *Dimensions of transistors used for the simulations.*

The technology scaling improves circuit performance by reducing capacitance and potential swings. When ideal scaling is applied, all horizontal and vertical dimensions of transistors are scaled down by 1/S (S>1 - scaling factor), parasitic gate capacitance ($C_g=[\varepsilon_{ox}*W*L]/t_{g\ ox}$) decreases by 1/S and intrinsic gate delay improves by 1/S. This fact explains the increasing of CMOS IC operating frequency as a result of the reduction of feature size.

CMOS technology	**Maximum frequency, f_{max}, MHz**	**Operating frequency, $f_{operating}$, MHz**
0.25 μm	2100	1500
0.35 μm	1350	750
0.5 μm	1050	650
1.5 μm	400	250

Table 3.2: *Frequencies used for the simulations of IC with BF fault.*

The next step of our research was the DC simulation of CMOS circuit (Fig. 3.2) when the resistor value was changed from 0Ω to 100 KΩ. For this simulation, data is fixed and clock is toggled at $f_{operating}$ in order to excite the bridging fault. We did simulations for three different conditions: 1) *normal operating conditions* - temperature T=25 °C, voltage supplier V_{dd}=2.5V (for 0.25 μm technology), V_{dd}=3.3 (for 0.35 and 0.5 μm technology) or 5 V (for 1.5μm technology); 2) *best operating conditions* - T=0 °C, V_{dd}=2.65, 3.5 or 5.3 V; 3) *worst operating conditions* - T=85°C, V_{dd}= 2.35, 3.1 or 4.7 V. On the basis of DC simulations, we plotted the dependence of logic swing and logic margin on the value of bridging resistor "R". These dependencies are shown in Figure 3.4 for 0.25 μm CMOS technology. From the plots *we defined the value of resistance for each technology and each condition of circuit operation in which the logic level "0" or "1" is reduced by 10%*

from nominal value. Typically, the degradation of logic levels less than 10% is not identified as a logic error. The obtained results are given in Table 3.3 and Figure 3.5. When the resistance of the MOSFET channels becomes very small the V_{dd} predominantly drops on the BF resistor, because R_{NMOS} and R_{PMOS} are very small (BF resistor, R_{NMOS} and R_{PMOS} are connected in series). The resistance of most defects is independent of the voltage applied (typically, BF resistance is less than 10 KOhm [13]), but the MOS transistors channel resistance is a function of V_{gs} and V_{ds} voltages.

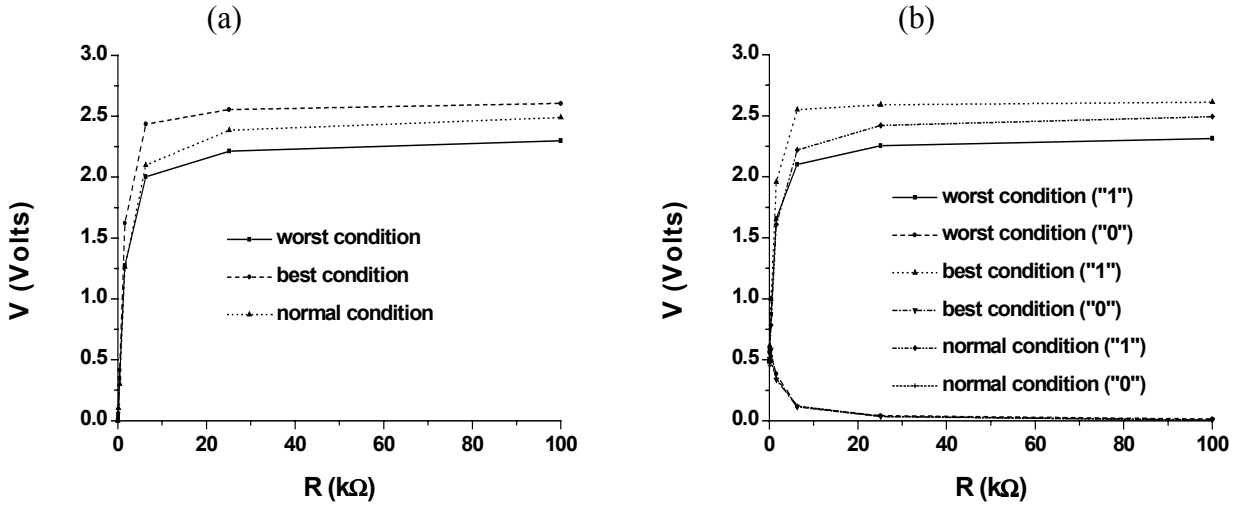


Figure 3.4: *Logic swing (a) and logic margin (b) for 0.25 μm technology.*

CMOS Technology	**Best Conditions**	**Normal Conditions**	**Worst Conditions**
0.25 μm	1.2 KΩ	2.1 KΩ	2.7 KΩ
0.35 μm	1.5 KΩ	2.5 KΩ	3.4 KΩ
0.5 μm	2.2 KΩ	3.0 KΩ	4.1 KΩ
1.5 μm	4.2 KΩ	5.0 KΩ	5.9 KΩ

Table 3.3: *BF resistance values for difference technologies and conditions on which the logic levels are reduced by 10% from nominal value (DC analyses method).*

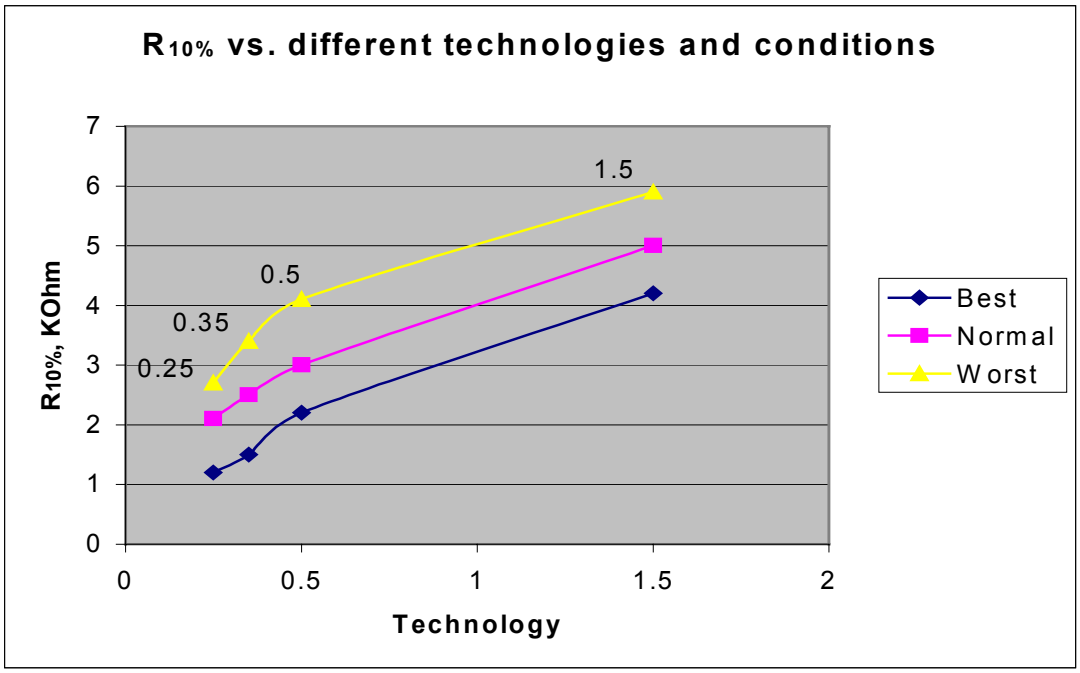


Figure 3.5: *$R_{10\%}$ vs. different technologies and conditions (DC analysis).*

This fact may explain the dependence of critical BF resistance value on disturbance of applied voltage supply. MOS transistor characteristics are strongly temperature dependent. The variation of channel conductance with temperature is due to the variation of the threshold voltage and the inversion layer mobility. The channel conductance is defined by the expression: $G = \mu_{eff} * [W/L]*C_o*(V_G-V_{th})$ [27]. The temperature dependent terms in G are the effective inversion layer mobility μ_{eff} and the threshold voltage V_{Th}. MOSFET transistor generally is operating in the strong inversion mode, where an increase of the operating temperature results an increase in the channel resistance. This fact may be explained by the dependence of critical BF resistance value on variation of operating temperature. The data in Table 3.3 shows that the transistors are becoming weaker with technology scaling, because a smaller defect resistance in smaller geometry causes 10% reduction in the swing.

The last step of our research was the parametric simulation of CMOS circuit under AC conditions (dynamic behavior). In this case both data and clock are changing together. Clock signal had frequency as shown in Table 3.2 (see operating frequency). Data signal parameters were chosen from the circuit robust operating condition. Typically the data signal frequency was 0.5 * f_{max} (clock signal). We defined the critical BF resistance values when output signals of the circuit were totally degraded (circuit did not function). The obtained results are given in Table 3.4 and Figure 3.6.

Typically, the output voltage of the circuit is stable for high defect resistance but it significantly degrades when the resistance is lower than a certain value. *The resistance value where the voltage response crosses $V_{dd}/2$ is called critical resistance*. Usually the output voltage is changed between V_{th} (or V_{dd}- V_{th}) and $V_{dd}/2$. In other cases, reducing BF resistor value more than threshold value results in a logic error and we accepted this value as critical resistance also.

CMOS technology	**Best Conditions**	**Normal Conditions**	**Worst Conditions**
0.25 µm	900 Ω	1100 Ω	1800 Ω
0.35 µm	700 Ω	750 Ω	950 Ω
0.5 µm	470 Ω	580 Ω	690 Ω
1.5 µm	450 Ω	550 Ω	660 Ω

Table 3.4: *Critical resistance values for different technologies and conditions (AC analysis method).*

The explanation of these results is not trivial. Probably, due to transistor scaling we observe two different processes. On one hand, the IC sensitivity to BF defects is increased (see the results of AC analysis in Table 3.4). It means that the interval [0:$R_{critical}$], when circuit does not work properly is increased under technology scaling.

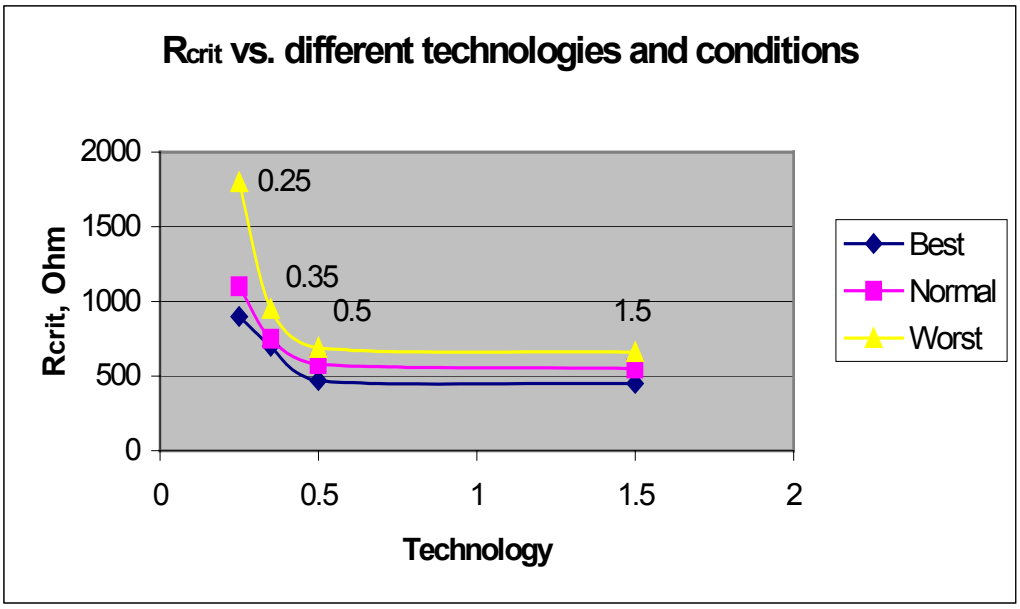


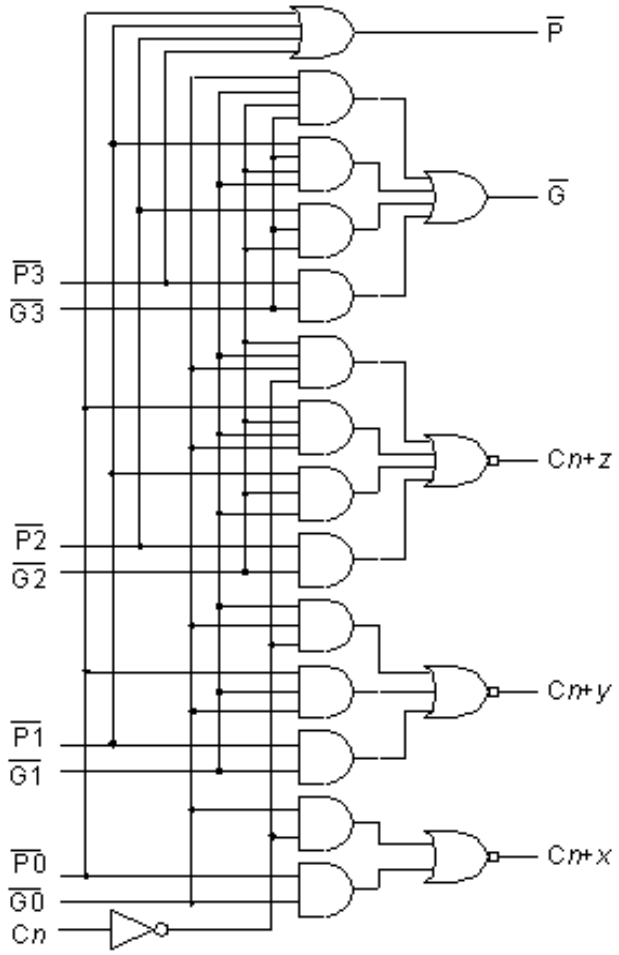
Figure 3.6: *R_{crit} vs. different technologies and conditions (AC analysis).*

The preliminary results of technology scaling impact on BF defects in inverter chain were shown in [32]. On other hand, the downsizing of components in CMOS ICs provides improvement for gate delay [7] (see Figure 1.7). The total delay (gate and interconnect delay) is reduced while the scaling of feature size does not achieve of 0.25 µm technology. In this case the BF delay has the crucial impact on the circuit robustness and R_{crit} is increased with technology scaling (AC conditions). For long channel technologies the gate and interconnect delay dominates and role of BF delay is not so important. It may be the reason of partial compensation of logic levels degradation (as a result of BF influence) and the increase of CMOS IC robustness (critical resistance values for 0.5 µm technology and 1.5 µm technology are not very different).

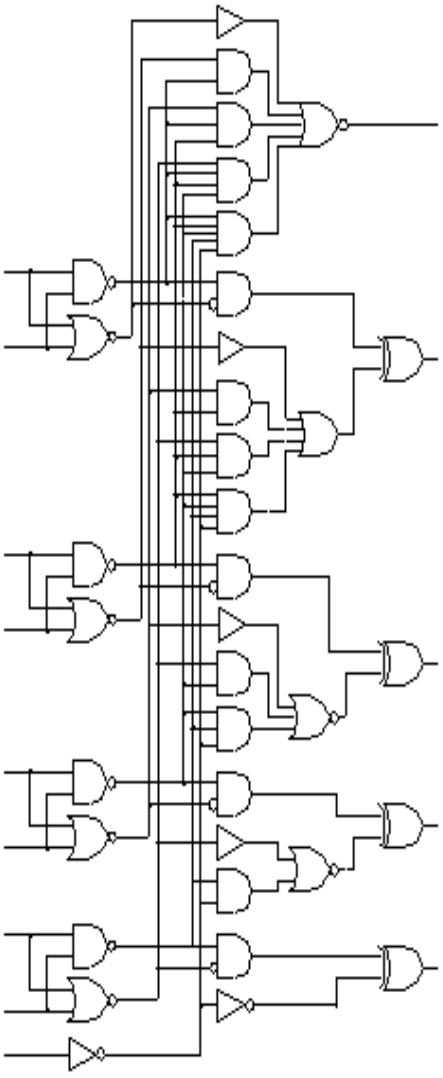
3.4 Bridging Fault Analysis in Combinational Benchmark CMOS ICs

The simple example of combinational benchmark CMOS ICs is a 74X-series circuit. The ISCAS-85 circuits are well-defined and high-level structures and functions are based on common building blocks such as multiplexers, ALUs, adders and decoders. Structural

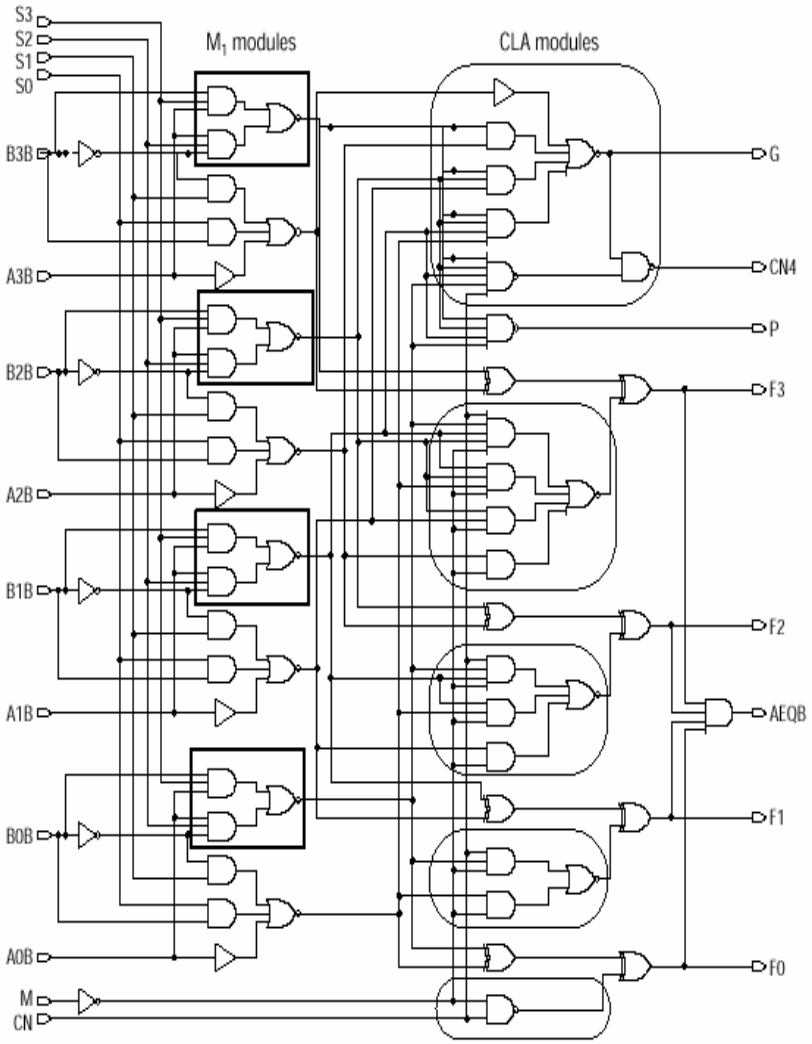
blocks for ISCAS-85 and ISCAS-89 circuits are successfully used in 74X-series circuit [33]. For instance, part of the ISCAS-85 c3540 circuit realizes the same logical and arithmetic functions as the 74181 ALU/function generator. Because the common 74181 ALU has a CLA (carry-look ahead) generator module, it is not surprising to find a similar module in the c880 (8-bit ALU). By this reason we choose the 74X-series circuits as the object of our research. The following circuits were tested: 74182 (4-bit carry-look ahead generator), 74283 (4-bit adder) and 74181 (4-bit ALU). The gate-level schematic for these circuits is presented in Figure 3.7.



(a) 74182 circuit Gate-Level Schematic



(b) 74283 circuit Gate-Level Schematic



(c) 74181 circuit Gate-Level Schematic

Figure 3.7: *Gate-level schematic of used 74X-series circuits.*

The electrical circuit for a BF influence analysis in 74X-series circuits was the same as for sequential circuit (see Figure 3.2). But we substituted flip-flops on combinational benchmark circuits, which were created on the basis of standard logic gates library in Cadence. The maximum and operating frequencies (60-70 % from the maximum value) was detected for 0.35 µm and 0.25 µm technology. The calculated results of maximum and operating frequencies have shown in Table 3.5. The method of critical resistance value detection and resistance value detection under which the logic levels degraded to 10% from the nominal value for different operating temperature, voltages supply and feature technology size is described in section 3.2 and 3.3 of this chapter. The detected resistance values for case of DC analyses ($R_{10\%}$ values) are shown in Table 3.6, Table 3.7 and Figure 3.8. $R_{critical}$ values in these tables were found under AC conditions.

Kind of Circuit	**Statistics**	**Maximum frequency**	**Operating frequency**
74182 : 4-bit carry-look-ahead generator	9 inputs; 5 outputs; 19 gates; test vector: 000001111	0.35 µm technology: 300 MHz 0.25 µm technology: 450 MHz	0.35 µm technology: 200 MHz 0.25 µm technology: 250 MHz
74283 : 4-bit adder	9 inputs; 5 outputs; 36 gates; test vector: 011110000	0.35 µm technology: 300 MHz 0.25 µm technology: 450 MHz	0.35 µm technology: 200 MHz 0.25 µm technology: 250 MHz
74181 : 4-bit ALU	14 inputs; 8 outputs; 61 gates; test vector: 01010000111101	0.35 µm technology: 300 MHz 0.25 µm technology: 450 MHz	0.35 µm technology: 200 MHz 0.25 µm technology: 300 MHz

Table 3.5: *Operating frequencies used for the simulation of combinational benchmark CMOS ICs with BF defect.*

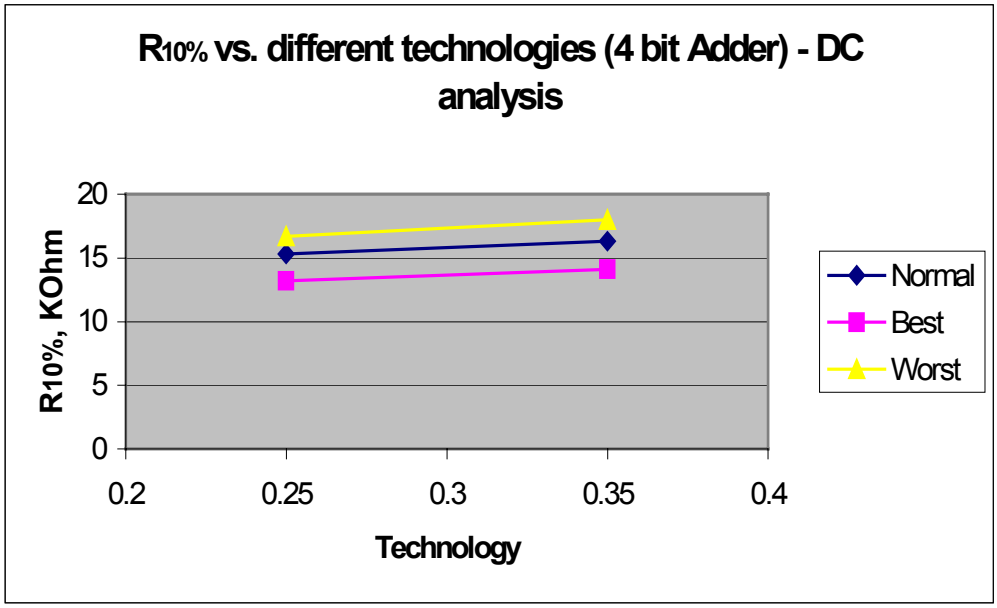
Kind of Circuit	Normal Conditions	Best Conditions	Worst Conditions
74182 : 4-bit CLA	R (10%) = 15.8 KOhm $R_{critical}$ = 1150 Ohm	R (10%) = 13.7 KOhm $R_{critical}$ = 1040 Ohm	R (10%) = 17.5 KOhm $R_{critical}$ = 1270 Ohm
74283 : 4-bit adder	R (10%) = 16.3 KOhm $R_{critical}$ = 660 Ohm	R (10%) = 14.1 KOhm $R_{critical}$ = 580 Ohm	R (10%) = 18.0 KOhm $R_{critical}$ = 780 Ohm
74181 : 4-bit ALU	R (10%) = 16.7 KOhm $R_{critical}$ = 920 Ohm	R (10%) = 14.5 KOhm $R_{critical}$ = 850 Ohm	R (10%) = 17.5 KOhm $R_{critical}$ = 1020 Ohm

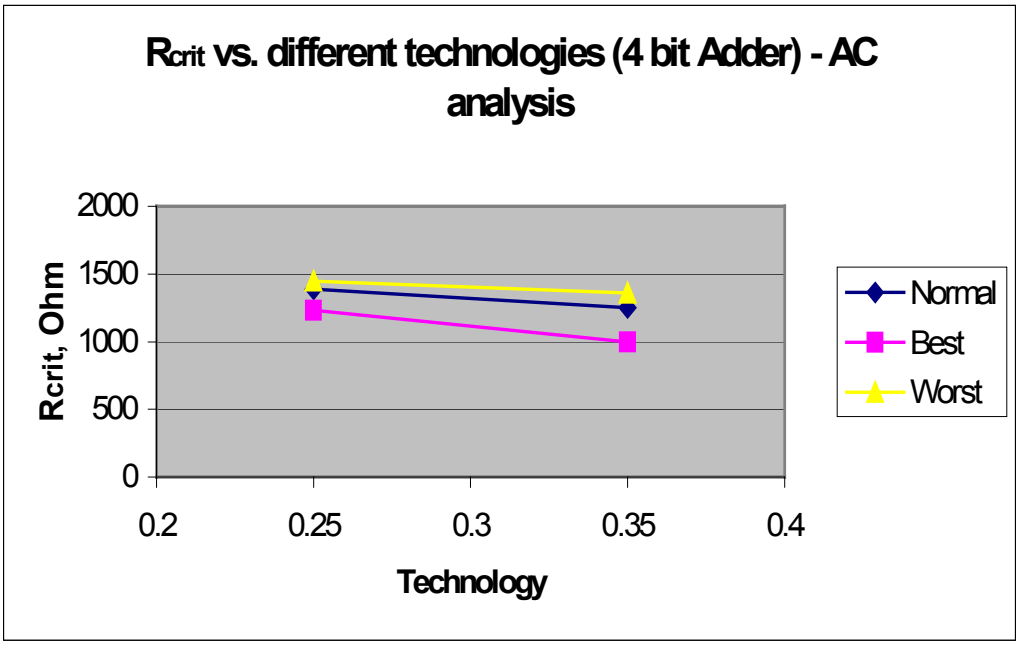
Table 3.6: *DC and AC analyses of BF in 74X-Series Circuits (0.35 µm technology).*

Kind of Circuit	Normal Conditions	Best Conditions	Worst Conditions
74182 : 4-bit CLA	R (10%) = 14.9 KOhm $R_{critical}$ = 1300 Ohm	R (10%) = 12.8 KOhm $R_{critical}$ = 1130 Ohm	R (10%) = 16.2 KOhm $R_{critical}$ = 1380 Ohm
74283 : 4-bit adder	R (10%) = 15.3 KOhm $R_{critical}$ = 890 Ohm	R (10%) = 13.2 KOhm $R_{critical}$ = 780 Ohm	R (10%) = 16.7 KOhm $R_{critical}$ = 930 Ohm
74181 : 4-bit ALU	R (10%) = 10.5 KOhm $R_{critical}$ = 1140 Ohm	R (10%) = 9.4 KOhm $R_{critical}$ = 1060 Ohm	R (10%) = 11.1 KOhm $R_{critical}$ = 1170 Ohm

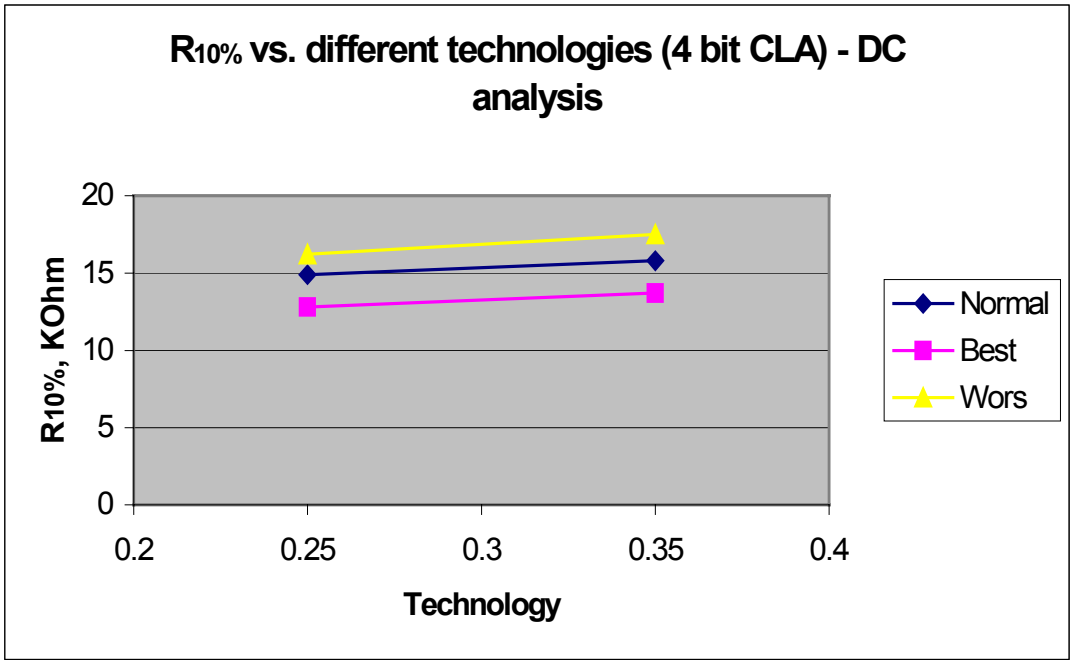
Table 3.7: *DC and AC analyses of BF in 74X-Series Circuits (0.25 µm technology).*

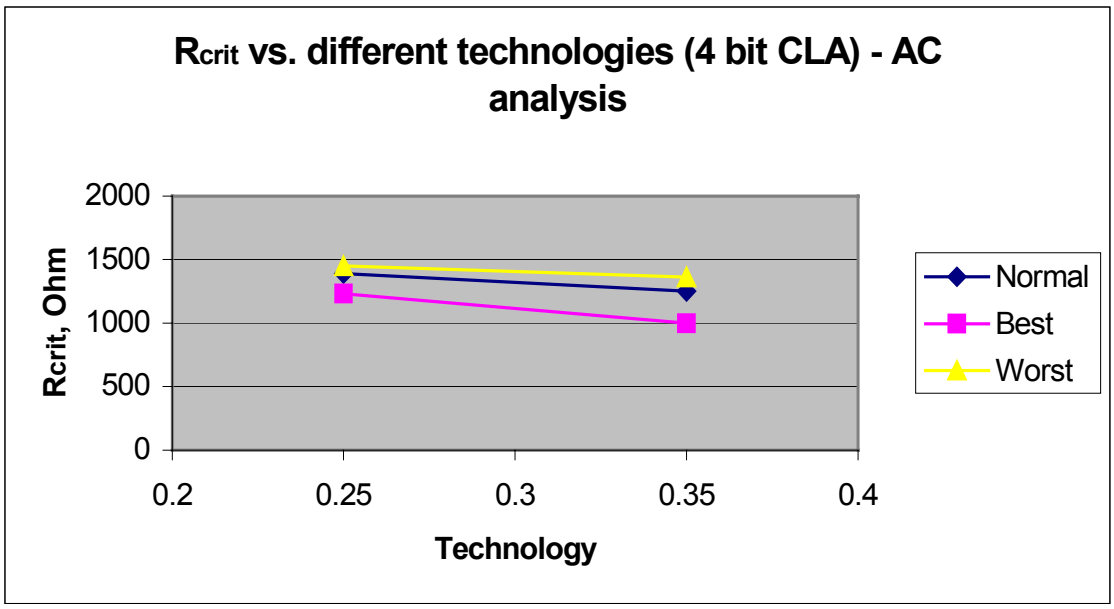
These results indicate that the sensitivity of both combinational and sequential circuits to BF defects are increased under technology scaling and deterioration of operating conditions (because the interval [0:$R_{critical}$], when circuit does not work, is increased in these cases). BFs can result in the same kind of effect as delay faults. Typically, the delay of circuit with BF defect is higher than fault-free circuit [34]. This fact may explain why the circuit becomes more sensitive to BF defect in case of AC analysis.



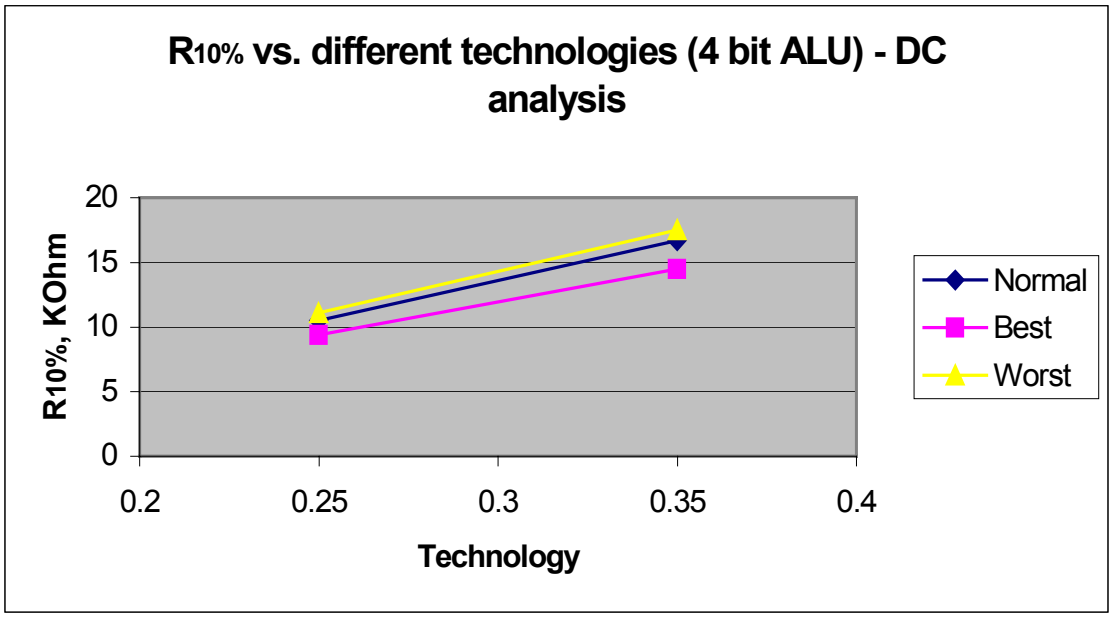


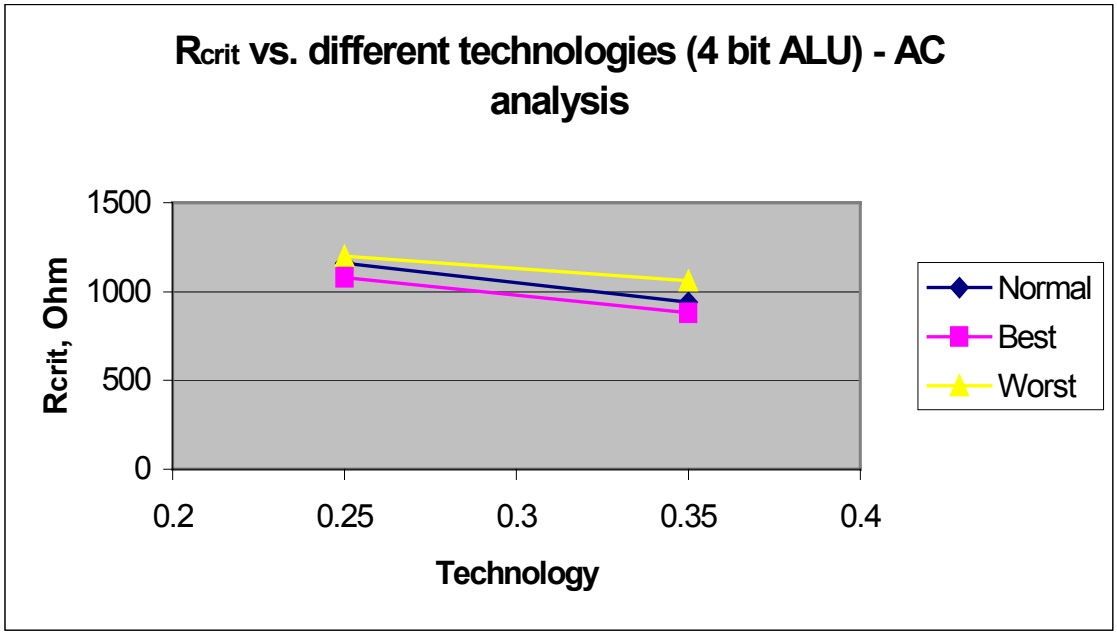
(a) R_{crit} and $R_{10\%}$ vs. technology and conditions (4 bit Adder).





(b) R_{crit} and $R_{10\%}$ vs. technology and conditions (4 bit CLA).





(c) R_{crit} and $R_{10\%}$ vs. technology and conditions (4 bit ALU).

Figure 3.8: *R_{crit} and $R_{10\%}$ vs. technology and conditions for combinational benchmark CMOS circuits.*

Bridging Fault (BF) Detection inside of Combinational Benchmark CMOS Circuits

The same combinational benchmark CMOS circuits (4 bit Adder and 4 bit CLA) were investigated. However, in this case 10 bridging shorts were inserted inside of each analyzed circuit. Initially all resistances were made equal to 100 MOhms in order to ensure that the faults do not cause any logic malfunction and the circuit operates under normal condition. Because the analyzed circuits were benchmark circuits, we had the necessary test vectors for each of BF detection [35]. Initially these vectors were used to excite the circuit and the outputs were noted for normal operating condition. Next, each BF was made equal to 0 Ohms one at a time and test vectors were applied. We noted the input vector and the output net that detected the change in logic functionality. Thus, for each BF the input test vector that detects the fault and an output net that shows a logic change because of the BF were found. *The following parameters were estimated in this investigation:*

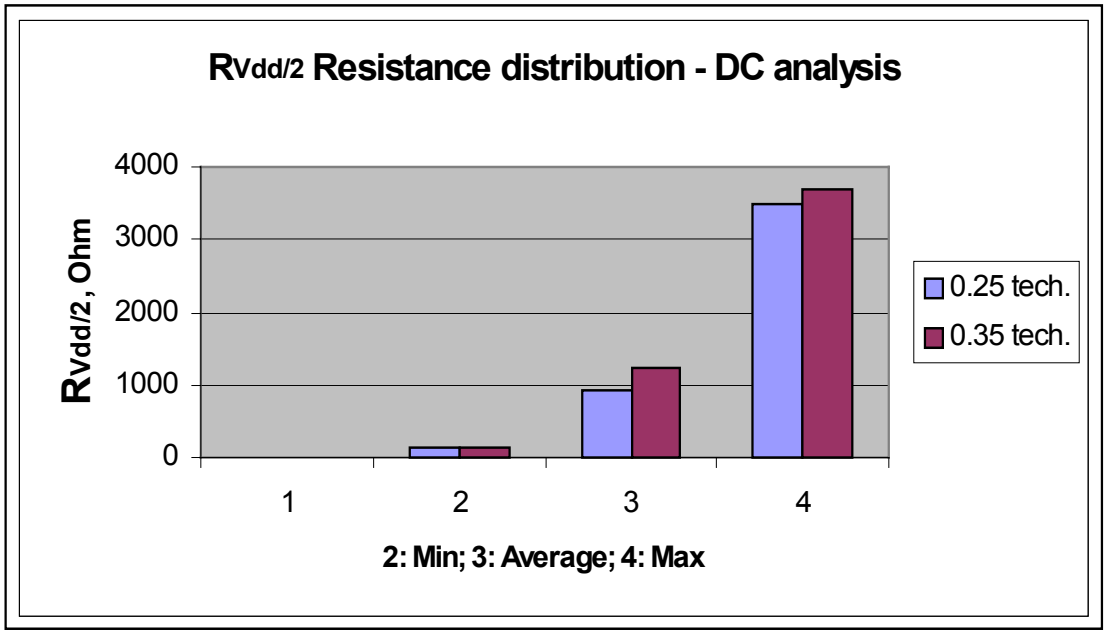
- $R_{vdd/2}$ is defined as the minimum resistance under steady DC inputs conditions below which the circuit always shows a logic malfunction. This is the critical BF resistance under DC conditions.
- R_{crit} is defined as the minimum resistance, which circuit does not operate properly under AC conditions or has 50% increase in propagation delay.

The results of simulations are presented in Figure 3.9.

3.5 Conclusion

In this chapter we have shown that the sensitivity of CMOS IC to BFs is increased with the reduction of feature size of IC, voltage supply and the increase of operating temperature. Because the critical resistance value of BF (the resistance above which the

defect cannot be detected) is reduced in case of DC conditions, as our research shows, the problem of CMOS ICs testing becomes more complicated.



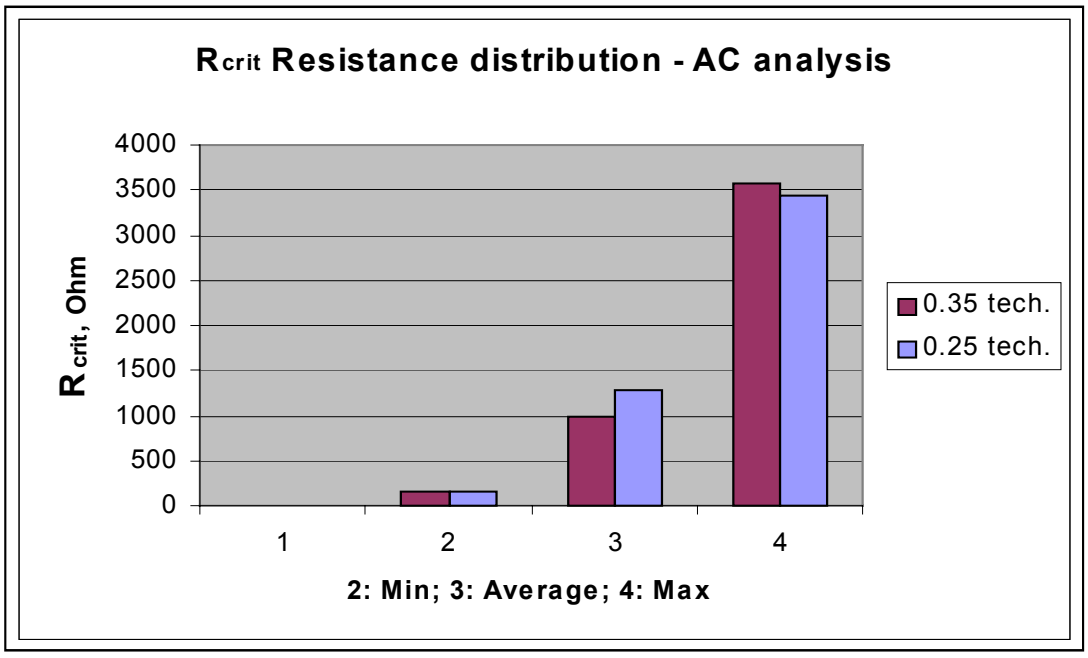


Figure 3.9: *Critical resistance distribution.*

This resistance depends on the maximum frequency that a given test can measure. Many tests run at a base test cycle frequency that is substantially less than the systems clock frequency. The defect impact on normal circuit operation depends on its operating frequency; thus, the critical defect has another resistance (higher) associated with operating frequency. Unfortunately, bridging defects are not 100% detectable by I_{DDQ} or Boolean methods only. In our research we used the DC and AC voltage test method (parametric method), which can successfully supplement the existing test methods of BF in CMOS ICs. The following conclusions were obtained from the analysis of external BF behavior in sequential and combinational CMOS circuits:

1) R_{crit} (AC conditions) values are changed in a wide range from 100 Ohm to almost 4000 Ohm and it is very difficult to predict the value of critical resistance;
2) R_{crit} (AC conditions) and $R_{10\%}$ (DC conditions) are increased as V_{dd} is reduced;
3) R_{crit} (AC conditions) and $R_{10\%}$ (DC conditions) are increased with increase of operating temperature;
4) BF coverage may be increased at low V_{dd} and high temperature during logic testing.

The following conclusions were obtained from the analysis of internal BFs behavior in combinational CMOS circuits:

1) R_{crit} (AC analysis) > $R_{vdd/2}$ (DC analysis), because delay faults precede the total logic failure;
2) $R_{vdd/2}$ (DC analysis) is reduced under technology scaling. It means that the interval of bridging resistor values when circuit does not work properly is reduced and consequently the effectiveness of DC voltage testing is reduced;

3) R_{crit} (AC analysis) increases with technology scaling. Hence, the voltage testing at the maximum operating frequency may increase the BF coverage in combinational CMOS circuits.

The obtained results were presented in [36,37].

Chapter 4: Impact of CMOS Technology Scaling on Bridging Fault (BF) Modeling

4.1 Introduction

BF detection methods can broadly be classified into the current monitoring and logic test methods. The current monitoring method (I_{ddq} method) has been effective in detecting BF in CMOS technologies [38]. However, owing to increased number of transistors and increased sub-threshold leakage with technology scaling make it difficult to detect BFs in deep sub-micron VLSIs with current measurement. Several researchers predicted that defect and defect-free currents for scaled devices will have similar distribution [16,39].

On the other hand, voltage testing is the predominant test methodology. Studies show that low resistive BFs can be detected by logic testing if voltage at a node affected by BF is close to faulty voltage level. Ferguson and Shen [40] extracted and simulated CMOS defects using Inductive Fault Analyses (IFA) techniques. Stuck-at fault (SAF) model performed rather poorly in modeling extracted BF, only 73% - 89% BFs were detected by SA based test patterns. On the other hand the fault coverage of extracted BF by exhaustive test set was relatively high. In another study, Storey and Maly [38] demonstrated similar results. The SAF testing could detect only 80% of the BFs in an 8:1 multiplexer. However, I_{ddq} could detect all the bridging faults.

Resistance of BF plays a significant role in its detection. As the resistance of a BF increases, its detection becomes difficult. Vierhaus et al. [41] investigated the impact of defect resistance on CMOS combinational logic. Their analysis resulted in similar conclusions. For high resistive bridging faults voltage testing was inadequate and delay

fault testing improved coverage. However, authors concluded that zero defect testing is impossible without I_{ddq} testing. Maiuri and Moore [32] extended this work by including impact of technology scaling on BF detection. They analyzed BFs in three different technologies. The results of their analysis show that with the scaling of technology the range of defect resistance for which, defects are not detected, is increasing.

Several researchers investigated test pattern generation techniques for BFs [42,43]. Chess and Larabee [42] described a system for simulating and generating tests for BFs. Their system could detect at least 98.32% of BFs in ISCAS-85 combinational benchmark circuits. In this study authors assume the resistance of BFs to be low. Recently, Lee et. al. [43] further investigated test pattern generation technique for BFs. An automatic test pattern generation (ATPG) algorithm was developed for faults that are logic testable. A built-in intermediate voltage sensor (BIVs) was embedded in chip for BFs that generate intermediate voltages.

Randomly placed bridging faults are a serious problem in CMOS processes. As technology advances to smaller geometry, more metal layers, reduced design margins and higher frequencies, the effects of these defects will grow in complexity, increasing the variety of bridging behavior we need to detect. Hence, the motivation of this research is to assess the impact of technology scaling on bridging fault detection. Theoretical analysis and HSPICE simulations carried out in four different technologies (0.18 μm, 0.25 μm, 0.35 μm, 0.8 μm) show that the detection of BFs is becoming increasingly harder with technology scaling. Fast and accurate calculations of the intermediate bridging voltages on the basis of BF model are presented in this chapter.

4.2 Description of the Analyzed Circuit

Electrical effects of a resistive short located between two CMOS inverters (Figure 4.1) were analyzed. The modeling and simulations of BF was done under DC conditions. Inputs of two inverters are kept at logic levels "0" and "1" respectively.

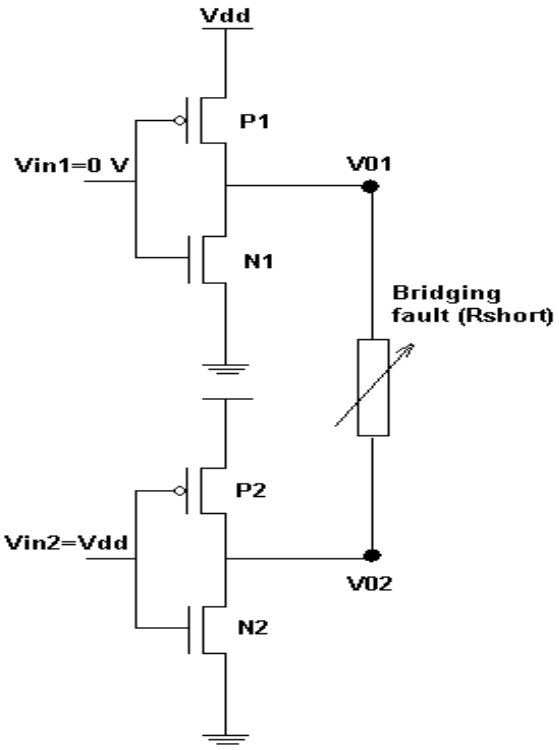


Figure 4.1: *Circuit for bridging fault (BF) modeling.*

The voltages at intermediate nodes are calculated as a function of BF resistances. In this analysis representative values of a given technology parameters are used in simulations. We used four different technologies available for us from Canadian Microelectronic Corporation (CMC) technology files. Transistor parameters for different technologies are listed in Table 4.1. Device parameters for 0.8 μm CMOS technology are used from [43].

Parameter	0.8-µm technology	0.35-µm technology	0.25-µm technology	0.18-µm technology
Vdd, V	5	3.3	2.5	1.8
V_{tn}, V	0.75	0.56	0.42	0.47
$V_{tp,}$ V	-0.9	-0.75	-0.6	-0.44
K_n, ($\mu A/V^2$)	101.05	148.3	212	224
K_p, ($\mu A/V^2$)	32.71	54.5	60	69.4

Table 4.1: *Transistor parameters for different CMOS technologies.*

4.3 Transistor Operating Modes

In Figure 4.1 let us assume that V_{in1} = 0V and V_{in2} = Vdd and BF resistance is significantly large. In this case the transistors N1 and P2 are in cut off mode and we have $I_{p1} \approx I_{n2} \approx I_{Rsh}$, where I_{p1} is the source-drain current of transistor P1 and I_{n2} is the drain-source current of transistor N2. Conversely, if V_{in1} = Vdd and V_{in2} = 0 V, the transistors N2 and P1 are in cut off mode.

Theoretically, P1 and N2 transistors can have four possible operating modes:

- P1 saturation and N2 saturation;
- P1 linear and N2 saturation;
- P1 saturation and N2 linear;
- P1 linear and N2 linear.

For transistor P1 to be in saturation, following condition should hold:

$|V_{01} - Vdd| > |V_{in1} - Vdd| - |V_{tp}|$.

If transistor P1 is in the linear region then $V_{01} > |V_{tp}|$. Similarly, we can describe operating modes for N2. For example, transistor N2 is in saturation mode if $V_{02} - 0 > V_{dd} - V_{tn}$ and it is in linear mode if $V_{02} < V_{dd} - V_{tn}$. The calculated voltage ranges for each operating mode and four different CMOS technologies are shown in Table 4.2. In order to calculate the voltages at V_{01} and V_{02} nodes, we describe the MOSFET DC model. At

0.8 µm CMOS technology, [43]		**0.35 µm CMOS technology**		**0.25 µm CMOS technology**		**0.18 µm CMOS technology**	
P1 (V_{01})	**N2 (V_{02})**	**P1 (V_{01})**	**N2 (V_{02})**	**P1 (V_{01})**	**N2 (V_{02})**	**P1 (V_{01})**	**N2 (V_{02})**
Saturation (< 0.9 V)	Saturation (> 4.25 V)	Saturation (< 0.75 V)	Saturation (> 2.74 V)	Saturation (< 0.6 V)	Saturation (> 2.08 V)	Saturation < 0.44 V	Saturation > 1.33 V
Linear (> 0.9 V)	Saturation (> 4.25 V)	Linear (> 0.75 V)	Saturation (> 2.74 V)	Linear (> 0.6 V)	Saturation (> 2.08 V)	Linear > 0.44 V	Saturation > 1.33 V
Saturation (< 0.9 V)	Linear (< 4.25 V)	Saturation (< 0.75 V)	Linear (< 2.74 V)	Saturation (< 0.6 V)	Linear (< 2.08 V)	Saturation < 0.44 V	Linear < 1.33 V
Linear (> 0.9 V)	Linear (< 4.25 V)	Linear (> 0.75 V)	Linear (< 2.74 V)	Linear (> 0.6 V)	Linear (< 2.08 V)	Linear > 0.44 V	Linear < 1.33 V

Table 4.2: *Transistor operation conditions for different CMOS technologies.*

At this stage we consider the long channel model (the SPICE MOS Level 1 model).

The first order model is based upon following assumptions [44]:

i) Gradual channel approximation is valid.

ii) Hole current can be neglected (for n-MOS).

iii) Recombination and generation are neglected.

iv) Current flows in the ***y*** direction (along the length of the channel) only.

v) Carrier mobility $\boldsymbol{\mu}$ in the inversion layer is constant in the ***y*** direction.

vi) Current flow is due to drift only (diffusion current is neglected).

vii) Bulk charge ***Q*** is constant at any point in the ***y*** direction.

The following equations describe the drain current of the transistor for different operating regions:

1) cut-off region: ($V_{gs} \leq V_{th}$), $I_{ds} = 0$;

2) linear region: ($V_{gs} > V_{th,}$ $V_{gs} \leq V_{dsat}$),

$$I_{ds} = \beta (V_{gs} - V_{th} - 0.5 V_{ds}) V_{ds}; \quad (4.1)$$

3) saturation region: ($V_{gs} > V_{th,}$ $V_{gs} > V_{dsat}$),

$$I_{ds} = \beta/2 (V_{gs} - V_{th})^2 (1 + \lambda V_{ds}), \quad (4.2)$$

where λ is the channel length modulation parameter and β is the gain factor, which is defined as $\beta = K^* (W/L)$ and $K = \mu C_{ox}$ is the process transconductance parameter (see Table 4.1 for values of this parameter for different technologies). Typically, λ values between 0.05 - 0.001 V^{-1} [44]. Table 4.1 has K_n and K_p for different CMOS technologies.

The data in Table 4.2 can be analyzed to simplify the analysis for a given technology. For example certain operating modes are impossible and some other modes are unlikely. The impossible mode is shaded dark while unlikely modes are shaded lightly in Table 4.2.

1) P1 Saturation and N2 Saturation case

This mode requires $V_{01} > V_{02}$ for all technologies. For 0.18-μm technology, $V_{01} < 0.44$ V (V_{tn}) and $V_{02} > 1.33$ V ($V_{dd} - V_{tn}$). This condition contradicts the $V_{01} > V_{02}$ condition hence it is not possible.

2) P1 Linear and N2 Saturation case

Using the condition $I_{p1} \approx I_{n2} \approx I_{Rsh}$ and equations for the drain current of transistor for these operating regions (Eq. 4.1 and Eq. 4.2), we have Eq. 4.3 and Eq. 4.4. Dividing Eq. 3.3 by Eq. 4.4 and by substituting specific parameters in 0.8 μm CMOS technology in [43] Eq. 4.5 and Eq 4.6. In the Eq. 4.6 were obtained, W_{p1} and L_{p1} are channel width and length for P1 transistor; W_{n2} and L_{n2} are channel width and length for N2 transistor.

Transistors size ratio more then 9.99 is seldom used for most logic circuits, hence this condition is very unlikely.

3) P1 Saturation and N2 Linear case

The similar technique may be used for P1 Saturation - N2 Linear transistor modes. From Table 4.2 for 0.8 μm CMOS technology it follows that V_{01}<0.9V and V_{02}<4.25V. Using a similar derivation in the previous case, Eq. 4.7 and Eq. 4.8 were obtained. Typically, the transistors size ratio in CMOS digital circuits lie between 2 and 3 for equal noise margin or balanced rise/fall times.

4) P1 Linear and N2 Linear case

Because $I_{p1} \approx I_{n2} \approx I_{Rsh}$, the voltage drop across the R_{sh} is described by two equations (see Eq. 4.9). Since both equations are nonlinear, the general approach to solving this kind of problem is by iteration, i.e. first guessing a solution and then successively refining it. The method of approximated solution of this case is described in [43] for 0.8-μm technology and we used it for other technologies. Dimensions of transistors, which were used for the BF modeling and simulation in HSPICE, are shown in Table 4.3 and required transistor parameters are shown in Table 4.1.

CMOS technology	**The size of n-MOS transistor, $K_n = (W/L)$**	**The size of p-MOS transistor, $K_p = (W/L)$**	**The ratio coefficient: $K = K_p/K_n$**
0.8 μm [43]	2 μm/1 μm= 2	4 μm/1 μm = 4	2.0
0.35 μm	0.8μm/0.35 μm = 2.29	1.96μm/0.35μm = 5.6	2.44
0.25 μm	0.8 μm/0.25 μm = 3.2	1.64 μm/0.25 μm = 6.56	2.05
0.18 μm	0.58 μm/0.18 μm = 3.2	1.5 μm/0.18 μm = 8.3	2.6

Table 4.3: *Transistor dimensions used for the BF simulation and modeling.*

$$V_{01} - V_{02} = R_{short} \cdot K_p \frac{W_{p1}}{L_{p1}} \left\{ \left(\left| V_{in1} - V_{dd} \right| - \left| V_{tp} \right| \right) \left(\left| V_{01} - V_{dd} \right| \right) - \frac{\left| V_{01} - V_{dd} \right|^2}{2} \right\} \quad (4.3)$$

and

$$V_{01} - V_{02} = R_{short} \cdot \left\{ \frac{K_n}{2} \frac{W_{n2}}{L_{n2}} \left(V_{in2} - V_{tn} \right)^2 \right\} \quad (4.4)$$

$$V_{01} = 0.9 + \sqrt{\frac{16.8 - 55.8 W_{n2}}{L_{n2} \frac{L_{p1}}{W_{p1}}}} > 4.25V \quad (4.5)$$

$$\frac{W_{p1} / L_{p1}}{W_{n2} / L_{n2}} > 9.99 \quad (4.6)$$

$$V_{02} = 4.25 - \sqrt{18.06 - 5.44 \frac{W_{p1}}{L_{p1}} \frac{L_{n2}}{W_{n2}}} < 0.9 \quad (4.7)$$

$$\frac{W_{p1} / L_{p1}}{W_{n2} / L_{n2}} < 1.26 \quad (4.8)$$

$$V_{01} - V_{02} = R_{sh} K_p \frac{W_{p1}}{L_{p1}} \left\{ \left(\left| V_{in1} - V_{dd} \right| - \left| V_{tp} \right| \right) \left(V_{dd} - V_{01} \right) - \frac{\left(V_{dd} - V_{01} \right)^2}{2} \right\} \quad (4.9)$$

and

$$V_{01} - V_{02} = R_{sh} \left\{ K_n \frac{W_{n1}}{L_{n1}} \left[\left(V_{in1} - V_{tn} \right) V_{02} - \frac{V_{02}^2}{2} \right] \right\}$$

For 0.8-µm technology, the following results were obtained in [43]:

$$\begin{cases} V_{01} = [4.51R_{short} + 6133] / [3027 + R_{short}] \\ V_{02} = 3.29 - 0.62\, V_{01} \end{cases} \quad (4.10)$$

Using a similar approach following expressions for 0.35-, 0.25- and 0.18- µm technologies were obtained:

For 0.35-µm technology we have

$$\begin{cases} V_{01} = [3.24\, R_{short} + 5000] / [3761 + R_{short}] \\ V_{02} = 2.15 - 0.63\, V_{01} \end{cases} \quad (4.11)$$

For 0.25-µm technology we have

$$\begin{cases} V_{01} = [2.24\, R_{short} + 604.7] / [720.7 + R_{short}] \\ V_{02} = 1.2 - 0.43\, V_{01} \end{cases} \quad (4.12)$$

For 0.18-µm technology we have

$$\begin{cases} V_{01} = [1.57\, R_{short} + 675] / [955.3 + R_{short}] \\ V_{02} = 1.09 - 0.54\, V_{01} \end{cases} \quad (4.13)$$

These equations were used to calculate bridging intermediate voltages V_{01} and V_{02} for a BF between two inverters.

HSPICE simulations of analyzed circuit (Figure 4.2) for 0.35 µm, 0.25 µm and 0.18 µm CMOS technologies show that P1 and N2 transistors are operating in Linear - Linear modes in a wide configuration interval (Eq. 4.14), which cover all real MOSFET

applications in digital circuits. R_{short} was set to 100 KΩ under circuit simulations for defect free case emulation.

$$1 \leq \frac{W_{p1} / L_{p1}}{W_{n2} / L_{n2}} \leq 10 \tag{4.14}$$

4.4 Correlation between Technology Parameters and Bridging Fault (BF) Behavior in CMOS Circuits

As the technology scales, several short channel effects influence the drain current. In our long channel model following four parameters are affected by the technology scaling. These parameters are listed as follows:

i) Carrier mobility μ in the channel

ii) Gate oxide capacitance

iii) Supply voltage

iv) Threshold voltage

Figure 4.2 illustrates the effective electron mobility μ as a function of channel length [45]. As it is apparent from the graph, the mobility degrades with reduced channel length. The process trans-conductance parameter (K) is suitably modified to include this effect (see Table 4.1). Similarly, the impact of change of gate oxide capacitance on K is also included in the model. Figure 4.3 shows the C_{gate}/C_{ox} ratio as a function of oxide thickness [45]. Here C_{gate} is the total transistor gate capacitance per unit area while C_{ox} is transistor thin oxide capacitance per unit area. In this analysis, constant electric field scaling is utilized for scaling of sub-micron devices. Therefore, power supply voltage, V_{dd}, is also scaled with technology. The reduced V_{dd} voltage results in lower power dissipation as well as enhanced reliability. The transistor threshold voltage is also

reduced proportionally in order to maintain high switching speed. Table 4.1 illustrates these parameters for different CMOS technologies.

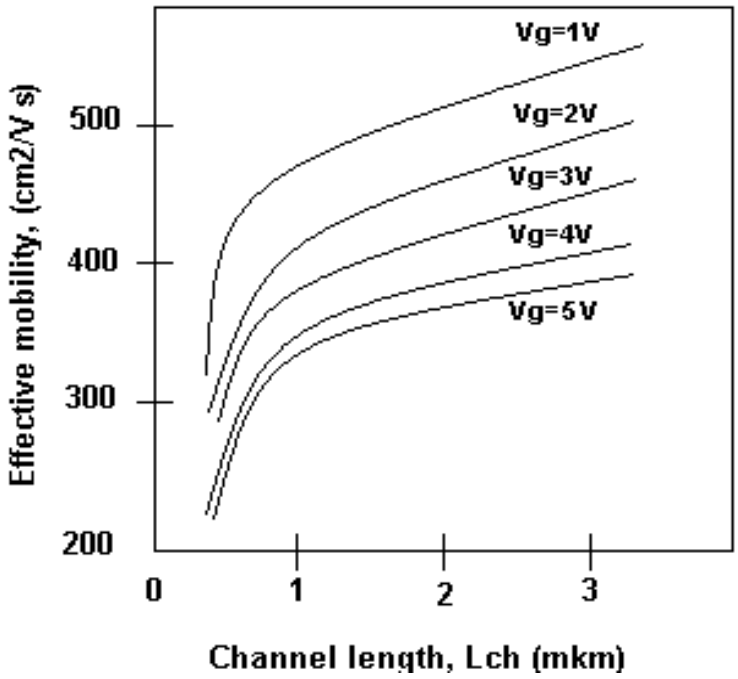


Figure 4.2: *Experimental variation of μ_n as a function of channel length, for different gate voltages [47]*.

In accordance with equations for V_{01} and V_{02} (section 4.3) for different CMOS technologies, voltages at nodes V_{01} and V_{02} were plotted for various values of bridging resistance R_{sh}. These results were compared with the simulated results in HSPICE. Figure 4.4 (a) and (b) illustrate the comparison of calculated as well as HSPICE simulated results. The average discrepancy between simulated results and that of the model was found to be 16%.

In our investigation we assumed that the critical value of BF resistance (R_{crit}) corresponds to R_{sh} that result in degradation of nominal logic levels by ($V_{tn} + |V_{tp}|$), (i.e. approximately 40% of Vdd for different technologies).

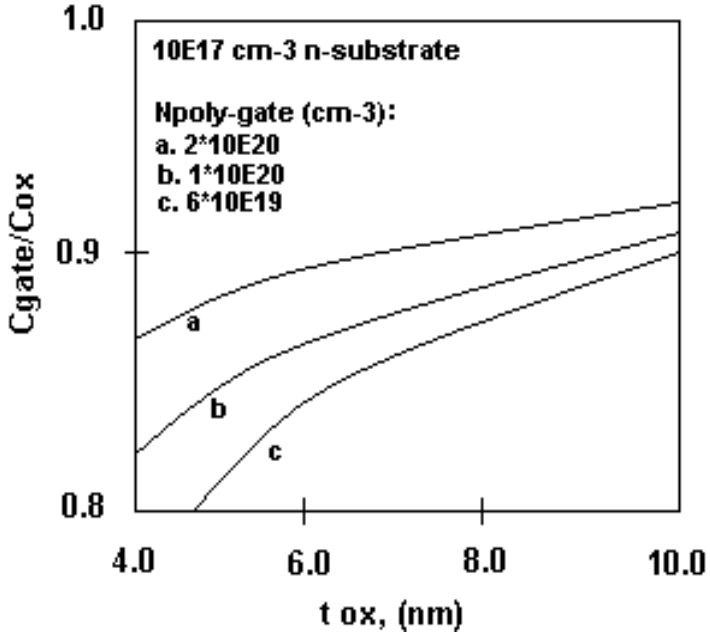


Figure 4.3: *Gate capacitance to oxide capacitance, as a function of oxide thickness and n^+ - polysilicon gate doping concentration [48].*

(a) (b)

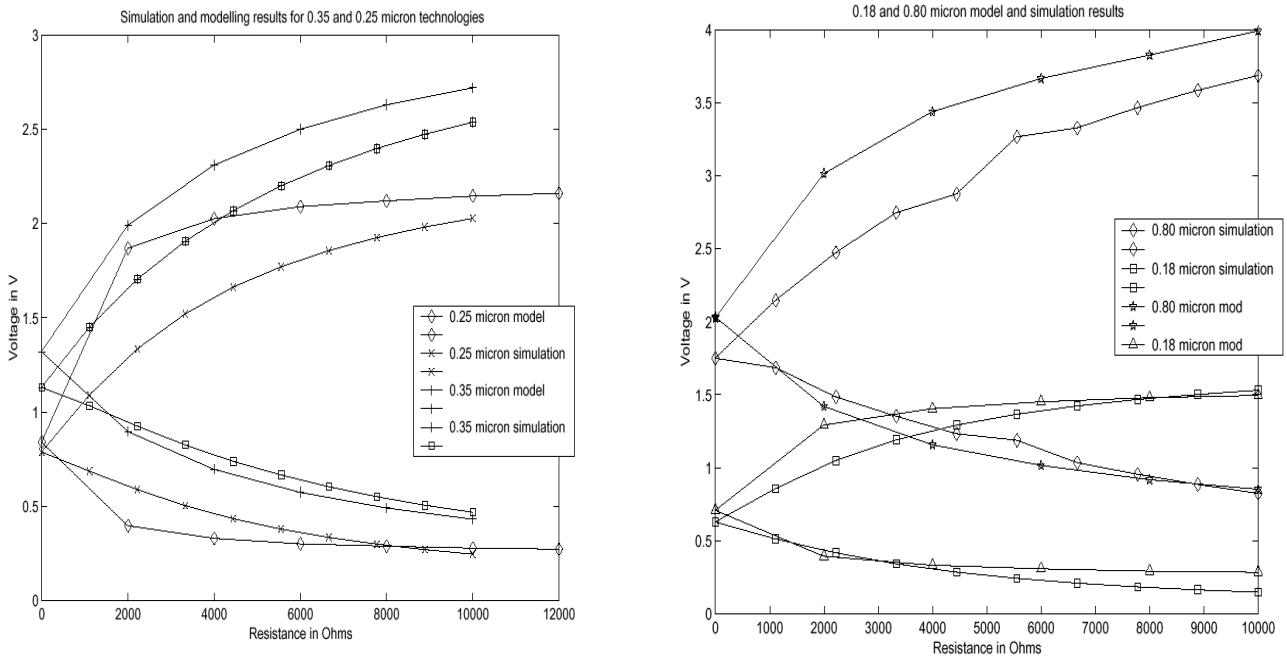


Figure 4.4: *Output voltage levels (V_{01} and V_{02}) vs. bridging resistance (the applied model and HSPICE simulations): (a) - 0.25- and 0.35 - μm technology; (b) - 0.8- and 0.18- μm technology.*

This ensures that transistors operate in linear mode (the proposed BF model is valid), and degraded logic levels are located close to the middle of the "linear - linear" interval. It has been shown that the threshold voltage of different logic gates (INV and 1 to 6 input NAND, NOR, XOR, XNOR) is located in interval [V_{dd} - 40%; 0 V + 40%] [43]. Other criterion, which we used in our investigation for interpretation of BF impact on logic levels, is $R_{10\%}$ value. When BF value corresponds to $R_{10\%}$, the nominal logic levels are degraded by 10%. Typically, the degradation of logic levels less then 10% is not identified as the logic error. The dependence of critical resistance (R_{crit}) value on analyzed technologies is plotted in Figure 4.5. It can be inferred that R_{crit} reduces under technology scaling.

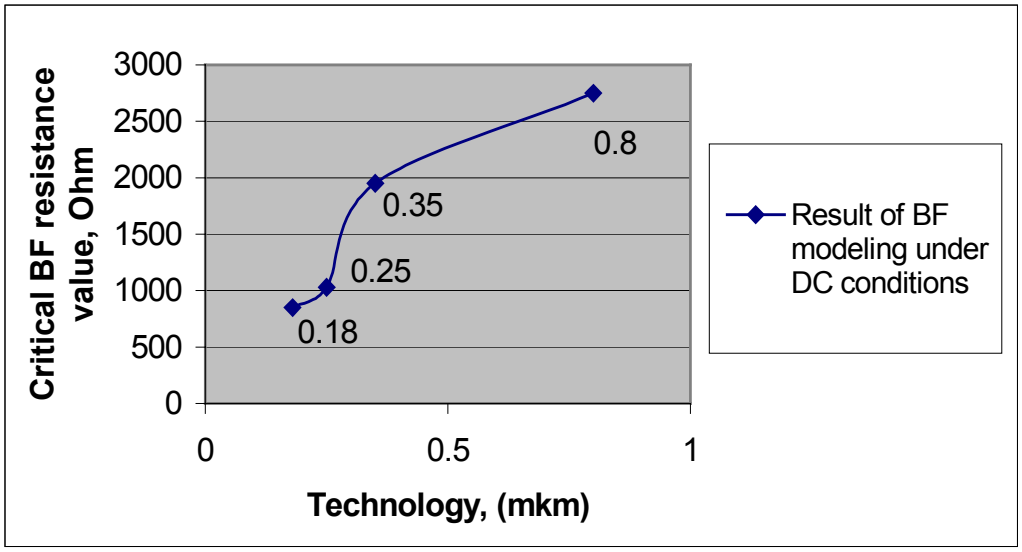


Figure 4.5: *Critical BF resistance vs. CMOS Technologies.*

The data from Figure 4.4 (a) and (b) are normalized in order to see the impact of technology scaling on voltages of node V_{01} and V_{02}. These, normalized node voltages are plotted as a function of BF resistance and are illustrated in Figure 4.6. Normalized plots were obtained for each technology for both V_{01} and V_{02} curves in the following manner.

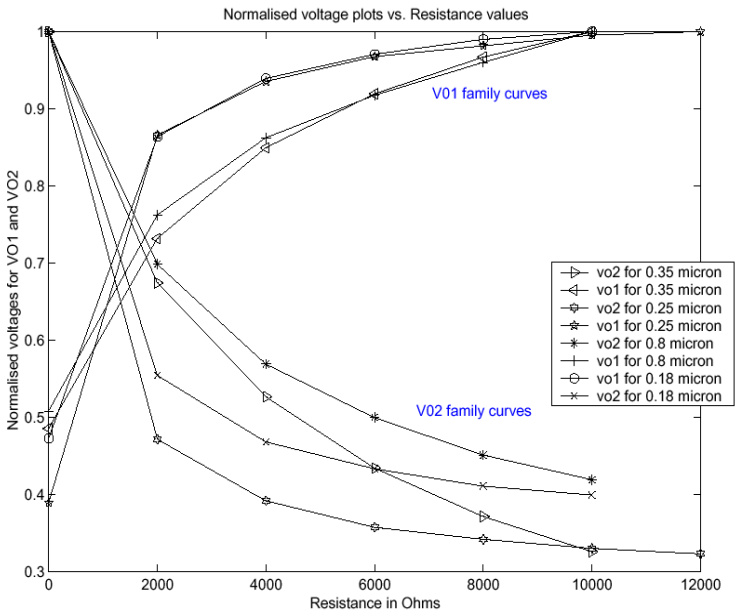


Figure 4.6: *Normalized voltages vs. BF resistance (V_{01} and V_{02} voltages for different technologies).*

For V_{01}, the data points were divided by the V_{dd} of the corresponding technology, while for V_{02}, each point was divided by the voltage when R_{sh} is 0 Ohms. Thus the normalized plots for V_{02} for different technologies converge at 1 when R_{sh} is 0 Ohms. This plot allows comparison of the results obtained for different technologies and illustrates the general trends of V_{01} and V_{02} variation with bridging fault resistance. Following conclusions can be drawn from Figure 4.6 using the analytical model:

1) For bridging resistances less than R_{crit}

(<~850 Ohms for 0.18 - µm technology; <~1030 Ohms for 0.25 - µm technology; <~1950 Ohms for 0.35 - µm technology; <~2750 Ohms for 0.8 - µm technology) BF may be detected by voltage testing methods, because the nominal voltage levels are significantly degraded and result into erroneous logic condition.

2) When the bridging resistance is between R_{crit} and $R_{10\%}$ (when the nominal logic levels are degraded by 10%), the BF cannot be detected by voltage testing method (voltage levels are in undefined range):

~ 850 Ohms ≤ R_{BF} ≤ ~ 3000 Ohms for 0.18 - μm technology;

~ 1030 Ohms ≤ R_{BF} ≤ ~ 3000 Ohms for 0.25 - μm technology;

~ 1950 Ohms ≤ R_{BF} ≤ ~ 5500 Ohms for 0.35 - μm technology;

~ 2750 Ohms ≤ R_{BF} ≤ ~ 5500 Ohms for 0.8 - μm technology.

3) For bridging resistance values grater then $R_{10\%}$ (~ 3000 Ohms for 0.18 - and 0.25 - μm technologies; ~ 5500 Ohms for 0.35 - and 0.8 - μm technologies), the output logic levels are not distorted, but the noise immunity is degraded near the mentioned resistance values.

Note that the interval of BF resistance values, which can be tested by voltage test method, is reduced under technology scaling.

4.5 Modeling of BF Including Short Channel Effects of MOSFET Transistors

The accuracy of the long channel model, which we used in Section 4.4 is far from satisfactory by today's standards. However, because of its simplicity, it is very useful model for performing basic circuit analysis and developing design equations for circuit performance. In this section we shall try to improve the accuracy of BF modeling using a simple short channel model for of 0.18 - μm technology.

The following effects are necessarily considered at the modeling of DC characteristics of small-geometry MOSFETs [44]:

- surface mobility reduction due to the vertical and lateral electric field in the channel;

- carrier velocity saturation;
- channel length modulation;
- depletion charge sharing by the source/drain;
- source/drain series resistance;
- hot-carrier effect.

This is the "Regional Approach", which was used in circuit simulator SPICE Level 3. The linear region drain current is expressed as [44]

$$I_{ds} = \frac{W\mu_s C_{ox}}{L_{eff}\left(1 + \frac{\mu_s V_{ds}}{L_{eff} v_{sat}}\right)}\left(V_{ds} - V_{th} - \alpha V_{ds}\right)V_{ds} \tag{4.15}$$

where α is the short-channel parameter (which includes short-channel effects, such as nonlinear velocity-field characteristics and modification of the bulk charge due to the presence of the mobile carriers), v_{sat} is the saturated carrier velocity, L_{eff} is the effective channel length, μ_s is the surface mobility.

At low fields, the carrier velocity in the channel is proportional to the source-drain electric field. At around 10^4 V/cm the carrier velocity increases with less proportionality to the field and when a field of 10^5 V/cm is applied, the carriers are deep in saturation and velocity (and hence current) is essentially independent of the field. 10^5 V/cm corresponds to $V_{ds} = 1$ V and $V_g = 2$ V for a 100 μm × 20 μm (W × L) n-channel MOSFET. It was reported, that measured value of saturated carrier velocity is 4×10^6 cm/s for channel electrons in Si MOSFETs [49]. From the experimental data for short-channel transistors, ($L \leq 0.3$ μm) it was found that the short-channel parameter α lies in the range $0.5 < \alpha < 0.85$ [50].

The Linear (P1) & Linear (N2) case for 0.18 - μm technology (see section 4.3) is considered again. We substitute long channel model for drain current (4.1) on short-channel model (Eq. 4.15) in equations (4.9) for voltage drop across the R_{sh}. Take into consideration the meaning of α and v_{sat} and solve the combined equations (4.9) we obtain

$$\begin{cases} V_{01} = [1.75\, R_{short} + 959.4] / [1522.9 + R_{short}] \\ V_{02} = 0.91 - 0.45\, V_{01} \end{cases} \qquad (4.16)$$

Figure 4.7 shows the dependency of logic levels V_{01} and V_{02} on R_{sh} for long channel and short-channel models. For comparison, we plotted the HSPICE simulation results for 0.18 - μm technology in the same graph. The difference between the short-channel model and HSPICE simulation is 9%. This is significantly better than the accuracy of the long channel model. Obviously, more accurate results may be obtained by using more accurate short-channel transistor models, for example "Hybrid Approach" described in [51], but in this case computerized calculations will be need.

4.6 BF Modeling in Complicated CMOS Logic Gates

Some distortion of the BF model may occur when dealing with transistors in series connection, because the body effect exists on any transistor whose source node is not connected to the V_{dd} or GND node. In case of complicated CMOS gates, the basic idea of BF modeling consists of finding a single transistor equivalent for the serial or parallel network. Indeed, using the equivalent transistor concept, any bridge with a serial or parallel network can be studied as a bridge between two single transistors. This concept is illustrated in figure 4.8.

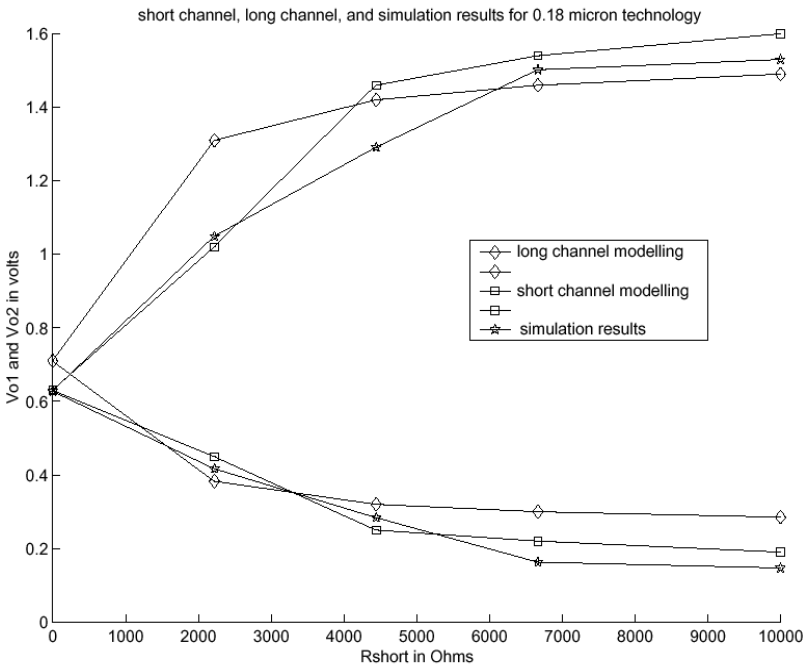


Figure 4.7: *Output voltage levels (V_{01} and V_{02}) vs. bridging resistance: long channel, short-channel models and HSPICE simulations for 0.18- μm technology.*

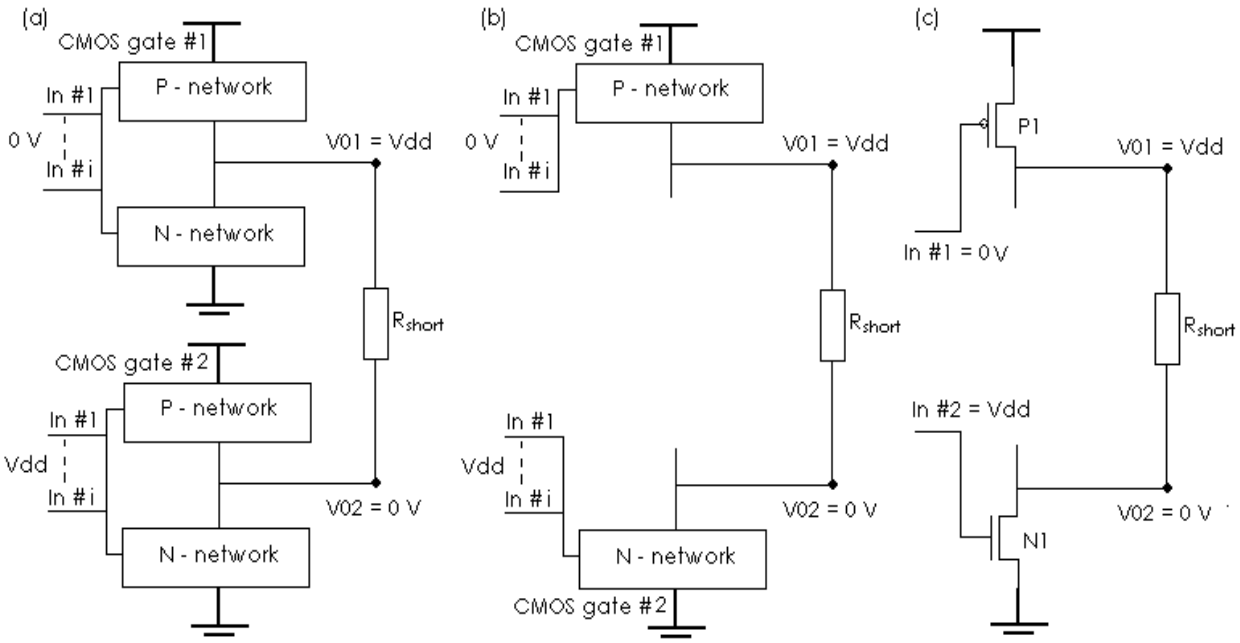


Figure 4.8: *A BF between two CMOS gates: (a) the original circuit; (b) the equivalent circuit under DC condition; (c) the equivalent transistor circuit for P - and N - networks.*

The case of a parallel network is obvious. The configuration of the equivalent single transistor is equal to the sum of the configurations of the different transistors in the network and may be described by:

$$k_p = \sum_{i=1}^{k} k_p(i) \qquad k_n = \sum_{i=1}^{k} k_n(i) \tag{4.17}$$

Where k is the number of transistors in a parallel network and $k_n = (W/L)_n$ and $k_p = (W/L)_p$ are the configuration of transistors.

The case of a serial network is much more complicated. Because of non-linearity, the configuration of the equivalent single transistor is not equal to the harmonic sum of the configurations of the different transistors in the network. M. Renovell et.al. [52] proposed the model for the distortion factor, which describes the effect of correction of serial transistors in the single equivalent transistor:

$$C_{or} = \left[1 - \gamma_n \frac{\sqrt{\theta_n + V_{dd}(k-1)/4k} - \sqrt{\theta_n}}{\frac{3V_{dd}}{4} - V_{tn}} \right] \tag{4.18}$$

where k is the number of transistors are connected in a serial network, γ_n is the transistor body-effect coefficient, θ_n is the surface potential, V_{tn} is the threshold voltage of transistors in a serial N - network. In this model the following parameters depend on technology scaling: V_{dd}, V_{tn}, γ_n and θ_n (because, the doping concentration in the channel region is changed under technology scaling). However, in a first order approximation we can assume that $\theta_n = 0.73$ as was shown in [52] for 0.5 μm CMOS technology. Values of these technology parameters are given in Table 4.4. These data adopted from Taiwan Semiconductor Microelectronic Corporation (TSMC).

Technology parameter	**0.8 µm technology**	**0.35µm technology**	**0.25 µm technology**	**0.18 µm technology**
V_{dd}, V	5	3.3	2.5	1.8
V_{tn}, V	0.7	0.56	0.42	0.47
γ_n, $V^{1/2}$	0.65	0.62	0.54	0.49

Table 4.4: *Transistor parameters for different technologies.*

Note that the threshold voltage of n-MOSFET in 0.25-µm CMOS technology is less than the same parameter in 0.18-µm CMOS technology. This is because, 0.25-µm CMOS technology was developed by TSMC for analog and RF applications.

It was demonstrated in [52], that in case of a serial network of n - channel transistors, the equivalent configuration is given by:

$$k_{eq} = \frac{1}{\sum_{i=1}^{k} \frac{1}{k_n}(i)} * C_{or} \tag{4.19}$$

The same formula may be used for p - channel transistors, which are connected in a serial network. In this case the k_n parameter (W/L of transistor channel) should be substituted for k_p. The equivalent transistor has the different threshold voltage than transistors in a serial N-network. The effective threshold voltage of equivalent transistor may be calculated approximately by [52]:

$$V_{tneq} = V_{tn} + \gamma_n\left(\sqrt{\theta_n + V_{dd}(k-1)/4k} - \sqrt{\theta_n}\right) \tag{4.20}$$

where V_{tn} is the threshold voltage of transistors in a serial N-network.

The calculated distortion factor values and effective threshold voltages for different CMOS technologies are given in Table 4.5 and Table 4.6 respectively.

# of n - channel transistors in the serial network	0.8 - µm CMOS technology	0.35 - µm CMOS technology	0.25 - µm CMOS technology	0.18 - µm CMOS technology
2	0.94	0.87	0.94	0.93
3	0.92	0.91	0.92	0.91
4	0.91	0.85	0.91	0.90

Table 4.5: *Distortion factor values (C_{or}) vs. CMOS technology.*

# of n - channel transistors in the serial network	0.8 - µm CMOS technology	0.35 - µm CMOS technology	0.25 - µm CMOS technology	0.18 - µm CMOS technology
2	0.9	0.7	0.5	0.53
3	0.96	0.73	0.54	0.55
4	0.99	0.75	0.55	0.56

Table 4.6: *Effective threshold voltage ($V_{t\,eq}$, V) vs. CMOS technology.*

The dependency of effective threshold voltage of equivalent n - channel transistor on the technology scaling for 4 inputs NAND gate is shown in Figure 4.9. The relative variation of threshold voltage (V_{tn}/V_{tneq}) for analyzed technology is almost constant (~ 0.74).

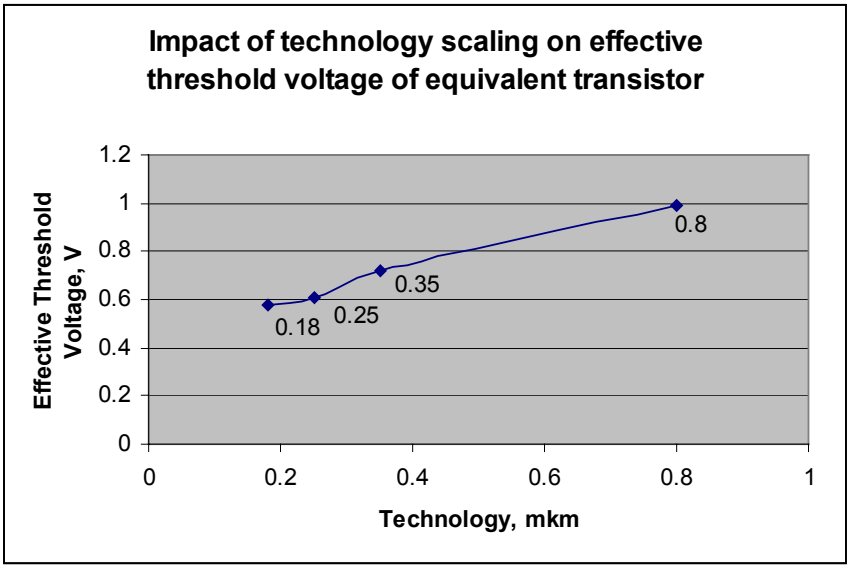


Figure 4.9: *The dependence of effective threshold voltage of equivalent transistor on technology scaling (4 inputs - NAND).*

In section 4.3 we have shown that the linear - linear operating mode is more probable operating mode for CMOS inverter. The following equations may be used for linear - linear operating mode (see Figure 4.1):

$$I_{ds(p)} = K_p \cdot k_p \left(\left(V_{dd} - |V_{tp}|\right)\left(V_{dd} - V_{br}\right) - \frac{\left(V_{dd} - V_{br}\right)^2}{2} \right) \tag{4.21}$$

$$I_{ds(n)} = K_n \cdot k_p \left(\left(V_{dd} - V_{tn}\right)V_{br} - \frac{V_{br}^{\,2}}{2} \right) \tag{4.22}$$

$$I_{ds(p)} \approx I_{ds(n)} \tag{4.23}$$

Where $I_{ds(p)}$ and $I_{ds(n)}$ are drain-to-source currents of p- channel and n- channel transistors respectively, K_p and K_n are process transconductance parameter, k_p and k_n are the configuration of transistors in inverter, V_{tn} and V_{tp} are the threshold voltage of transistors and $V_{br} = |V_{01} - V_{02}|$ is the voltage at bridging fault resistor.

Equations 4.21, 4.22 and 4.23 may be used also for I_{ds} current calculation of equivalent transistors in equivalent circuit of two complicated CMOS gates (Figure 4.8(c)). In this case the configuration of equivalent transistor (k_{neq} and k_{peq}) should be calculated using equation (4.17) for parallel network and equation (4.19) for serial network. The threshold voltage of equivalent transistor of serial network should be calculated using equation (4.20). The results of these calculations for number of transistors in a serial and parallel networks from 2 to 4 are given in Tables 4.7, 4.8, 4.9, and 4.10. We considered p- and n-transistors in a serial and parallel networks; transistor parameters for different technologies were adopted from Table. 4.1; surface potential (θ_n, θ_p) and transistor body-effect coefficients (γ_n, γ_p) for n- channel and p- channel transistors are assumed equal.

# of n - channel transistors in the serial network	0.8 - µm CMOS technology	0.35 - µm CMOS technology	0.25 - µm CMOS technology	0.18 - µm CMOS technology
2	0.94	1.0	1.5	1.49
3	0.61	0.69	0.98	0.97
4	0.46	0.49	0.73	0.72

Table 4.7: *The configuration ($k_{n\ eff}$) of the equivalent single transistor of* ***n - channel transistors in the serial network.***

# of p - channel transistors in the serial network	0.8 - µm CMOS technology	0.35 - µm CMOS technology	0.25 - µm CMOS technology	0.18 - µm CMOS technology
2	1.88	2.4	3.08	3.9
3	1.23	1.7	2.01	2.52
4	0.91	1.19	1.49	1.86

Table 4.8: *The configuration ($k_{p\ eff}$) of the equivalent single transistor of* ***p - channel transistors in the serial network.***

# of n - channel transistors in the parallel network	0.8 - µm CMOS technology	0.35 - µm CMOS technology	0.25 - µm CMOS technology	0.18 - µm CMOS technology
2	4	4.58	6.4	6.4
3	6	6.87	9.6	9.6
4	8	9.16	12.8	12.8

Table 4.9: *The configuration ($k_{n\ eff}$) of the equivalent single transistor of* ***n - channel transistors in the parallel network.***

# of p - channel transistors in the parallel network	0.8 - µm CMOS technology	0.35 - µm CMOS technology	0.25 - µm CMOS technology	0.18 - µm CMOS technology
2	8	11.2	13.12	16.6
3	12	16.8	19.68	24.9
4	16	22.4	26.24	33.2

Table 4.10: *The configuration ($k_{p\ eff}$) of the equivalent single transistor of* ***p - channel transistors in the parallel network.***

The simulation and modeling results of BF between two 2-4 inputs NAND gates have shown in Figure 4.10. These results were obtained for fixed R_{sh}=4 KOhms. Drain-to-source current across BF resistor was calculated using equation (4.22). The intermediate

voltage (V_{br}) at V_{01} and V_{02} nodes (see Figure 4.8 (c)) was found from HSPICE simulations of analyzed circuit in Cadence.

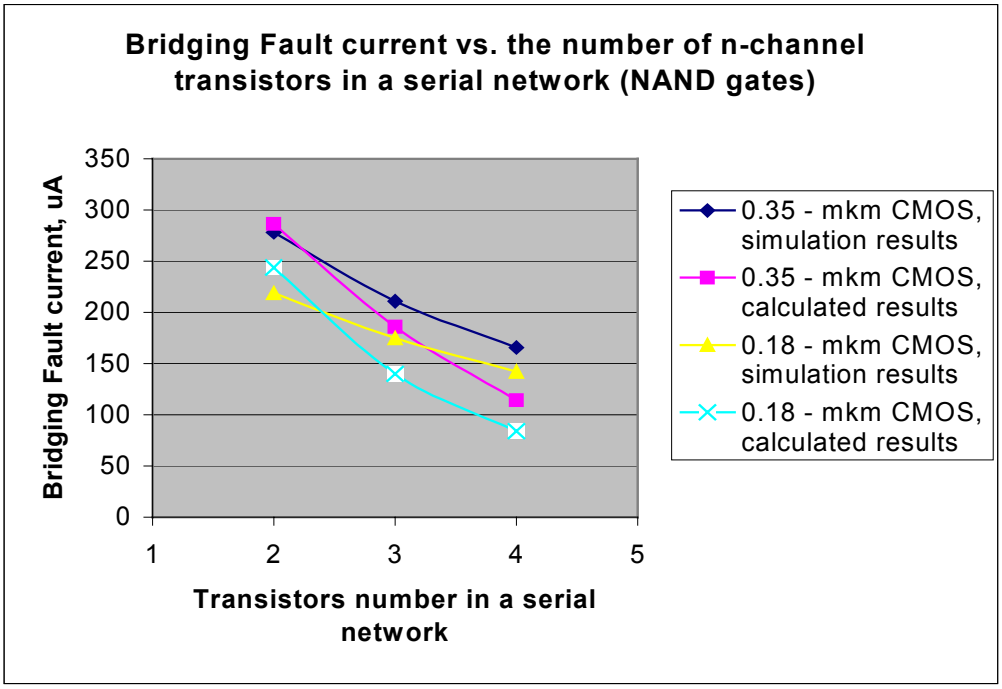


Figure 4.10: *Bridging Fault current vs. the number of n-channel transistors in a serial network (NAND-to-NAND short gates).*

The average error of BF current modeling of 2-4 inputs NAND gates was ~19% for 0.35 - µm and 0.18 - µm CMOS. Note that the equation (4.18) for distortion factor calculation was obtained for long channel 0.5 -µm CMOS technology [52]. The comparative analysis of simulation and modeling results for short channel CMOS technologies allowed to modify the distortion factor:

$$C_{or\ (short\text{-}channel)} = 1.25 \cdot C_{or} \qquad (4.24)$$

It means that the data in Table 4.7 and 4.8 should be increased by 1.25 times. The BF modeling error was reduced by 9%.

As the example of BF model of complicated CMOS gates, we considered the bridging short between 2 inputs NOR and 2 inputs NAND gates. The analyzed circuit and its equivalent circuit are shown in figure 4.11.

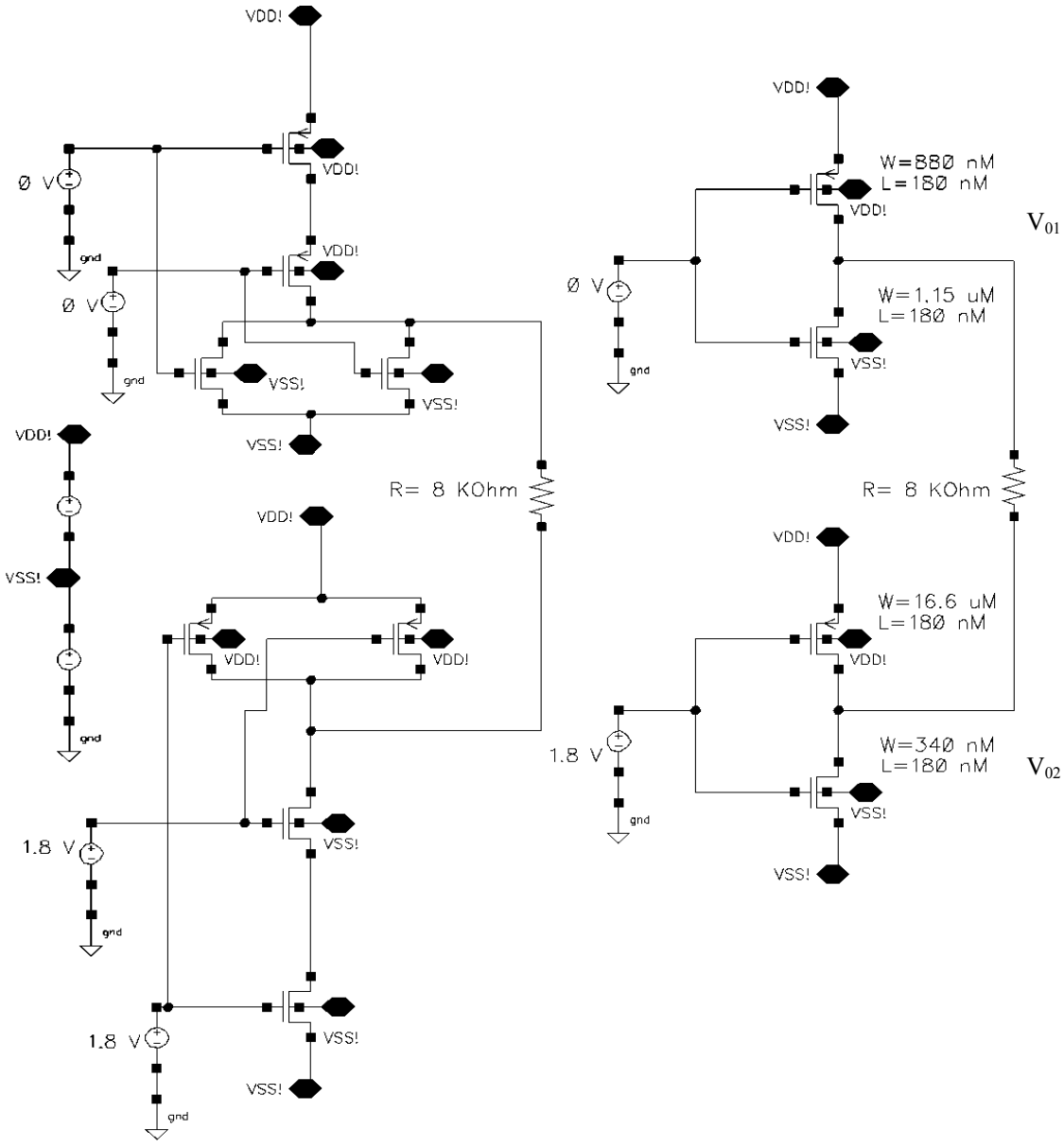


Figure 4.11: *2-NOR-2-NAND short - circuit (a) and its equivalent circuit (b).*

The transistor sizes of original circuit for 0.18-μm CMOS technology are given in Table 4.3 and the calculated transistor sizes of equivalent circuit are presented in Figure 4.11 (b). The results of BF simulation and modeling are given in Table 4.11. All simulations were done for R_{short} = 8 KOhm.

Analyzed circuit	**V_{01}, V**	**V_{02}, V**	**V_{Rshort}, V**	**I_{Rshort}, μA**
2-NOR-2-NAND	1.26	0.27	0.99	123.0
Equivalent circuit	1.29	0.24	1.05	131.4

Table 4.11: *The simulation results of 2-NOR-2NAND short - circuit and equivalent circuit.*

The error in I_{Rshort} value of equivalent circuit in comparison with the original circuit was 7%. In this example the difference of threshold voltage of equivalent serial network transistors and the nominal threshold voltage for 0.18 -μm CMOS technology is modeled by applying of appropriate body-bias voltage to bulk pin of equivalent transistors.

4.7 Conclusion

As CMOS technologies scale down, background leakage increases significantly, primarily due to device subthreshold leakage. As a result, even for 0.25 - μm technology, conventional pass/fail I_{ddq} testing may no longer be practical [53]. Thus for advanced CMOS technologies we should combine current and logic test methods for the best coverage and identification of defects. From this point of view, the voltage modeling of BFs for deep submicron technologies may predict the perspectives of logic testing in the future. In this chapter we have analyzed the impact of CMOS scaling on BF modeling and arrived at the following conclusion:

1) Under technology scaling BF models should include short-channel effects of MOSFETs. The range of intermediate voltages, which can be interpreted as a 0 by one gate and as a 1 by another, will be increased;

2) The developed BF model shows that R_{crit} value is reduced with technology scaling. In chapter 3 the same conclusion was obtained from simulations of sequential and combinational CMOS circuits at DC conditions;

3) The undefined range of R_{BF}, in which BF cannot be detected by voltage testing is increased under technology scaling. Possibly, "Test Mix" technique, combining I_{ddq} and voltage test methods, allow to increase the coverage of detected BFs in submicron CMOS technologies;

4) The error of applied BF model on the basis on long channel MOSFETs model was 16% in comparison with HSPICE simulations. Using short-channel MOSFETs model allows reduction of error in BF model to 9%;

5) The BF model in complicated CMOS gates was modified for submicron CMOS technologies. This model is based on the concept of *Equivalent Transistor*. The error of modified model for 0.18 - μm CMOS technology was ~7 - 9% in comparison with HSPICE simulations.

These results were presented in [54].

Chapter 5: Conclusion

The microelectronics industry is approaching physical, material, and economics limits as aggressive scaling continues. This will require unprecedented changes, resulting in an essential reliability and testing challenge. From a reliability perspective, the most essential change will be the introduction of new materials. Historically, the industry has been conservative in adopting new materials. Furthermore, these materials were extensively characterized prior to insertion into high-volume manufacturing. Today, the industry is forced to introduce multiple new materials. For example, copper is replacing aluminum interconnect, lower dielectric constant inter-level insulators are replacing SiO_2. The reliability of these new materials is not well characterized. The progress in CMOS technology is combined with increased design speed, increased circuit densities, reduced time-to-market period and increased leakage currents. Thus there is a lot of risk that new failure modes will be discovered, requiring new reliability solutions and novel fault-detection techniques.

In this thesis we investigated the bridging faults (BF) behavior in deep submicron CMOS technologies and analyzed the impact of technology scaling on BF detection. The resistive shorts are the prevalent kind of defects in advanced CMOS circuits. It was shown in chapter 2 that the current test methods may lose the effectiveness of defect detection because of the high background defect-free leakage current in deep submicron technologies (≤0.18 μm feature size). Hence, voltage testing will play the crucial role in BF detection. In chapter 3 we analyzed the BF detection in sequential and combinational CMOS circuits for different operating conditions and CMOS technologies. Using the developed BF model we calculated the critical resistance values in chapter 4, which

confirmed the simulation results obtained in chapter 3. The main results of our research presented in this thesis are as follows:

1) BF critical resistance (R_{crit}) values are changed in a wide range from 100 Ohm to almost 4000 Ohms and it is very difficult to predict the value of critical resistance;
2) R_{crit} is increased with increasing of operating temperature and reducing of operating voltage (V_{dd}). Hence, BF coverage may be increased at low V_{dd} and high temperature during logic testing;
3) R_{crit} ($R_{Vdd/2}$ used in chapter 3) is reduced under technology scaling in case of DC operating conditions. It means that the interval of bridging resistor values when circuit does not work properly is reduced and consequently the effectiveness of DC voltage testing is reduced. However, the R_{crit} increases with technology scaling in case of AC operating conditions and the voltage testing at the maximum operating frequency may increase the BF coverage in digital CMOS circuits;
4) The developed BF model shows that R_{crit} value is reduced with technology scaling at DC operating conditions. Hence, this model may explain the simulation results obtained in Cadence. The error of BF model on the basis on long-channel MOSFET model was 16% in comparison with HSPICE simulations. Using short-channel MOSFET model allows reduction of error in BF model to 9%;
5) The BF model in complicated CMOS gates was modified for submicron CMOS technologies. This model is based on the concept of *Equivalent Transistor*. The error of modified model for 0.18 - μm CMOS technology was ~7 - 9% in comparison with HSPICE simulations.

In future, we are going to develop the BF model, which can describe the resistive short behavior in submicron CMOS circuits under AC conditions, because the reason of R_{crit} increase under AC conditions, when transistor sizes are reduced in result of technology scaling, is not completely clear.

References

[1] S. Thompson et al., "MOS scaling: transistor challenges for the 21th century", Intel Technology Journal, Q3, p.1, 1998

[2] M. Bohr, "Silicon trends and limits for advanced microprocessors", Communications of the ACM, vol. 41, No. 3, p. 80, 1998

[3] B. Yu et al., "Limit of gate oxide scaling in nano-transistors", Symposium on VLSI Technology, p. 90, 2000

[4] R. Singh and R.K. Ulrich, "High and low dielectrics constant materials", The Electrochemical Society Interface, vol. 8, No. 2, p. 26, 1999

[5] A. Hokazono et al., "Source/Drain engineering for sub-100 nm CMOS using selective epitaxial growth technique", IEDM, p. 10.6.1, 2000

[6] J.B. Jacobs and D. Antoniadis, "Channel profile engineering for MOSFET's with 100 nm channel lengths, IEEE Trans. on Electron Devices, vol. 42, No. 5, p. 870, 1995

[7] T. Kikkawa, "VLSI interconnect process integration", 5th International Conference on Solid-State and Integrated Circuit Technology, p. 40, 1998

[8] M.T. Bohr, "Interconnect scaling - the real limiter to high performance ULSI", Solid State Technology, No. 9, p. 105, 1996

[9] T. Takewaki et al., "A novel self-aligned surface-silicide passivation technology for reliability enhancement in copper interconnects", Symposium on VLSI Technology, p. 31, 1995

[10] C.F. Hawkins and J. Segure, "Test and reliability: Partners in IC manufacturing, Part 1", IEEE Design & Test of Computers, p. 64, July - September 1999

[11] C. Ryu et al., "Microstructure and reliability of copper interconnects", IEEE Trans. on Electron Devices, vol. 46, No. 6, p. 1113, 1999

[12] J.R. Black, "Mass transport of aluminum by momentum exchange with conducting electrons", International Reliability Physics Symp., p. 148, 1967

[13] C.F. Hawkins et al., "Defect classes - an overdue paradigm for CMOS IC testing", ITC, p. 413, 1994

[14] V. Champac et al., "Electrical model of the floating gate defect in CMOS ICs: Implications on I_{ddq} testing", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 13, No. 3, p. 359, 1994

[15] S. Chakravarty, "On the capability of delay tests to detect bridges and opens", Sixth Asian Test Symposium, p. 314, 1997

[16] J. Figueras and A. Ferre, "Possibilities and limitations of I_{ddq} testing in Submicron CMOS", IEEE Trans. on Components, Packaging, and Manufacturing Technology - Part B, vol. 21, No. 4, p. 352, 1998

[17] J.M. Soden and C.F. Hawkins, "Electrical properties and detection methods for CMOS defects", 1st European Test Conference, p. 159, 1989

[18] M. Abramovici and P.R. Menon, "A practical aproach to fault sinulation and test generation for bridging faults", ITC, p. 138, 1983

[19] R. Rodriguez-Montanes et al. "Current vs. logic testing of gate oxide short, floating gate and bridging faulures in CMOS", ITC, p. 510, 1991

[20] J.M. Acken, "Testing for bridging faults (shorts) in CMOS circuits", Design Automation Conference, p. 717, 1983

[21] A. Ferre et al. "I_{ddq} testing: state of the art and future trends", Integration, the VLSI journal, vol. 26, p. 167, 1998

[22] M. Hashizume et al. "A current sensing circuit for feedback bridging faults", International Worshop on I_{ddq} Testing, p. 110, 1997

[23] R. Rodriguez-Montanes and J. Figueras, "Analysis of bridging defects in sequential CMOS circuits and their current testability", European Design and Test Conference, p. 356, 1994

[24] M. Sachdev, "I_{ddq} and voltage testable CMOS flip-flop configuration", ITC, p. 534, 1995

[25] A. Keshavarzi et al., "Intrinsic leakage in low power deep submicron CMOS ICs", ITC, p. 146, 1997

[26] Siborg Corp. web-site: http://www.siborg.com/

[27] N. Arora, "MOSFET Models for VLSI Circuit Simulation: theory and practice", Wien - New York: Springer-Verlag, 1993

[28] J.R. Soden et al., "Identificating defects in deep-submicron CMOS ICs", IEEE Spectrum, p. 66, September 1996

[29] F. Joel Ferguson, John P. Shen, "A CMOS Fault Extractor for Inductive Fault Analyses", IEEE Transactions on Computer Aided Design, Vol. 7, No. 11, p. 1181, 1988

[30] The National Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, Calif., 1994

[31] D. P. Vallett, "IC Failure Analysis: The Importance of Test and Diagnostics", IEEE Design & Test of Computers, July-September, p.76, 1997

[32] O.V. Maiuri, W.R. Moore, "Implications of voltage and dimension scaling on CMOS Testing: the Multidimensional Testing Paradigm", VLSI test symposium, p.22, 1998

[33] M.C. Hansen, H. Yalcin and J.P. Hayes, "Univeiling the ISCAS-85 Benchmarks: A case study in reverse engineering", IEEE Design & Test of computers, July-September, p.72, 1999

[34] S.D. Millman and J.H. Acken, "Special Application of the voting model for Bridging Faults", IEEE Journal of Solid-State Circuits, vol. 29, No. 3, p. 263, 1994

[35] Web site: http://www.eecs.umich.edu/~jhayes/iscas/benchmark.html

[36] O. Semenov and M.Sachdev, "Impact of technology scaling on bridging fault detections", Canadian Conference on Electrical and Computer Engineering, p. 199, 2000

[37] O. Semenov and M.Sachdev, "Impact of technology scaling on bridging fault detections in sequential and combinational CMOS circuits", IEEE International Workshop on Defect Based Testing, p. 36, 2000

[38] T. Story et al., "Current test and stuck-at fault comparison on a CMOS chip", Electronic-Engineering, vol. 63, no. 779, p. 89, 1991

[39] T. Williams et al., "Iddq Test: Sensitivity Analysis of Scaling", Proceedings of International Test Conference (ITC), p. 786, 1996

[40] F. Joel Ferguson and John P. Shen, "A CMOS Fault Extractor for Inductive Fault Analyses (IFA)", IEEE Transactions on Computer Aided Design, vol. 7, no. 11, p. 1181 1988

[41] H.Vierhaus, W. Meyer and U. Glaser, "CMOS Bridges and Resistive Transistor Faults: I_{DDQ} versus Delay Effects", ITC, p. 83, Oct. 1993

[42] B. Chess and T. Larrabee, "Logic Testing of Bridging Faults in CMOS Integrated Circuits", IEEE Trans. on Computers, vol. 47, no. 3, p. 338, 1998

[43] K.J. Lee et al., "BIFEST: A Built-in Intermediate Fault Effect Sensing and Test generation System for CMOS Bridging Faults", ACM Trans. on Design Automation of Electronic Systems, vol. 4, no. 2, p. 194, 1999

[44] N. Arora, "MOSFET Models for VLSI Circuit Simulation - Theory and Practice", Springer - Verlag/Wien, p.250, 1993

[45] C. Hao et al., "Experimental Determination of Short-Channel MOSFET Parameters", Solid-State Electronics, vol. 28, no. 10, p. 1025, 1985

[46] K. S. Krisch et al., "Gate Capacitance Attenuation in MOS Devices with Thin Gate Dielectrics", IEEE Electron Device Letters, vol. 17, no. 11, p. 521, 1996

[47] C. Hao et al., "Experimental Determination of Short-Channel MOSFET Parameters", Solid-State Electronics, vol. 28, no. 10, p. 1025, 1985

[48] K. S. Krisch et al., "Gate Capacitance Attenuation in MOS Devices with Thin Gate Dielectrics", IEEE Electron Device Letters, vol. 17, no. 11, p. 521, 1996

[49] D. Hoyniak and E. Nowak, "Channel electron mobility dependence on lateral electric field in field-effect transistors", J. of Applied Physics, vol. 87, no. 2, p. 876, 2000

[50] H. Katto "Device Parameter Extraction in the Linear Region of MOSFET's", IEEE Electron Device Letters, vol. 18, no. 9, p. 408, 1997

[51] N.D. Arora "Modeling and Characterization of Ultra Deep Submicron CMOS Devices", IEICE Trans. Electron., vol. E82-C, no. 6, p. 967, 1999

[52] M. Renovell, et. al. "The Configuration Ratio: A Model for Simulation CMOS Intra-Gate Bridge with Variable Logic Thresholds", Dependable Computing, EDCC-1, First

European Dependable Computing Conference Proceedings, Berlin, Germany, #618, p.165, 1994

[53] R.C. Aitken, "Nanometer technology effects on fault models for IC testing", Computer, vol. 32, no. 11, p. 46, 1999

[54] O. Semenov, B. Chatterjee and M. Sachdev, "Impact of technology scaling on bridging fault modeling and detection in CMOS circuits", IEEE International Workshop on Defect Based Testing, p. 45, 2001