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Novel gate and substrate triggering techniques for deep sub-micron ESD protection devices

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Abstract

As technology feature size is reduced, ESD becomes the dominant failure mode due to lower gate oxide breakdown voltage. In this paper, the effectiveness of new gate and substrate triggering techniques has been investigated to lower the trigger voltage of the LVTSCR and MOSFET based ESD protection circuits using 2D simulations and HBM/TLP measurements. The simulation results show that the using these techniques reduces the ESD triggering voltage by 63 and 44% for MOSFET-based and LVTSCR-based ESD structures, respectively, under 2 kV HBM ESD stress. The effectiveness of proposed gate and substrate triggering techniques is also confirmed by the HBM and TLP measurements.

Keywords: Electrostatic discharge (ESD); Gate triggering; Substrate triggering; ESD robustness

1. Introduction

Electrostatic discharge is considered as a major reliability threat in the semiconductor industry for decades. It was reported that ESD and EOS are responsible for up to 70% of failures in IC technology [1]. Therefore, each I/O must be designed with a protection circuitry that creates a discharge path for ESD current. As a CMOS technology scales down, the design of ESD protection circuits becomes more challenging. This is due to thinner gate oxide and shallower junction depth in advanced technologies that makes them more vulnerable to ESD damages. In addition, advanced process techniques, such as silicidation, make ESD performance of protection devises even worse. While the physical dimensions of VLSI devices continue to shrink, the magnitude of the ESD event remains the same.

To test the protection level of ESD devices, different standards are available. Human body model (HBM) and Charged device model (CDM) are more common. The required protection level depends on application and is usually at least 2 kV for HBM and 500 V for CDM.

MOSFETs and silicon-controlled rectifiers (SCRs) are the two popular protection elements that are used in industry [2]. These devices are generally used in gate-grounded-NMOSFET (GG-NMOSFET) and low voltage triggered SCR (LVTSCR) configurations. There are some practical issues related to each of them. GG-MOSFET is usually realized using multiple fingers. In order to obtain maximum protection and avoid current filamentation and thermal runaway [3], all fingers should turn on at the same time. This can be achieved using gate coupling [4], substrate triggering [5] techniques or by applying layout technique, so-called Back-End-Ballast (BEB) poly resistors in compact Merged-Ballast-Circuit (MBC) configurations [6]. In addition, these techniques reduce the first breakdown voltage of MOSFET and further increase the protection level of the MOSFET. Chen et al. explained the operation principles of gate-grounded design, gate-driven design, and substrate triggering design of CMOS devices for ESD protection using energy-band diagrams [7]. On the other hand, the conventional LVTSCR has the first breakdown voltage, which is not low enough to ensure the required protection of a gate oxide in advanced CMOS technologies [8].

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Therefore, substrate and gate triggering have been applied to further reduce the first breakdown voltage. Generally, ESD protection device should have the first breakdown voltage less than the breakdown voltage of the gate oxide, and its holding voltage should be greater than V_{DD} in order to avoid the latch-up possibilities.

In this paper, a new implementation of gate and substrate triggering techniques for ESD NMOSFET and LVTSCR is proposed. These techniques allow the ESD protection devices with the following features:

(1) The triggering voltage (V_{t1}) less than 8 V for MOSFET-based and approximately 12 V for LVTSCR-based ESD protection devices (to prevent the gate oxide breakdown due to ESD event in 0.18 μm CMOS technology).
(2) The holding voltage (V_h) more than 2 V (to avoid latch-up in LVTSCR).
(3) The second (thermal) breakdown voltage (V_{t2}) greater than V_{t1} (to ensure uniform triggering) while maintaining the protection level to at least 2 kV HBM ESD stress.

The rest of the paper is organized as follows: In Section 2, we review the conventional gate and substrate triggering techniques and discuss their impact on ESD robustness. The ESD device structures and ESD protection circuits, used in our research, are described in Section 3. The circuit and device simulation results for 2 kV HBM ESD stress are presented in Section 4. In Section 5, the layout issues of proposed ESD circuits are described. Section 6 presents the measurement results of HBM and TLP testing of LVTSCR-based ESD protection devices. Finally, the conclusions are summarized in Section 7.

2. Gate and substrate triggering techniques

As technology scales down, gate oxide layer becomes thinner, junctions become shallower and length of transistors becomes smaller. Decreasing gate oxide thickness reduces the electric field that can be tolerated by the transistor and therefore, it reduces ESD robustness. In addition, decreasing junction depth reduces the second breakdown current (I_{t2}) and therefore, the ESD robustness (maximum allowed ESD voltage) is degraded. On the other hand, reducing length of transistor reduces the base area of parasitic bipolar transistor, which improves the ESD performance [9].

In order to overcome ESD performance degradation, due to the use of advanced CMOS technology processes, several solutions have been developed over the years. Gate coupling and substrate triggering are considered as important circuit design methods to decrease V_{t1}, to enable uniform triggering of ESD protection device and to increase the ESD robustness (I_{t2}) [4,5,10]. The basic purpose of gate coupling technique is the reduction of V_{t1} by applying a positive voltage to the gate. When the gate is biased slightly above the transistor threshold voltage (V_{th}), the transistor breakdown voltage is reduced. The substrate current of ESD MOSFET helps to forward bias the source-substrate junction. As a result, the triggering voltage is lowered and this improves the turn-on uniformity of multi-finger ESD MOSFET. In order to apply a voltage to the gate during the ESD event, a coupling RC network is traditionally used [11]. Similarly, in substrate coupling, a positive substrate voltage reduces the V_{t1}. This external voltage will increase the base voltage of the parasitic bipolar transistor and hence, smaller voltage is needed to turn on the parasitic bipolar transistor.

Triggering techniques with various implementations can be applied to MOSFETs and SCRs. Since, the triggering voltage of LVTSCR is almost equal to triggering voltage of its built in MOS structure, gate-coupling technique can be applied to LVTSCR as well [12]. In addition, substrate coupling has been reported for SCR [13].

3. Device simulator and proposed ESD protection devices

In our research, we used 2D 'SEQUOIA ESD' simulation software, which was developed by Sequoia Design Systems for characterization of an ESD event [14]. This simulator has built-in device synthesis, mesh generation, device simulation, circuit-device mixed-mode simulation and lattice self-heating simulation modules. Electrothermal simulation has been introduced to general-purpose commercially available device simulation in the early 1990s by TMA [15]. Validity of physical models such as mobility, generation-recombination, impact ionization rates etc. has been confirmed by numerous industrial applications and is generally believed to extend to approximately 700 K. In our case, the Lombardi low electric field and the Caughey–Thomas high electric field mobility models were used. The Chynoweth model and the Shockley–Read–Hall model were used for the modeling of impact ionization and the generation–recombination processes [14].

For the analysis of impact of gate and substrate triggering techniques on the performance of sub-micron ESD devices, the following ESD structures were studied in this work: (1) GG-NMOSFET, (2) N-MOSFET with gate/substrate triggering, (3) LVTSCR and (4) LVTSCR with gate/substrate triggering. LVTSCR structure was implemented as a punch-through-induced protection element [16]. All these circuits were designed using the process parameters of 0.18 μm salicided TSMC CMOS technology with $T_{ox} = 41$ Å. The physical structures of ESD devices, used for simulations, are given in Fig. 1(a) and (b). The schematics of GG-MOSFET and proposed implementations of gate and substrate triggering techniques in MOSFET and LVTSCR are shown in Fig. 2(a)–(c). For the thermal boundary conditions, a thermal electrode was defined at the bottom of the

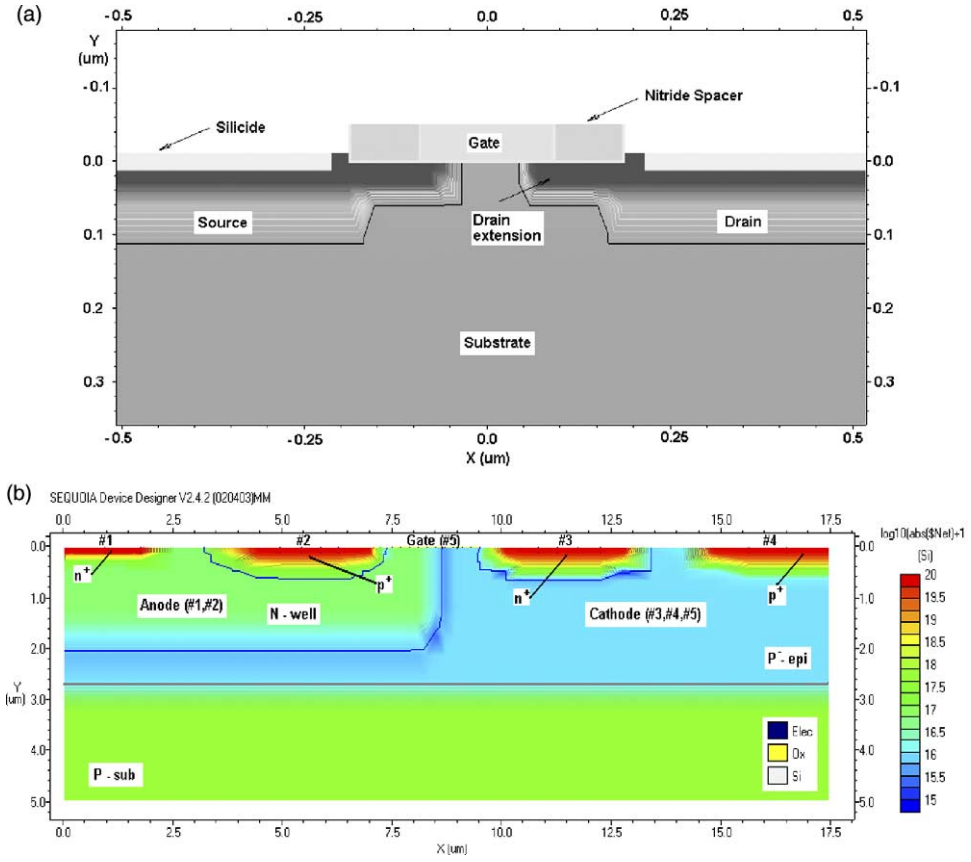

Fig. 1. (a) Cross-section of 0.18 μm silicided GG-NMOSFET, (b) cross-section of LVTSCR.

substrate and the temperature of this thermal electrode is assumed to be the same as the ambient temperature (300 K). All contacts were ideal ohmic electrodes.

Destruction of an ESD device occurs when the temperature reaches the melting point of metallization (660 °C for aluminum based metallization and 1034 °C for copper based metallization), or melting point of silicon (1412 °C) (typically in the gate-to-drain overlap region) [17]. We performed thermal simulations to optimize the size of primary ESD protection devices, shown in Fig. 2. The peak temperature in analyzed ESD devices did not exceed 660 °C at 2 kV HBM ESD stress. These simulations provide a lower bound value for the size of primary ESD device. Note, that layout plays an important role, and improper layout results in hot spots allowing local temperature to rise rapidly resulting in ESD failures. Transistor used for substrate triggering should also be large so as to provide a significant current pumped into the substrate of ESD MOSFET or LVTSCR. On the other hand, the transistor used for gate triggering can be significantly smaller. This transistor only provides the voltage biasing on the gate of ESD devices during ESD event.

Finally, note that to make the accurate evaluation of the ESD protection structure while taken into account spatial current instability and hot spot formation the third dimension along the contacts should be considered. However, 3D simulations are expensive and unstable due to memory requirements, very long simulation time and convergence limitations. Recently, Esmark et al. showed that in case of relatively homogeneous triggering of ESD protection device, 2D device simulations can be used for a worst-case estimation of critical parameters (V_{t1}, V_h, V_{t2} and I_{t2}) of ESD devices [18].

4. Simulation results: HBM ESD stress

During the ESD event, the analyzed devices operate primarily in the snapback mode. To investigate this operating mode, first we performed fast transient simulations under high current conditions. The input voltage is ramped linearly with a high ramp rate (200 V/ns) and is applied to a large resistor (1500 Ω) in series with the ESD device to limit the current. *I–V* characteristics were extracted from these simulations. This is possible because the output voltage and current are function of time. The extracted breakdown *I–V* characteristics of ESD MOSFET-based structures and LVTSCR-based structures are shown in Figs. 3 and 4, respectively. From these graphs we can conclude that proposed gate and substrate triggering techniques reduce the triggering voltage (V_{t1}) of these devices substantially. Substrate triggering has also been

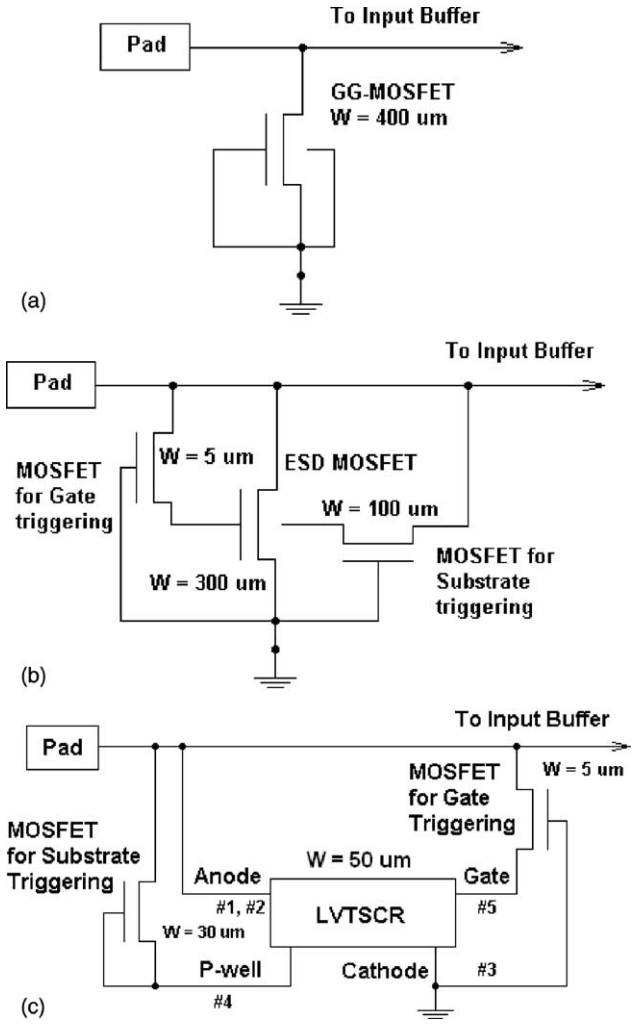

Fig. 2. (a) ESD GG-NMOSFET, (b) ESD MOSFET with gate-substrate triggering, (c) LVTSCR with gate-substrate triggering.

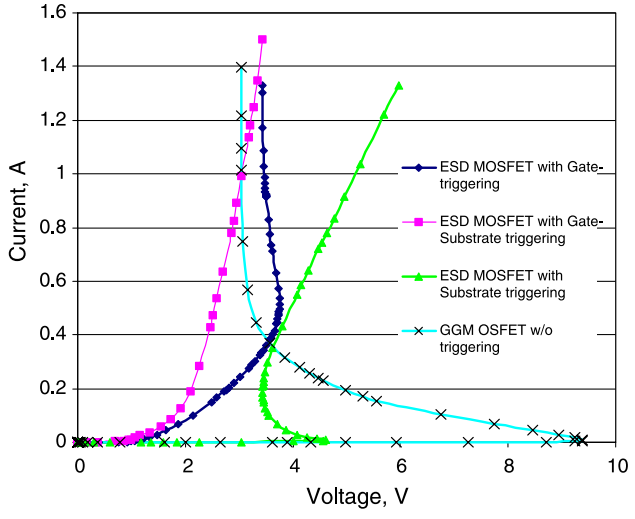

Fig. 3. *I–V* characteristics of ESD MOSFET-based protection circuits.

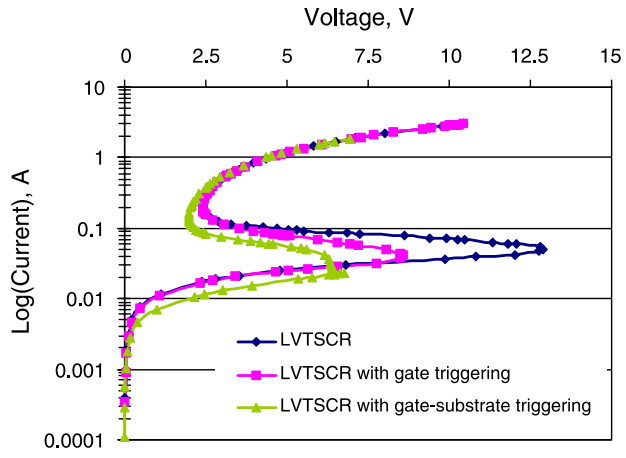

Fig. 4. *I–V* characteristics of ESD LVTSCR-based protection circuits (Semi-logarithmic scale is used to properly extract V_{t1}).

reported to improve the second breakdown current of ESD devices [5]. The second (destructive) breakdown occurs when local temperature reaches melting temperature (1412 °C) of silicon. Simulation results in Fig. 5 confirm that the peak device temperature rises slowly if positive substrate voltage is applied.

After fast transient simulations, we also simulated human body ESD events. The HBM is the principal ESD test method used in industry, and it is specified in the MIL-STD-883E standard (method 3015.7). Typically, HBM ESD waveform is defined as having a rise time of <10 ns and a decay time of about 150 ns. The transient current and voltage waveforms of 2 kV HBM ESD stress used in our simulations are shown in Fig. 6. The simulation results of analyzed ESD structures under 2 kV HBM ESD stress are shown in Figs. 7 and 8. The summary of results is presented in Tables 1 and 2. These results confirm the effectiveness of proposed implementation of gate and substrate triggering techniques under dynamic conditions. It can be seen that

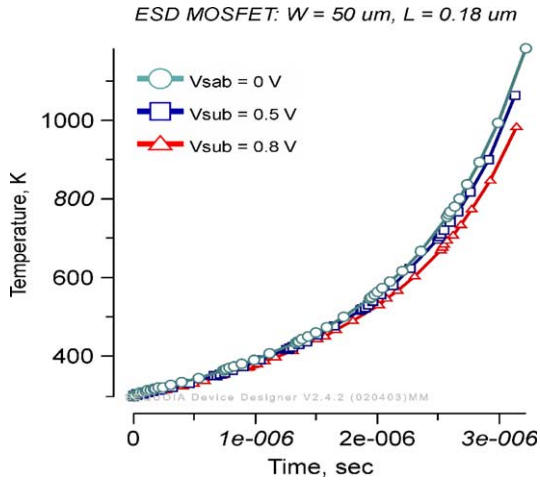

Fig. 5. Hot spot temperature increase when input voltage is ramped slow and linearly.

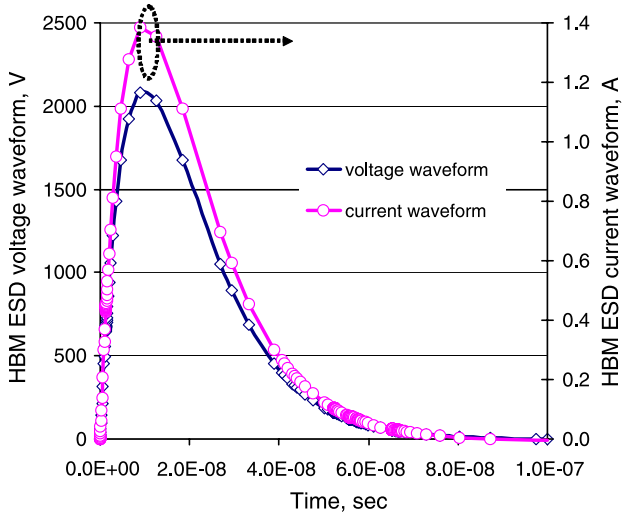

Fig. 6. Two kilovolts HBM ESD stress waveforms used for simulations.

the applying of gate and substrate triggering to N-MOSFET and LVTSCR reduces the first breakdown voltage (V_{t1}) from 9.5 to 3.5 V and from 14.5 to 8.0 V, respectively, ramped linearly with the rate of 200 V/ns, can underestimate the maximum voltage across the protection structure obtained from HBM ESD stress, since this voltage also depends on the rise time of the applied pulse [19]. Although, the gate and substrate triggering techniques have almost the same effectiveness of V_{t1} reduction (31.6%) and both can be used separately under normal operating voltage (1.8 V), the substrate triggering technique is preferable to improve the robustness of ESD circuits than the gate-driven design. The substrate triggering design can enhance the space-charge region to sustain higher ESD current far away from the channel surface and can continually increase the turn-on area for heat dissipation [7]. The holding voltage of LVTSCR-based ESD structures is significantly higher than the supply voltage (1.8 V) used in 0.18 μm CMOS

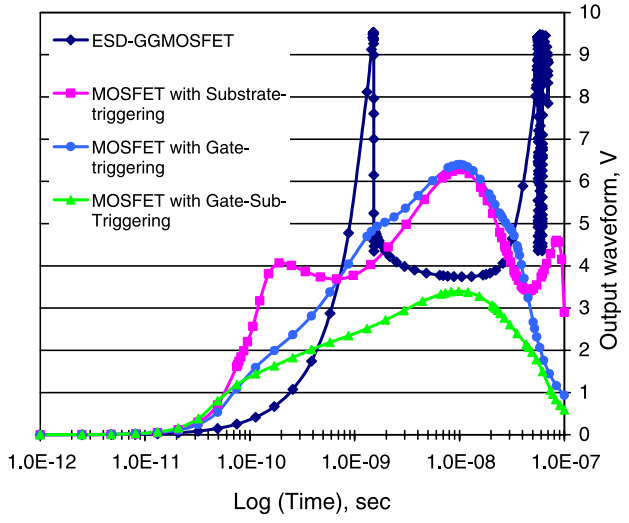

Fig. 7. Output waveform of MOSFET-based protection circuits under 2 kV HBM ESD stress.

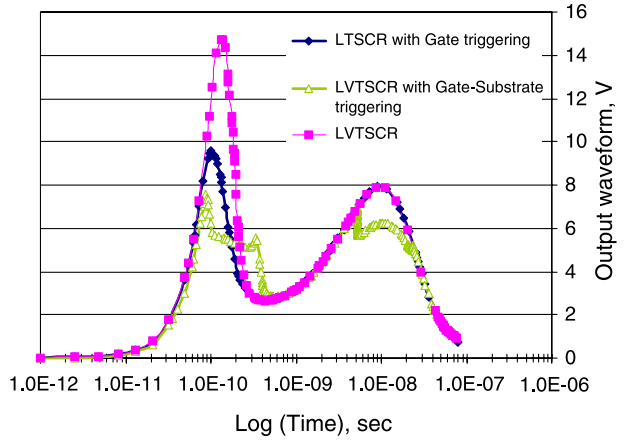

Fig. 8. Output waveform of LVTSCR-based protection circuits under 2 kV HBM ESD stress.

technology. Hence, the proposed LVTSCR-based structures are latch-up free.

However, ESD MOSFET with gate and substrate triggering can be recommended to be use only for low voltage applications (~0.8 V), because of elevated leakage current under nominal voltage conditions. At nominal V_{DD} (1.8 V), the voltage drop on substrate electrode of primary ESD device (Fig. 2(b)) is approximately 80 mV, which slightly reduces the threshold voltage (V_{th}) of ESD MOSFET. Note, that the leakage current of MOSFET is exponentially increased with linear reduction of V_{th}. The second reason of leakage current increase at nominal V_{DD} is that the voltage drop on the gate electrode is approximately 60 mV. This voltage is significantly less than V_{th} (~0.5 V) and cannot switch on the device, but it can increase the leakage current.

The effectiveness of proposed implementation of gate and substrate triggering techniques shown in Fig. 2 can be explained in the following manner. During ESD stress the substrate potential exceeds the built-in p–n junction potential (~0.7 V) and gate potential exceeds the V_{th} (> 0.5 V) as shown in Figs. 9 and 10 for MOSFET and LVTSCR based ESD devices, respectively. These two factors reduce the V_{t1} of ESD structures. Note, that the breakdown voltage (V_{t1}) of ESD structures simulated in fast transient conditions, when the input voltage is ramped

Table 1
Effectiveness of proposed Gate and Substrate triggering in MOSFET-based ESD circuits under 2 kV HBM stress

	Triggering voltage (V_{t1}), (V)	V_{t1} reduction, (%)
GG-MOSFET	9.5	N/A
MOSFET with gate triggering	6.5	31.6
MOSFET with sub-strate triggering	6.5	31.6
MOSFET with gate-substrate triggering	3.5	63.2

Table 2
Effectiveness of proposed gate and substrate triggering in LVTSCR-based ESD circuits under 2 kV HBM stress

	Triggering voltage (V_{t1}), (V)	Holding voltage (V_{hold}), (V)	V_{t1} reduction, (%)
LVTSCR	14.5	2.5	N/A
LVTSCR with gate triggering	9.5	2.5	34.5
LVTSCR with gate-substrate triggering	8.0	2.5	44.8

linearly with the rate of 200 V/ns, can underestimate the maximum voltage across the protection structure obtained from HBM ESD stress, since this voltage also depends on the rise time of the applied pulse [19]. Although, the gate and substrate triggering techniques have almost the same effectiveness of V_{t1} reduction (31.6%) and both can be used separately under normal operating voltage (1.8 V), the substrate triggering technique is preferable to improve the robustness of ESD circuits than the gate-driven design. The substrate triggering design can enhance the space-charge region to sustain higher ESD current far away from the channel surface and can continually increase the turn-on area for heat dissipation [7]. The holding voltage of LVTSCR-based ESD structures is significantly higher than the supply voltage (1.8 V) used in 0.18 μm CMOS technology. Hence, the proposed LVTSCR-based structures are latch-up free.

5. Layout of proposed ESD devices

Any ESD protection technique adds extra devices to the I/O circuits and inevitably introduces parasitic effects to these circuits. This adversely influences the I/O performance, which is becoming the limiting factor in RF ICs and high-speed I/O interface designs. Previously, it was reported

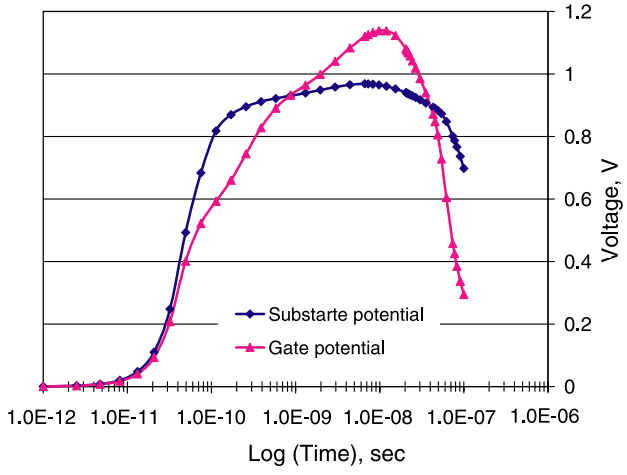

Fig. 9. Gate and Substrate potentials in ESD MOSFET with gate–substrate triggering under 2 kV HBM ESD stress.

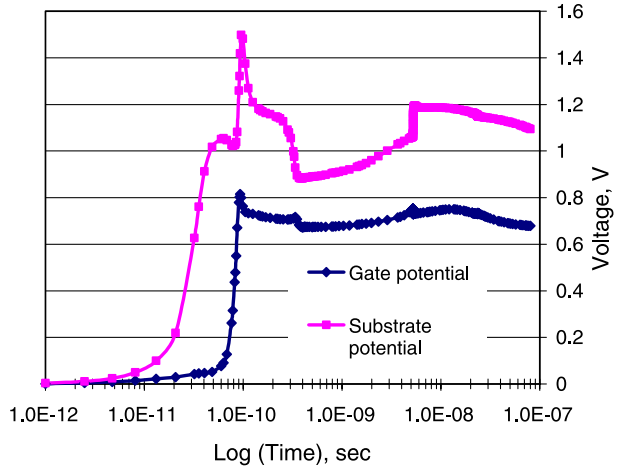

Fig. 10. Gate and substrate potentials in LVTSCR with gate–substrate triggering under 2 kV HBM ESD stress.

that due to the large internal parasitic capacitance, the conventional MOSFET-based ESD designs are not suitable for such critical applications and LVTSCR-based ESD protection devices were proposed [20,21]. Consequently, the proposed LVTSCR-based ESD protection circuits were implemented in silicon to verify simulation results. The robustness of ESD protection devices is very sensitive to layout. The thermal damages of ESD protection structures usually come from current crowding induced local overheating stemming from layout discontinuities. For example, the current crowding occurs at the corners and edges of diffusion/metal layers. Therefore, layout is an extremely important for realizing robust ESD protection circuits. In our investigation, we used the SEMATECH ESD layout design guide to design a test chip with LVTSCR protection devices [22]. The developed test chip had the following ESD structures: conventional LVTSCR, LVTSCR with gate triggering (GT-LVTSCR), LVTSCR with substrate triggering (ST-LVTSCR) and LVTSCR with gate and substrate triggering (GT-ST-LVTSCR), as shown in Fig. 2(c). The developed layout of LVTSCR (the total width is 50 μm) with gate and substrate triggering transistors is shown in Fig. 11.

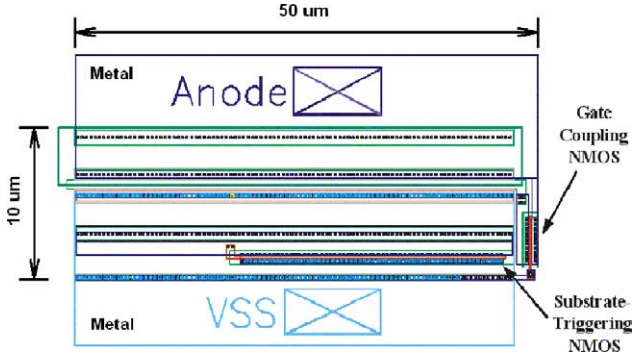

Fig. 11. Layout of two-fingers LVTSCR with proposed implementation of gate and substrate triggering.

6. Experimental results

The designed test chip with LVTSCR-based ESD protection circuits was fabricated in TSMC using 0.18 μm salicided CMOS technology (T_{ox} = 41 Å). The first experiments were using 2 kV human body model (HBM) ESD tests. These tests were performed using IMCS-700 HBM/MM ESD tester. All developed LVTSCR-based ESD structures passed the positive and the negative 2 kV HBM ESD tests. To extract V_{t1} and V_h parameters from measurements, the Transmission Line Pulse (TLP) testing was performed using the Pulsar 900 TLP Test System [23]. The TLP pulse duration was 100 ns and the rise time (10–90%) was 10 ns. The obtained results are shown in Fig. 12.

To extract I_{t2} and V_{t2} parameters, we repeated TLP testing at stronger stress conditions. The leakage current was measured between TLP pulses at V_{DD} = 2 V to indicate the start of irreversible device degradation leading to catastrophic failure. The results of high stress TLP measurements for LVTSCR structure are depicted in Fig. 13. Similar measurements were performed for other ESD structures.

The extracted parameters of developed LVTSCR-based ESD protection circuits are summarized in Table 3. The HBM ESD robustness can be expressed as [10]:

$$V_{ESD} = (1500\ \Omega + R_{on\ device})I_{t2} \approx 1500\ \Omega \times I_{t2} \quad (1)$$

In Eq. (1), the 1500 ω is the discharge resistance of the HBM ESD event and $R_{ondevice}$ is the equivalent resistance of ESD protection device in the ESD-stress condition. Generally, $R_{ondevice}$ is much smaller than 1500 ω. For our LVTSCR-based ESD circuits, $R_{on\text{-}device}$ is approximately 4.5 ω.

Experimental results presented in Table 3 confirm the simulation results shown in Table 2 that the proposed implementation of gate and substrate triggering techniques are effective in reducing the triggering voltage (V_{t1}) of LVTSCR-based ESD protection circuits. However, measured reduction in triggering voltage due to proposed techniques is less than predicted by the simulation results.

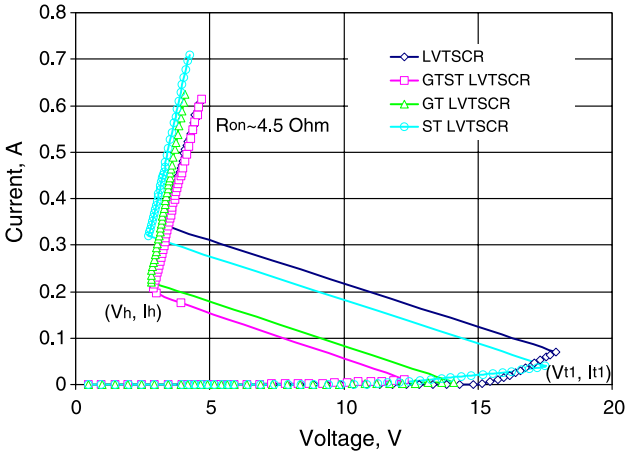

Fig. 12. TLP *I–V* curves of LVTSCR-based ESD protection devices.

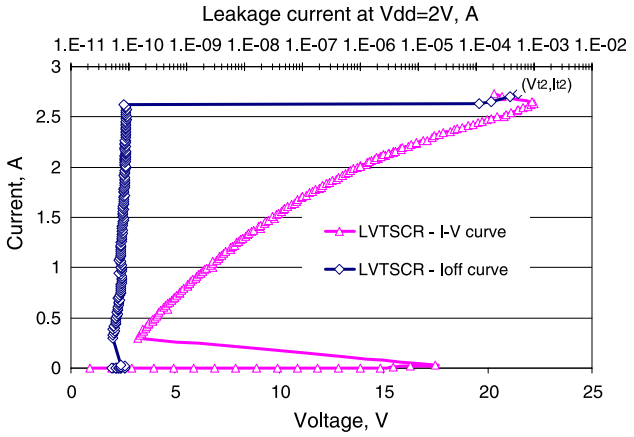

Fig. 13. TLP thermal (second) breakdown *I V* characteristics and leakage current (I_{OFF}) curve of LVTSCR structure.

For example, the measured reduction of V_{t1} for GT-ST-LVTSCR with respect to LVTSVR is 33% compared to 44.8% in simulation. This can be attributed to relatively simplified, 2D, model.

The leakage current of GT-LVTSCR and GT-ST-LVTSCR obtained from TLP measurements at V_{DD} = 2 V is significantly higher than the leakage current of LVTSCR and ST-LVTSCR. This is because the leakage current measurements were performed between multiple TLP pulses. As a result, a significant effective charge is accumulated at the gate electrode of GT-LVTSCR and GT-ST-LVTSCR, which results in elevated leakage. The gate electrode of LVTSCR and ST-LVTSCR structures is grounded and therefore no charge accumulation occurred. Table 4, depicts the pre-TLP measurement leakage for implemented LVTSCR based ESD protection circuits.

Although, different implementations of gate and substrate triggering techniques were proposed in literature [4,5,10–13], most triggering techniques increase leakage

Table 3
Parameters of LVTSCR-based ESD circuits obtained from TLP measurements

Parameters of ESD devices	LVTSCR	ST-LVTSCR	GT-LVTSCR	GT-ST-LVTSCR
Trig. Voltage (V_{t1}), (V)	18	17 (6%↓)	14 (22%↓)	12 (33%↓)
Holding voltage (V_h), (V)	3	3	3	3
Second breakdown current (I_{t2}), (A)	2.65	2.0	2.15	2.10
Second breakdown voltage (V_{t2}), (V)	22	12.5	13	13
Leak current (I_{off}, (A/μm)) at V_{DD} = 2 V	3.03e–12	6.2e–12	6.1e–9	2.1e–8
HBM ESD robustness (kV)	4.0	3.0 (25%↓)	3.2 (20%↓)	3.1 (23%↓)

Table 4
Leakage current of LVTSCR-based ESD circuits measured at $V_{DD}=2$ V before TLP testing

Parameter	LVTSCR	ST-LVTSCR	GT-LVTSCR	CT-ST-LVTSCR
Leakage current (A/μm)	2.0×10^{-12}	4.5×10^{-12}	1.4×10^{-11}	1.1×10^{-10}

currents as shown in Table 4. The similar observation was done by Ker et al. for substrate triggering technique used for ESD protection design of mixed-voltage I/O circuits [24]. It can be a limiting factor for low-power applications to use both gate and substrate triggering techniques in ESD circuits. The possible reason of increased leakage current is the voltage drop on the gate (~70 mV) and substrate (~80 mV) terminals of GT-ST-LVTSCR structure at nominal V_{DD} (1.8 V).

The usage of MOS transistors for gate and substrate triggering of LVTSCR structure may also marginally reduce the ESD robustness of complete ESD circuit (Table 3) since these MOSFETs are likely to fail earlier than LVTSCRs in high HBM ESD stress.

7. Conclusion

This paper reports a new implementation of gate and substrate triggering techniques, which can be used for ESD robustness improvement in sub-micrometer CMOS technologies. The presented device and circuit simulation results support this conclusion and show that the ESD triggering voltage is reduced by 63.2 and 44.8% for MOSFET-based and LVTSCR-based ESD structures for 2 kV HBM ESD stress, respectively. The obtained measurement data confirm the simulation results and show that the LVTSCR-based ESD protection circuit with gate and substrate triggering reduces the LVTSCR triggering voltage by 33%. However, these triggering techniques may increase the leakage current of ESD protection circuits, hence they are not suitable for low-power applications. The proposed ESD protection circuits are capable of withstanding 3–4 kV of HBM ESD stress.

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