A Comparative Analysis of Dual Edge Triggered Flip-Flops

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Abstract

A dual edge triggered (DET) flip-flop responds to both edges of the clock. Hence the usage of DET flip-flops reduces clock related power dissipation in digital VLSIs. DET flip-flops are also desirable in high performance applications since clock frequency can be halved for the same data throughput. In this article, we compare several published implementations of DET flip-flops for performance, power consumption. A modified DET flip-flop is proposed that exhibits improved specifications. Preliminary simulations are also carried out to evaluate DET flip-flop sensitivities to VDD, temperature, clock and data rise times, etc.

1 Introduction

With ever increasing integration complexity of modern VLSI, low power is becoming a critical issue. Power dissipation, active as well as passive, has become a limiting factor for transistor performance, long term device reliability and further integration. Soaring clock frequencies in high performance processors are contributing to increased power consumption. As we scale devices aggressively towards sub 0.25 micron, scaling paths for high performance and low power applications diverge [1]. For high performance ICs, containment of power is desirable from reliability, transistor performance and cooling considerations. For low power, battery operated systems low power is necessary to extend the battery life.

Unlike single edge triggered (SET) flip-flop, DET flip-flop triggers at its both clock edges. Hence, the clock frequency can be reduced to half while maintaining the same data throughput. The reduced clock frequency not only results in reduced active power dissipation but also eases clock generation and propagation. Therefore, usage of DET flip-flop is desirable irrespective of high performance or low power application.

However, caution should be exercised while using DET flip-flops. High performance and low power applications put severe constraints on the usage DET flip-flops. For high performance applications, flip-flops should have low propagation delay, insensitivity of propagation delay to temperature and clock rise and fall times. On the other hand, in low power application, battery voltage deteriorates; therefore, graceful degradation of flip-flop parameters with supply voltage is highly desirable.

2 Review and Motivation

In digital CMOS circuits, active or dynamic power consumption is the main source of energy dissipation. The static power component is relatively small. This scenario is expected to change owing to increased sub-threshold leakage current in deep sub-micron transistor [2]. However, sub-threshold leakage reduction techniques are addressed elsewhere and are beyond the scope of this article.

The clock power dissipation in synchronous VLSI circuits is divided into three major components [3]:
(i) power dissipation in clock net, (ii) power dissipation in clock buffers and (iii) power dissipation in flip-flops. The total power dissipation of the clock network can be computed as follows:

$$P_{clk} = V^2_{dd} \{f_{clk} (C_{clk} + C_{ff,clk}) + f_{data} C_{ff,data}\}$$

where f_{clk} is the clock frequency; f_{data} is the average data frequency; C_{clk} is the total capacitance seen by the clock network; $C_{ff,clk}$ is the capacitance of the clock path; $C_{ff,data}$ is the capacitance of the data path. This equation illustrates that the power dissipation depends both on the clock and on the data.

One of the earliest DET flip-flops is proposed by Unger in 1981 [4]. He suggested DET flip-flop usage would result into reduced power consumption in digital circuits. A number of DET flip-flop implementations were proposed in 90s once their potential for low power applications was recognized.

In spite of several recent DET flip-flops and their potentials in power reduction, DET flip-flops are not widely used. DET flip-flops have larger number of transistors compared to a conventional flip-flop. As a consequence, DET flip-flops have larger propagation delay. DET flip-flops also have larger input capacitance that makes their setup and hold times larger compared to the conventional flip-flop.

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This article is organized as follows. In following section we study some of the published DET flip-flop configurations. In Sections 4 and 5, simulation results are presented. Finally in Section 6, conclusions are drawn.

3 DET Flip-Flops Implementations

In this study, we restricted ourselves to static implementations of DET flip-flops owing to their insensitivity to noise and higher design robustness. Clock buffers and output buffers are added in some of the implementations for comparison purposes. Figures 1 to 5 show DET flip-flop implementations proposed in literature. In this article, they will be referred to as DET1 [5], DET2 [7], DET3 [8], DET4 and DET5 [3], respectively. DET 6 is a modified version of DET3 and exhibits improved characteristics. These six DET flip-flops are of similar structure: two parallel-connected latches driving the inputs of a multiplexer.

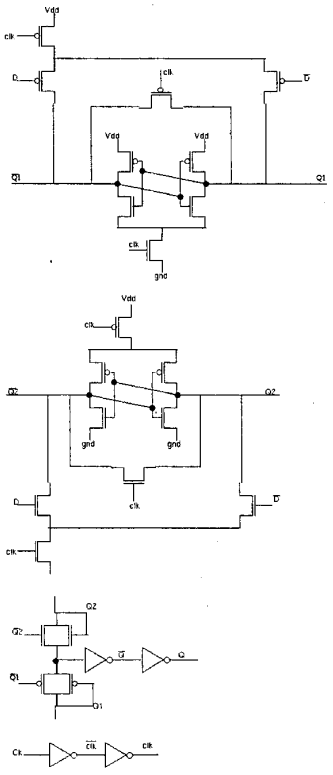

Figure 1: An implementation of DET flip-flop (DET1): latch 1, latch 2 and pass-transistor logic [5].

DET1 is illustrated in Figure 1 and has two cross-coupled latches that are enabled/disabled by the clock. When the clock is low, latch 1 is disabled and latch 2 is enabled. A high clock enables latch 1 and disables latch 2. Disabled latch 1 has both of its outputs set to high and both outputs of disabled latch 2 are set to low. With the pass-transistor logic, the DET flip-flop output is determined by the enabled latch. In addition, unlike the other implementations, DET1 uses single phase of the clock. However, the DET flip-flop requires data inversion. This implementation allowed Lu and Ercegovac [5] to reduce number of transistors to implement a DET flip-flop to 26 from 36 proposed by Unger [4].

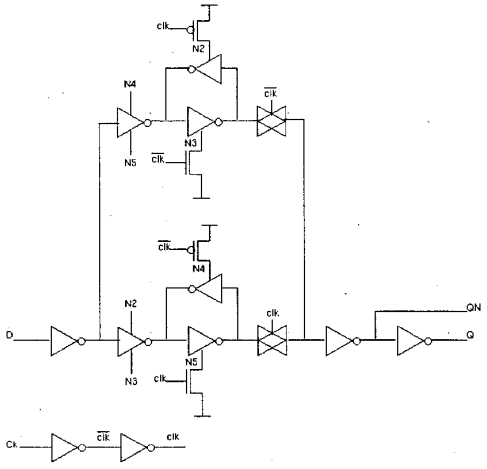

Figure 2: The implementation of DET flip-flop (DET2) proposed in [7].

Gago et al. [7] modified the DET flip-flop proposed by Lu and Ercegovac. However, the operation and performance of DET2 are highly dependent on transistor dimensions. This imposes certain restrictions in porting a design from one technology to another. Moreover, transmission gates are added on the output path of this configuration to reduce the output capacitance, as well as to balance the two (high and low) logic levels. The clock signal controls the enabling of the latches, the input buffers and the output pass gates. Only one input buffer and one latch are enabled at any one time. Thus, DET2 offers possible higher energy saving comparing to the other five configurations for the disabled buffer and latch are turned off completely by the control transistors. Because of this, DET2 also provides a good level of immunity to metastability [7].

Hossain et al. [8] further simplified design of the DET flip-flop. This flip-flop is illustrated in Figure 3. DET flip-flops have two latches in parallel connected to D input. Therefore, DET flip-flops have larger input

capacitance, poorer metastability and offer greater propagation delay sensitivity with respect to changes in supply voltage and clock rise/fall times. Upon this shortcoming of DET, Llopis and Sachdev modified DET3 to realize DET4 and DET5. In these two configurations, transmission gate pairs were used instead of only n channel pass gates. This change was made to have equal propagation delay for logic 0 and 1. In DET4 and 5 data input was buffered to reduce the impact of the above mentioned issues on DET performance. In addition, in DET5 the outputs of latches are buffered. This arrangement improves the propagation delay as well as I_{DDQ} testability of the flip-flop [3,9]. However, number of transistors may increase resulting in higher power dissipation.

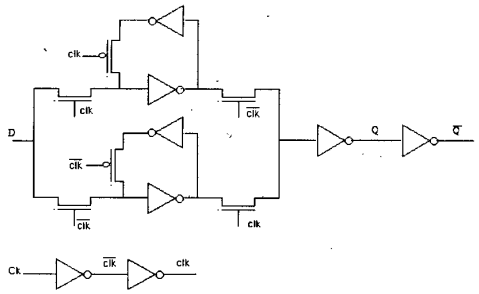

Figure 3: The DET flip-flop (DET3) proposed in [8].

It is observed that DET3 has large difference between data rising delay (t_{plh}) and data falling delay (t_{phl}). Such data dependent propagation delay is not desirable in high performance applications. This difference can be reduced significantly by replacing n pass transistor with complementary transmission gate pair at outputs of latches. This modification is illustrated in Figure 6.

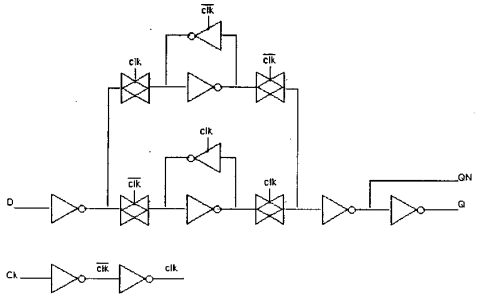

Figure 4: An implementation of DET flip-flop (DET4) proposed in [3].

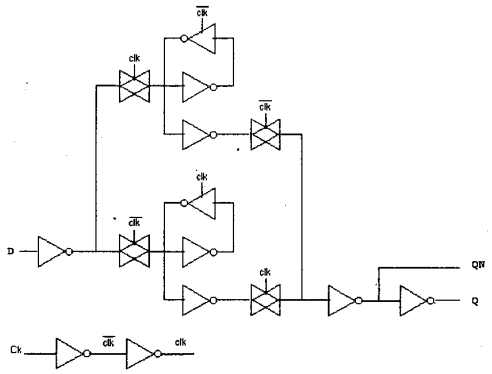

Figure 5: Another implementation of DET flip-flop (DET5) proposed in [3].

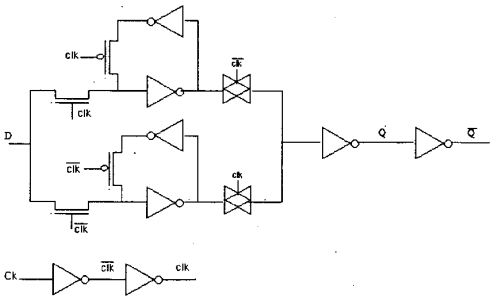

Figure 6: DET6: A modification of DET3 with complementary transmission gates in the output path.

4 Performance Parameters

For this analysis, single poly, triple metal 0.35 micron CMOS technology is used. Transistor sizes are selected to be representative of the technology. For this comparative study, transistors sizes in all flip-flops were kept of the comparable dimensions, except for the DET2. It is because DET2 cannot operate properly without non-trivial transistor sizing. All DET flip-flop configurations are circuit simulated with HSpice in Cadence design environment. A moderate clock frequency of 50 MHz is chosen for this analysis. Data and clock rise/fall times of 1ns are used. In addition, the DET flip-flops are simulated at room temperature, 3.3V input supply voltage and no load conditions.

The performance of a flip-flop is characterized by its setup and hold times, propagation delay, and power dissipation. The performance parameters of DET flip-flops are compiled in Table 1. As shown in the table, DET3 depicts the smallest setup time while DET5 has the largest setup time. Flip-flops often show negative hold time. DET5 has the most negative hold time. The output of a flip-flop is unpredictable if the input data arrives between setup and hold times. This time difference is also interpreted as metastability window and is a measure of flip-flop performance [9]. This window should be as small as possible. DET4 and DET5 show better metastability performance compared to other flip-flops. DET3 has the smallest propagation delay. However, as mentioned before, it also has the largest difference between tplh and tphl delays. DET1 on the other hand has the largest propagation delay followed by DET2.

Table 1: DET flip-flops performance parameters. Measurements are taking at room temperature, 3.3V input supply voltage, 50MHz clock frequency, 1ns clock and data rise and fall times, and no load conditions.

	DET1	DET2	DET3	DET4	DET5	DET6
Setup (ps)	-130.0	190.0	190.0	610.0	270.0	240.0
Hold (ps)	340.0	-110.0	-20.0	-250.0	-130.0	-20.0
t_{plh} (ps)	662.9	570.0	321.9	458.2	458.3	427.5
t_{phl} (ps)	717.9	571.3	512.5	500.3	442.4	453.3
Prop. Delay (ps)	690.4	570.7	417.2	479.3	450.4	440.4
Power Diss. (uW)	370.3	372.6	325.48	256.84	425.7	292.71

For low power applications, power consumption is an important parameter. DET4 has the lowest power dissipation, followed by DET3. DET5 owing to the large number of transistors has the largest power dissipation figure. It is interesting to compare DET3, DET4 and DET6. DET 4 and DET6 have lower power dissipation in spite of larger number of transistors compared to DET3. In DET4 and DET6, n channel pass transistors have been replaced by transmission gate pairs which does not have threshold drop associated with them.

5 Environmental Sensitivity

The sensitivity of a flip-flop to the variation of environmental parameters can be used to determine the robustness of a flip-flop. In this comparative analysis, sensitivity of DET flip-flops to parameters such as temperature (T), supply voltage (V_{dd}), load (C), clock and data rise (t_r) and fall (t_f) times are examined.

5.1 Clock and Data Rise and Fall Times

Figure 7 illustrates the propagation delay (t_{pd}) of DET flip-flops is a function of clock and data rise and fall times. In the ideal case (i.e. zero rise and fall times), DET1 and DET2 have substantially higher propagation delays compared to the other DET flip-flops. On the other hand, DET3 flip-flop exhibits the smallest propagation delay amongst all.

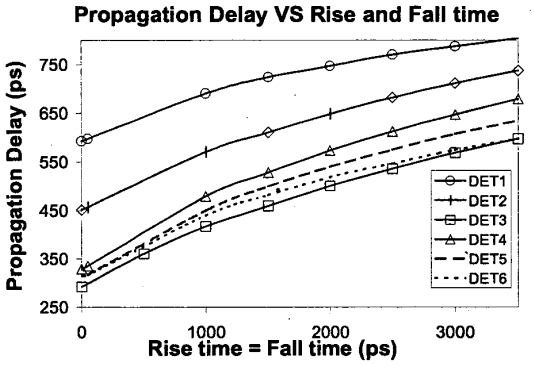

Figure 7: Propagation delay as a function of clock and data rise and fall times.

As the rise and fall times increase, propagation delays of flip-flops also increase monotonically. However, all the DET flip-flops have different rate of change of delays. As depicted in the figure, DET3 and DET4 have a higher rate of increase than the other flip-flops. At very high values of rise and fall times (e.g. 3.5ns) the propagation delays of DET3 and DET6 become comparable.

As mentioned earlier, DET3 has the biggest difference between propagation low to high (t_{plh}) and propagation high to low (t_{phl}). As the rise and fall times increase, the difference also increases. Therefore, DET6 performs the best in terms of sensitivity on clock and data rise and fall times.

5.2 Supply Voltage

Battery voltage decreases overtime. Therefore, low sensitivity to supply voltage is desirable for battery powered applications. Transistor delay increases as supply voltage is reduced. Therefore, logic delay is also increased as supply voltage is reduced (Figure 8). However, secondary factors such as pass transistors, parasitic capacitance, number of transistors in a flip-flop play a role in determining overall flip-flop delay as a function of supply voltage.

As depicted in Figure 8, DET1 and DET2 have the highest propagation delay. The other DET flip-flops have relatively smaller propagation delays. DET3 has the smallest propagation delay when V_{dd} is 3.3V. However, since DET5 varies at the slowest rate with V_{dd} while DET3 varies at a comparatively higher rate, DET5 in

turns has the lowest propagation delay when the supply voltage is as low as 2V. Although DET5 has the lowest propagation delay, DET6 also has a comparable delay value.

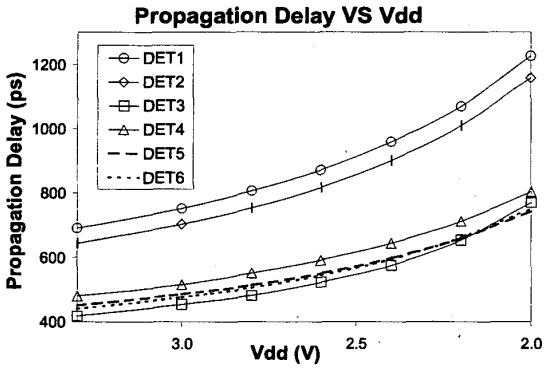

Figure 8: Propagation delay as a function of supply voltage (V_{dd}).

5.3 Temperature

Transistor switching delay increases monotonically as temperature is increased. This is owing to mobility degradation at higher temperature. All DET flip-flops exhibit higher propagation delay with temperature (Figure 9).

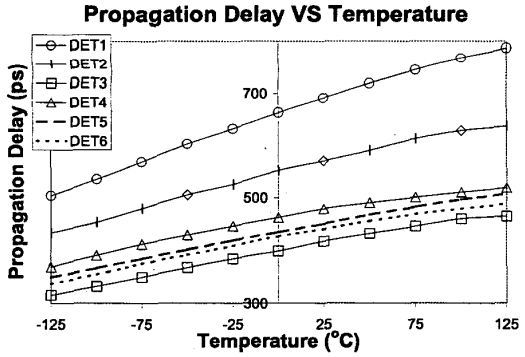

Figure 9: Propagation delay as a function of temperature.

5.4 Output Load

Figure 10 illustrates the DET flip-flop propagation delay as a function of output load capacitance. DET3 shows higher rate of delay increase compared to any other DET flip-flop. DET3 utilises n-channel pass transistors, which pass logic 1 with a threshold voltage drop. As a consequence the drive capability of the output buffer is restricted. It becomes more and more pronounced as output load is increased.

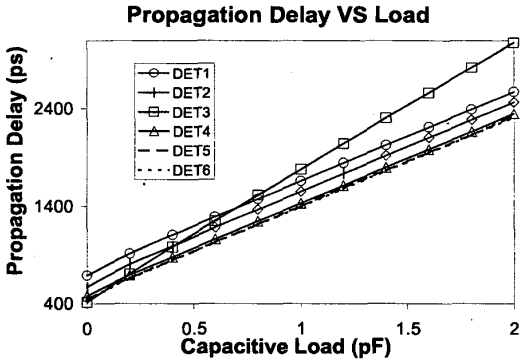

Figure 10: Propagation delay as a function of output load.

6 Conclusion

According to the preliminary comparative analysis of the DET flip-flop characteristics and sensitivities, DET6 is found to have the best performance among the DET flip-flops in discussion. Further investigations are to be done. These flip-flops will be incorporated into a larger integrated circuit or application to evaluate the power saving, as well as the robustness of the designs.

7 References

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