E&CE 327 Final

2008t1 (Winter)

Instructions and General Information

- 100 marks total
- Time limit: 2.5 hours (150 minutes)
- Calculators are allowed
- No books, no notes, no computers
- If you need extra paper, request some from a proctor.
- Write neatly.
- **The proctors and instructors will not answer questions, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.**
- **To earn partial credit, you must show the formulas you are using and all of your work.**
- **Justifications of answers will be marked according to correctness, clarity, and conciseness.**

Name: _____

UWUserid: _____

Potentially Useful Information

$$\mathsf{P} = \frac{1}{2}(\mathsf{A}\times\mathsf{C}\times\mathsf{V}^2\times\mathsf{F}) + (\tau\times\mathsf{A}\times\mathsf{V}\times\mathsf{ISh}\times\mathsf{F}) + (\mathsf{V}\times\mathsf{IL})$$

$$\mathsf{T} = \frac{\mathsf{Ins}\times\mathsf{C}}{\mathsf{F}}$$

$$\mathsf{F} \propto \frac{(\mathsf{V}-\mathsf{Vt})^2}{\mathsf{V}}$$

$$\mathsf{P} = \mathsf{V}\times\mathsf{I}$$

$$\mathsf{P} = \frac{\mathsf{W}}{\mathsf{T}}$$

$$\mathsf{IL} \propto e^{\frac{-q\times\mathsf{Vt}}{k\times T}}$$

$$\mathsf{S} = \frac{\mathsf{T1}}{\mathsf{T2}}$$

$$\mathsf{M} = \frac{\mathsf{F}/10^6}{(\sum_{i=0}^{n}\mathsf{PI}_i\times\mathsf{C}_i)}$$

$$q = 1.60218\times10^{-19}\mathrm{C}$$

$$k = 1.38066\times10^{-23}\mathrm{J/K}$$

$$\log_x y = \frac{\log y}{\log x}$$

Q0 (1 Mark) !!Almost Free!!

(*estimated time: 0 minutes*)

Ten years from now, what, if anything, will you remember about this course, other than TimBits?

Q1 (20 Marks) Short Answer

(*estimated time: 20 minutes*)

Q1a (5 Marks) Area

How many generic FPGA cells are required to implement the VHDL code below? **For full marks, you must justify your answer.**

```
sel           : std_logic_vector(1 downto 0);
a, b, c, d, z : signed(3 downto 0);
...
z <=   a when sel = "00"
  else b when sel = "01"
  else c when sel = "10"
  else d;
```

Q1b (5 Marks) Timing Analysis

Briefly describe what a *late side input* is, and explain what could happen if we ignore late side inputs.

Example: *A late side input is a student who enters a lecture through a side door after the lecture has started. If we ignore late side inputs, then we lose the opportunity to enjoy a diversion from the boring ramblings of the instructor.*

Q1c (10 Marks) Functional Verification

Your manager recently attended a conference on Assertion-Based Verification (ABV) and wants to explore whether to adopt ABV in the verification process. She has asked you to prepare a brief information sheet for discussion in the group.

Briefly describe what an assertion is and how it is used in verification.

List any specification styles that are alternatives to assertions.

Describe the types of circuits that are best suited for assertions.

Describe the types of circuits for which assertions are a poor choice of specificatio style.

Q2 (20 Marks) Performance

(*estimated time: 20 minutes*)

You are designing a Waterluvian filter for image processing. The first phase of the Waterluvian filter enhances yellow and black colours while converting purple to gray. The second phase does edge detection.

The current plan is to implement the complete Waterluvian filter in software. Your task is to evaluate the option of a mixed hardware-software system where the first phase is run in software and the edge detection is done in hardware.

Statistics for Waterluvian filter

Microprocessor clock speed	500 MHz
Pixels per image	350,000

Statistic for sofware Waterluvian filter

The total time to run the Waterluvian filter on one image in software is 30 milliseconds.

Statistics for software edge detection routine

	CPI	Number of instructions
Arithmetic	1.0	2.7×10^6
Load	1.6	1.4×10^6
Store	1.2	0.8×10^6
Branch	1.4	0.5×10^6

NOTES:

1. While the hardware edge detector is running, the microprocessor is idle.

Q2a (12 Marks) Hardware performance

Calculate the minimum performace for the hardware edge detector such that the hardware-software Waterluvian filter is 40% faster than the software Waterluvian filter.

NOTES:

1. Performance is measured in pixels-per-second.
2. Write the answer on the next page.

Minimum pixels-per-second

Q2b (8 Marks) Time to market

The average performance of Waterluvian filters increases 1.5% per week. The software Waterluvian filter is predicted to be 10% faster than average at the time that it is finished.

Assume that the hardware-software Waterluvian filter achieves the 40% performance improvement from part a, but delays your project by 14 weeks. What will be the performance of the hardware-software system in comparison to the average Waterluvian filter at the time that the hardware-software system is finished?

Performance improvement

Q3 (20 Marks) Power

(*estimated time: 25 minutes*)

You have been asked to design a clock-gating circuit for the circuit described below. Without clock gating, the circuit is 45% over its power budget.

Area of main circuit	200 cells
Activity factor	60%
Percentage of valid input data	40%
Average length of continuous sequence of valid parcels	50 clock cycles
Latency	20 clock cycles

Q3a (12 Marks) Maximum Area

What is the maximum area that your clock gating circuit can use without going over the power budget?

NOTES:

1. If you do not have enough information to answer the question, make reasonable assumptions about the values, or describe the additional information that you need and how you would use it to calculate the answer.
2. If you cannot reduce the power to within the power budget, calculate the minimum percentage over the power budget that you can reduce the power to.

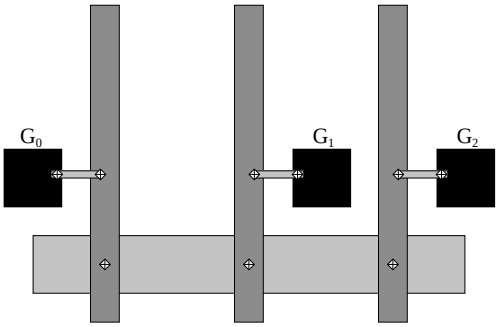
Q3b (8 Marks) Clock Gating Design

Briefly describe your design for the clock gating circuit. You may describe the design in words, draw a circuit, or use both text and a picture.

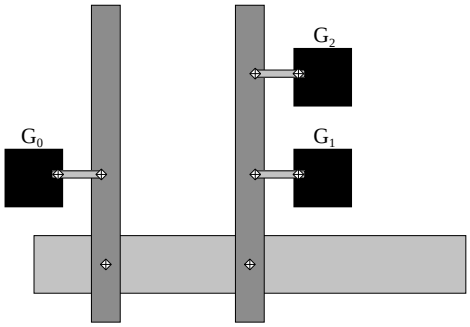
Q4 (20 Marks) Timing Analysis

(*estimated time: 25 minutes*)

In this question you will analyze the 2 layouts below using the Elmore delay model.



Layout-A



Layout-B

Symbol	Description	Capacitance	Resistance
	Interconnect level 3	C_X	0
	Interconnect level 2	C_Y	0
	Interconnect level 1	0	0
	Gate	C_L	0
	Antifuse	0	R

Q4a (10 Marks) Minimum Delay

Which of the layouts has the least delay from G_0 to G_2? **Justify your answer in terms of the Elmore delay model.**

NOTES:

1. If you do not have sufficient information to answer the question, find an equation for the relationship between C_X, C_Y, and C_L such that the two layouts have the same delay (An example equation is: $C_X = C_Y + C_L$).
2. The capacitance of a wire is independent of distance and location on the wire.
3. Write your answer on the next page

Layout with least delay, or equation

Q4b (5 Marks) Alternative layout

In Layout A, how would the delay from G_0 to G_2 be affected by swapping the location of G_1 and G_2? **Justify your answer in terms of the Elmore delay model.**

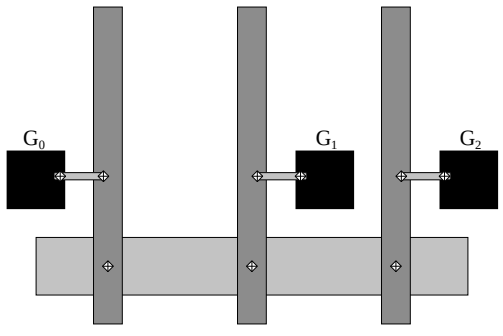
	Increase	**No change**	**Decrease**	**Insufficient info**
Delay change	☐	☐	☐	☐

Q4c (5 Marks) Low-res antifuse

The FPGA layout rules allow one of the antifuses to be a special low-resistance antifuse which has significantly less resistance than a normal antifuse. For layout-A, which antifuse would you choose to have low-resistance to minimize the delay from G_0 to G_2?

NOTES:

1. Indicate your choice for the low-resistance antifuse by circling it in the picture below

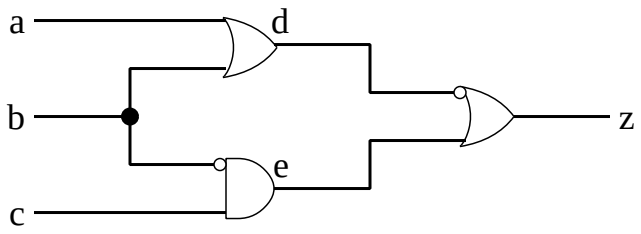


Layout-A

Q5 (20 Marks) Testing and Faults

(*estimated time: 35 minutes*)

In this question, you will analyze the circuit below for single stuck-at faults.



NOTES:

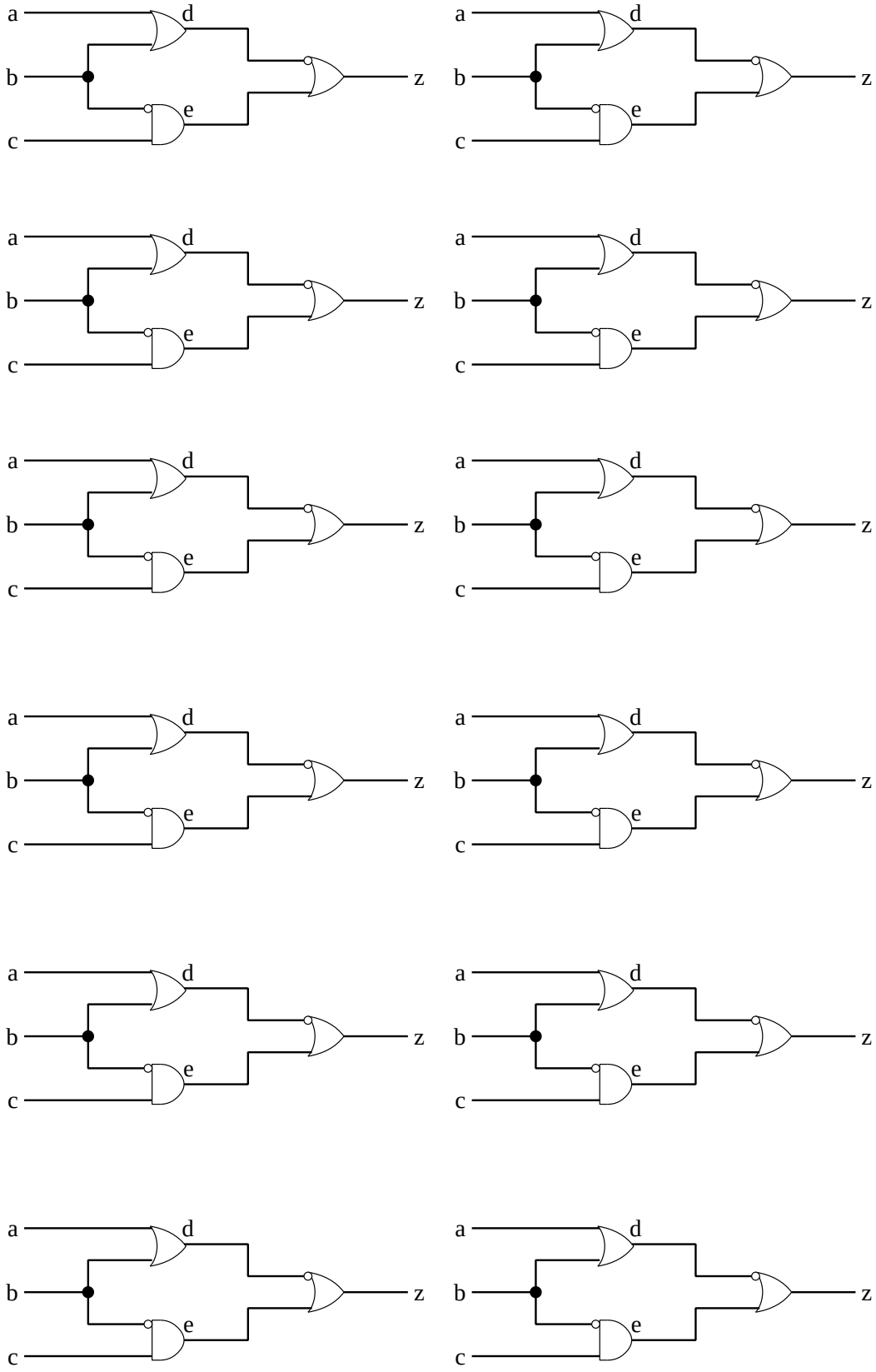
1. There are copies of the circuit and Karnaugh-map templates on the pages following this question.

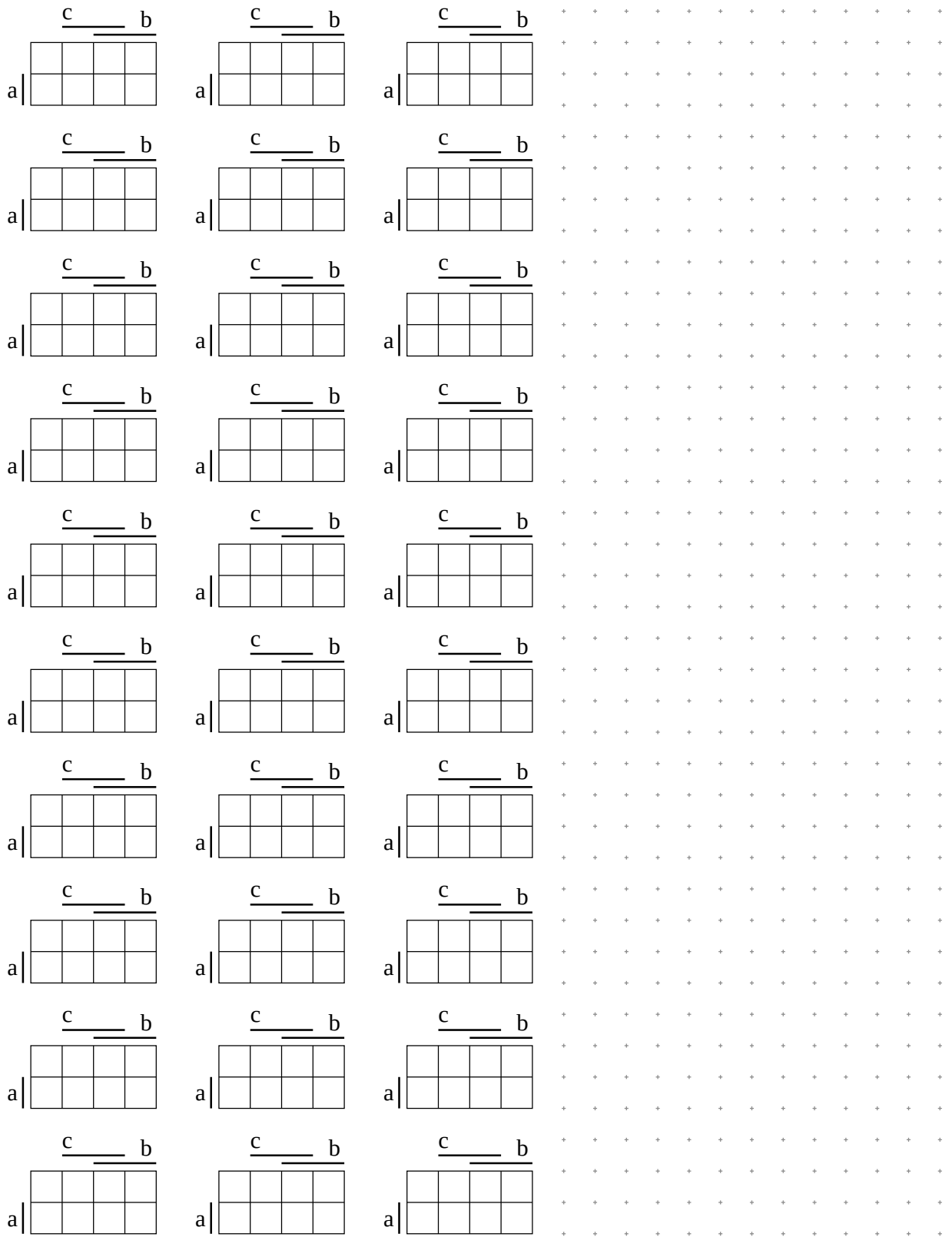
Q5a (15 Marks) Test Vectors

You have time to run at most three test vectors. Which test vectors should you run, and in which order should you run them?

Test vector #1	
Test vector #2	
Test vector #3	

Extra copies for work




c
b
a

Q5b (5 Marks) Coverage

With the test vectors that you chose, what fault coverage will you achieve?

Fault coverage