
ECE-327 Midterm

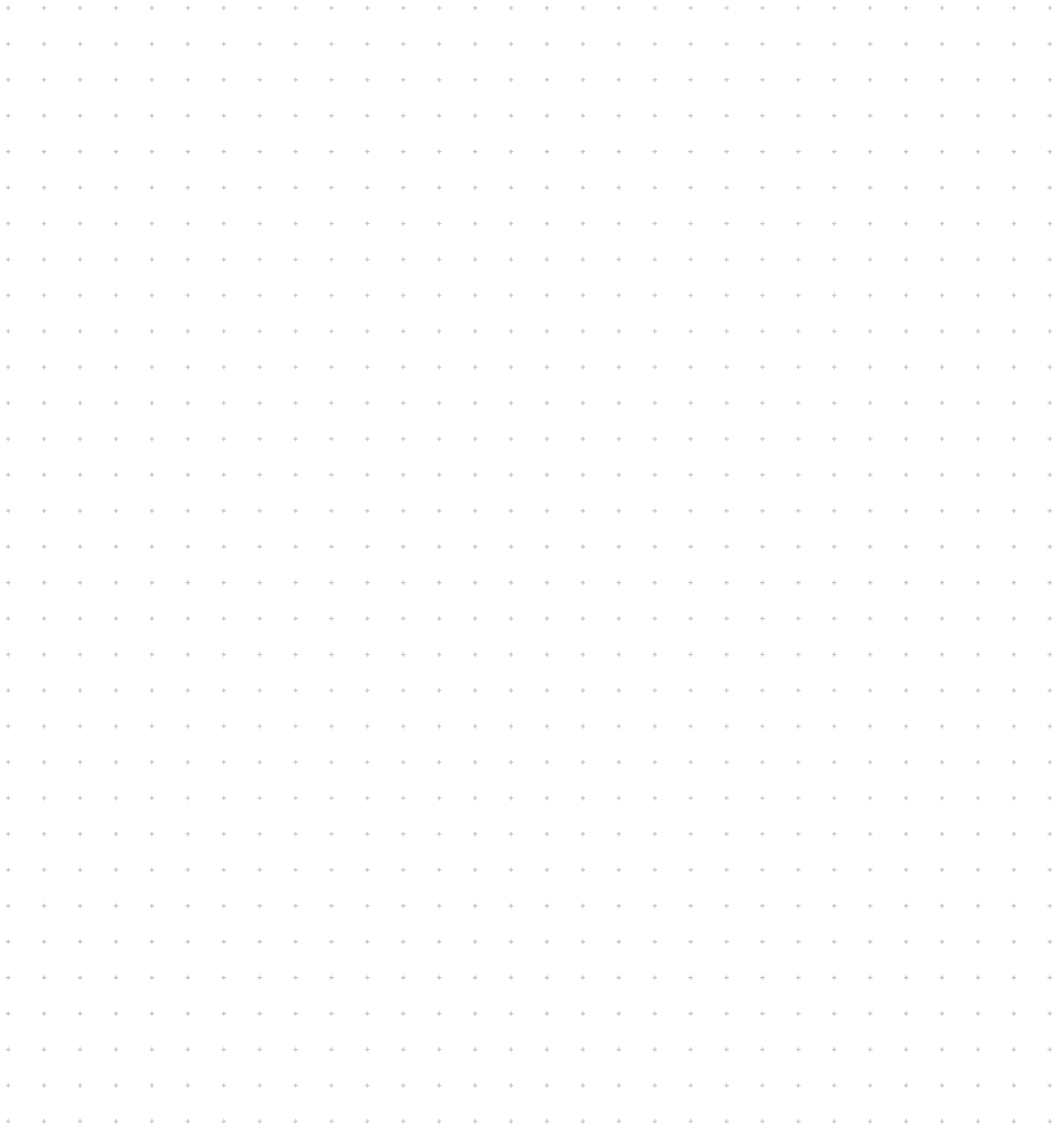
2020t1 (Winter)

Instructions and General Information

- 100 marks total
- There are extra pages for scratch work at the end of the exam.
- If you need *additional scratch* paper, request some from a proctor. The work done on the *additional scratch* paper will not be marked. **All answers to be marked must be on the exam paper.**
- The proctors and instructors will **not answer questions**, except in cases where an error on the exam is suspected. If you are confused about a question, write down your assumptions or interpretation.
- **Justifications** of answers will be marked according to correctness, clarity, and concision.
- To earn part marks, you must show the formulas you use and all of your work.

		Total	Approx.	
		Marks	Time	Page
Q0	!!Almost Free!!	2	2	3
Q1	VHDL Semantics	21	15	4
Q2	Area Analysis	25	15	8
Q3	FSM	27	18	10
Q4	DFD	27	18	14
<hr/> Totals		100	68	

This page is for scratch work for any question.



Q0 (2 Marks) !!Almost Free!!

(estimated time: 2 minutes)

Q0a (1 Mark) Best part

What is the best part of the course?

Q0b (1 Mark) Most improve

What one thing could be done to most improve the course for the remainder of the term?

Q1 (21 Marks) VHDL Semantics

(estimated time: 15 minutes)

For each pair of VHDL programs in Q1a and Q1b, answer whether the signal *z* has the same behaviour in both programs.

NOTES:

1. The code shown is the body of the architecture.
2. All signals are of type `std_logic`.
3. The inputs are `a`, `b`, and `clk`.
4. “*Same simulation cycle behaviour*” means that the two programs have the same number of simulation cycles and that at the end of each simulation cycle, *z* has the same value in both programs.
5. Similarly, “*same simulation round behaviour*” means that the two programs have the same number of simulation rounds and that at the end of each simulation round, *z* has the same value in both programs.
6. If the programs do *not* have the same behaviour:
 - Describe (with text or waveforms) the behaviour of the inputs that will cause the different behaviour.
 - Describe (with text or waveforms) how the behaviour of *z* is different in the two programs.
7. If the programs do have the same behaviour: **justify** your answer with text or waveforms.

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Q1a (10 Marks)

Program 1

```
c <= not a;  
z <= b and c;
```

Program 2

```
process (a,b) begin  
  z <= b and not a;  
end process;
```

Handwriting area consisting of a grid of small '+' symbols.

z has the same simulation *cycle* behaviour **Yes** **No**

Handwriting area consisting of a grid of small '+' symbols.

z has the same simulation *round* behaviour **Yes** **No**

Q1b (10 Marks)

The lines of code that are different in the two programs are denoted with underline.

Program 1

```

process begin
  clk <= '0';
  wait for 5 ns;
  clk <= '1';
  wait for 5 ns;
end process;

```

```

process begin
  wait until rising_edge(clk);
  z <= a;
end process;

```

Program 2

```

process begin
  clk <= '0';
  wait for 5 ns;
  clk <= '1';
  wait for 5 ns;
end process;

```

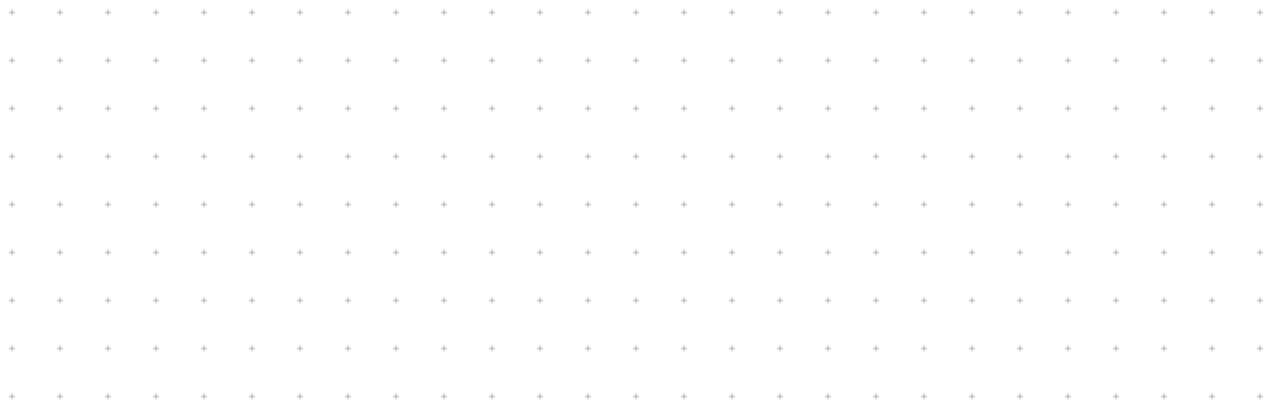
```

process begin
  wait for 5 ns;
  z <= a;
end process;

```



z has the same simulation *cycle* behaviour **Yes** **No**



z has the same simulation *round* behaviour **Yes** **No**

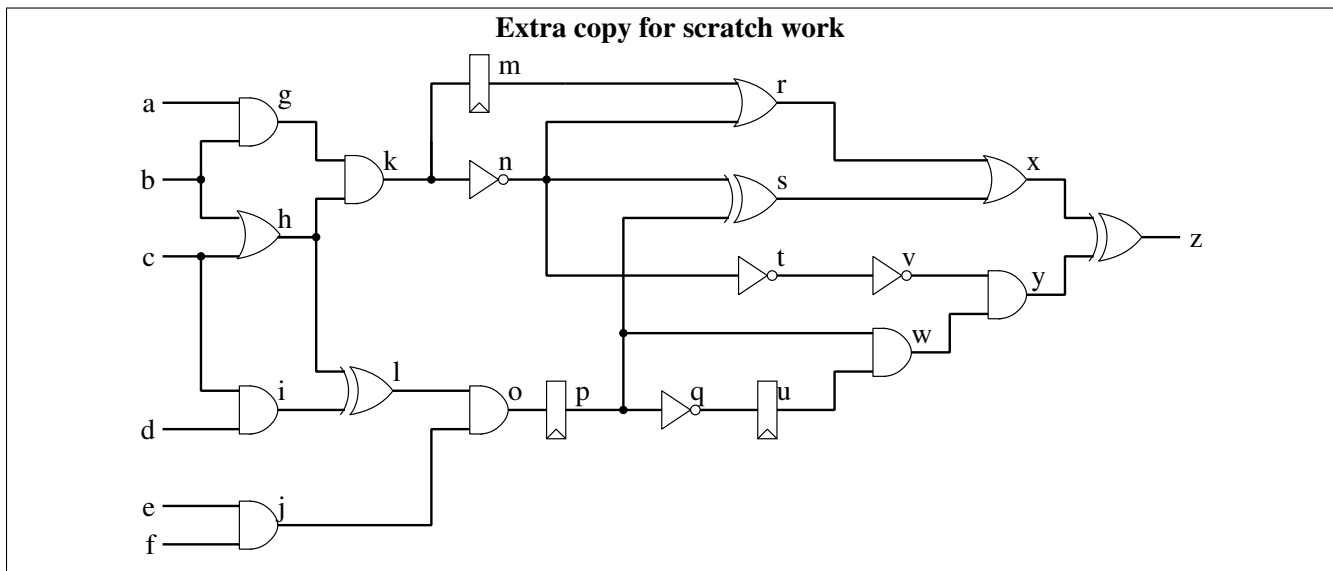
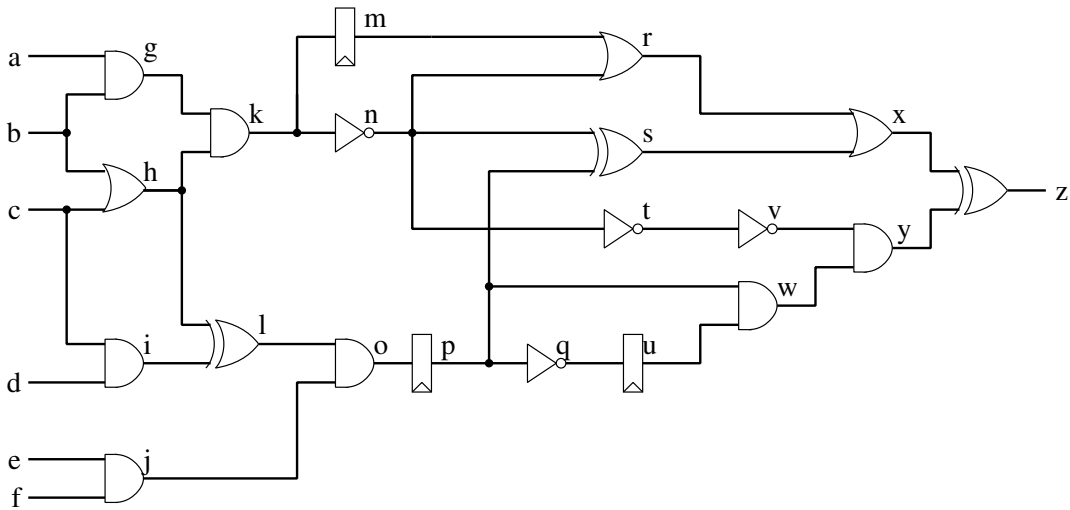
Q2 (25 Marks) Area Analysis

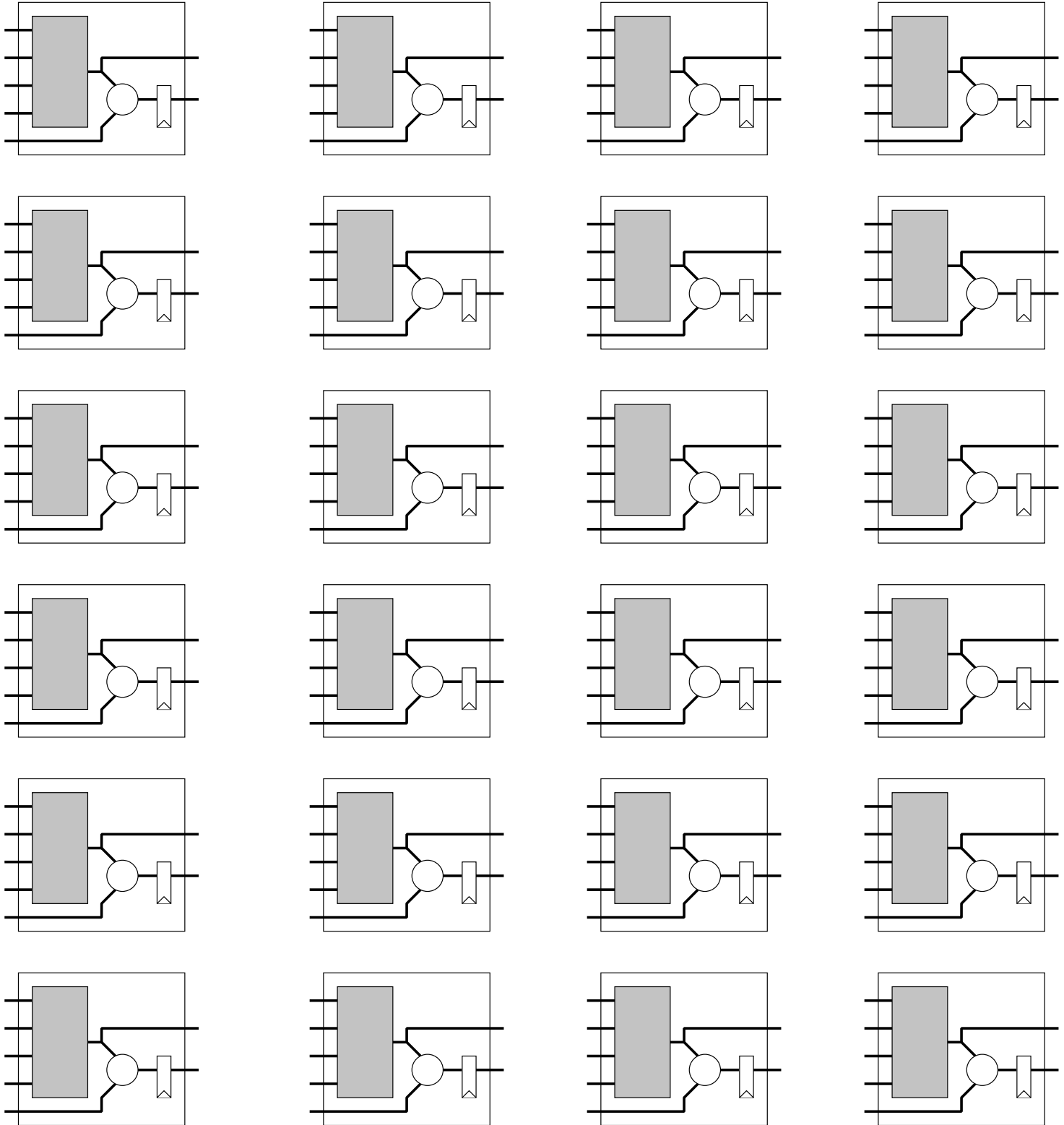
(estimated time: 15 minutes)

Design an FPGA implementation of the gate-level circuit shown below that uses the minimum number of FPGA cells. Use the FPGA cells on the following page to answer the question.

NOTES:

1. The primary inputs of the circuit are: a, b, c, d, e, and f.
2. The primary output of the circuit is: z.
3. Do not perform any logic optimizations.
4. For each FPGA cell that you use:
 - Label the input and output ports of the cell using the signal names from the gate-level circuit for ports that you use and **NC** (for no-connect) for ports that you do not use.
 - Show the configuration for the internal multiplexer.





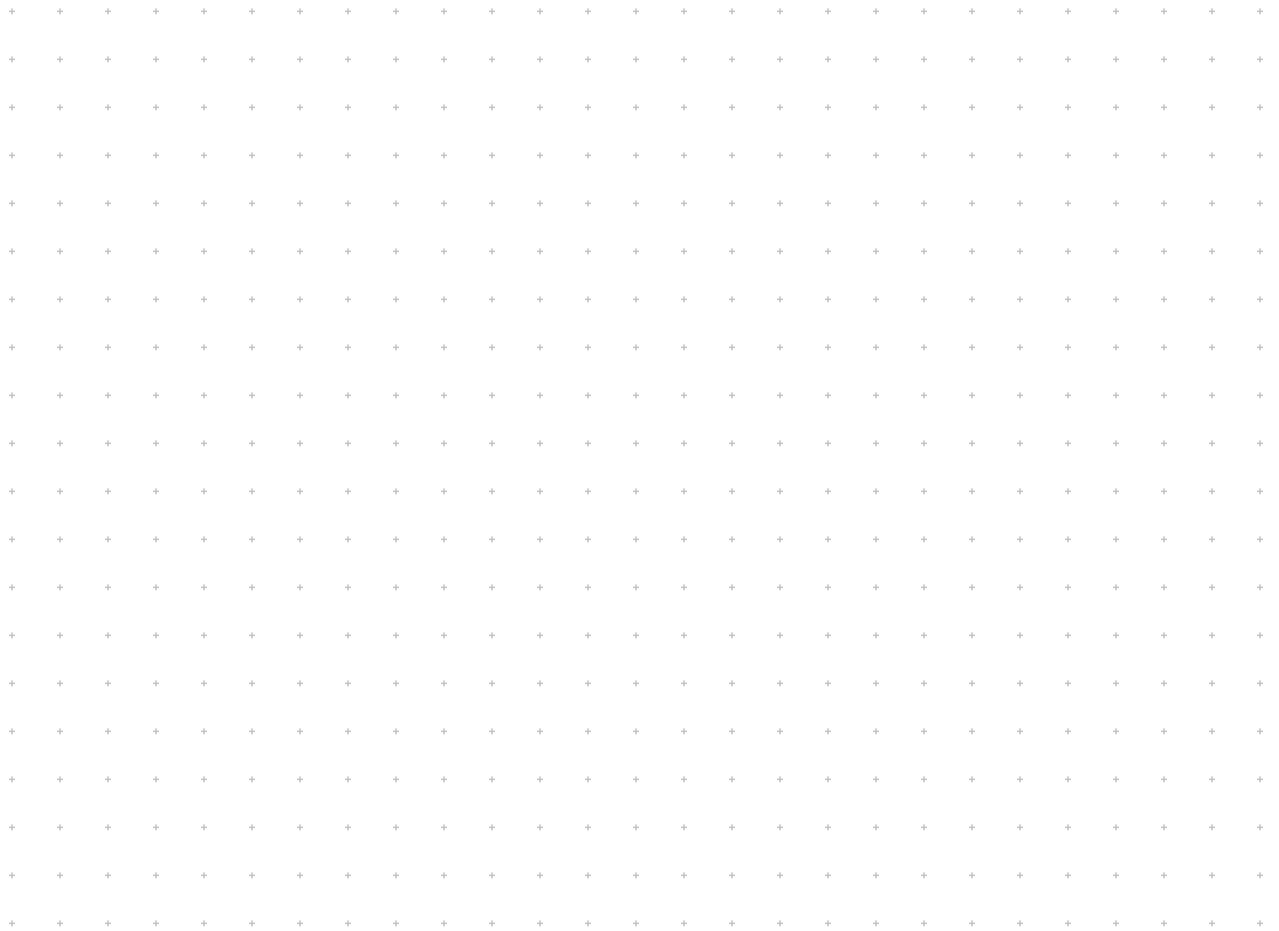
Total number of cells used:

**This page is for scratch work.
The next two pages are for your answer.**

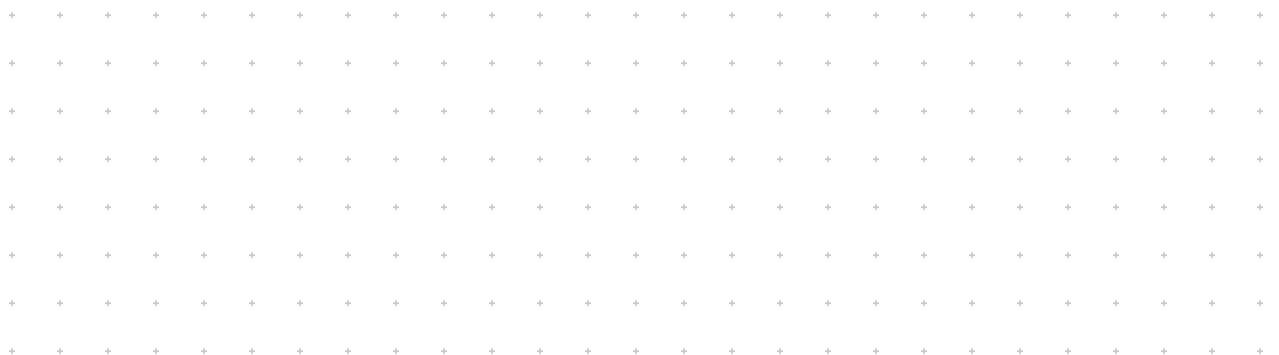


Q3b (9 Marks) Next-State Circuitry

Draw a schematic for the next-state circuitry.

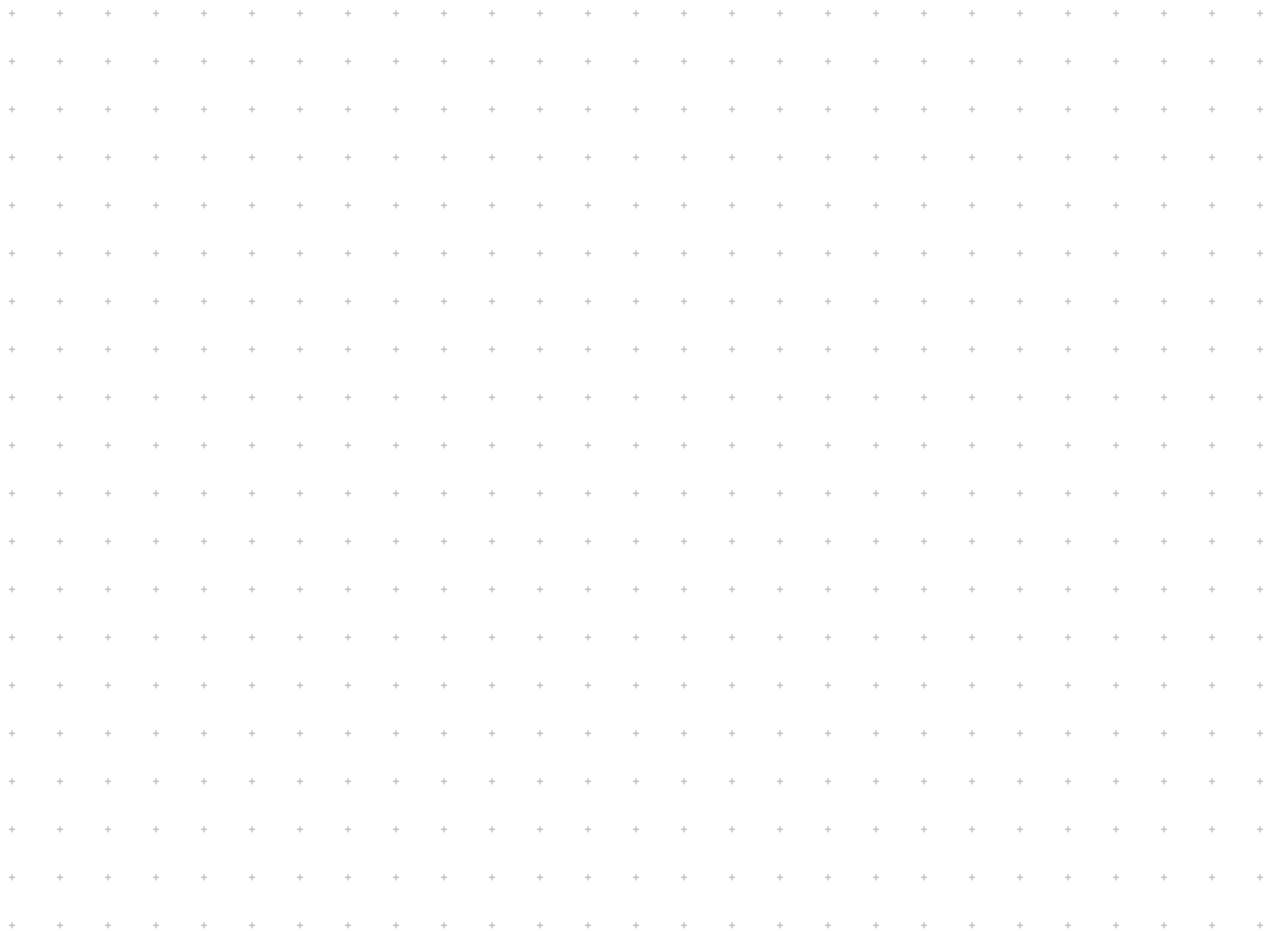


Write an expression for each control signal (mux-select or chip-enable) in the next-state circuitry.

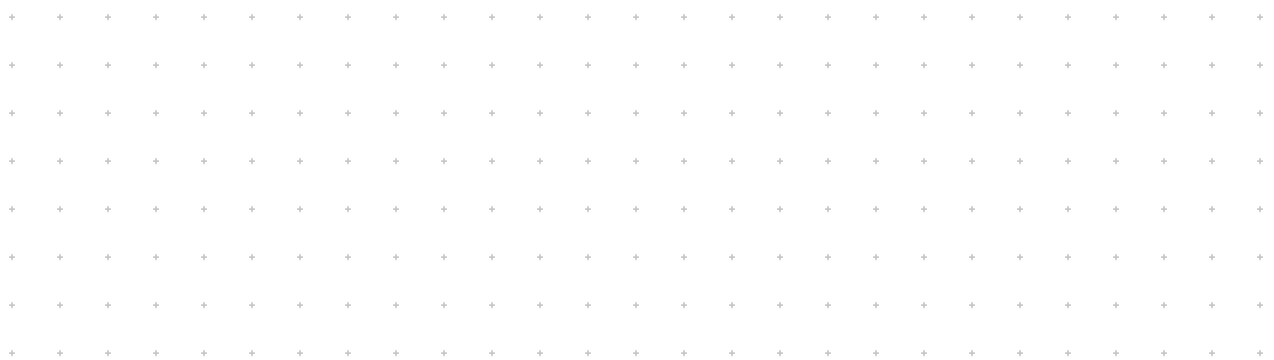


Q3c (14 Marks) Datapath Circuitry

Draw a schematic for the datapath circuitry.



Write an expression for each control signal (mux-select or chip-enable) in the datapath circuitry.



Q4 (27 Marks) DFD*(estimated time: 18 minutes)*

In this question, you will design and analyze a dataflow diagram for the equation:

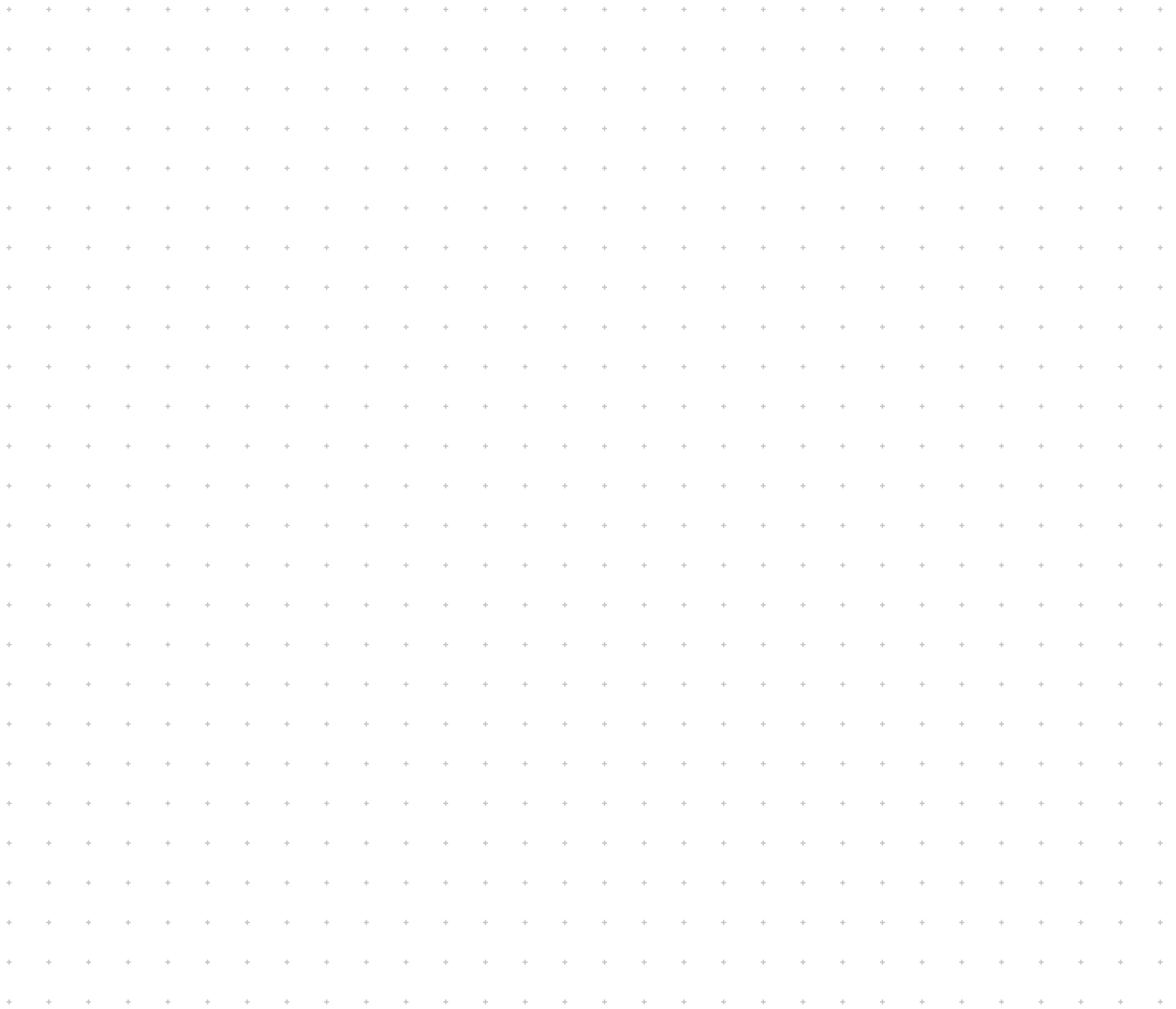
$$z = a*e + b + b*e + 7*d + c*d$$

NOTES:

1. Inputs shall be combinational and outputs shall be registered.
2. The delay of a multiplier is approximately twice that of an adder.
3. Optimization goals in order of decreasing importance:
 - (a) minimize number of *multipliers*
 - (b) minimize *clock period*
 - (c) minimize *latency*
 - (d) minimize number of *adders*
 - (e) minimize number of *registers*
 - (f) minimize number of *input ports*
 - (g) minimize number of *output ports*
4. Input values may be read in any clock cycle, but each input value shall be read exactly once.
5. Algebraic optimizations are allowed, as long as the final value of z is correct.
6. You do *not* need to perform allocation.

Scratch work

The next page is for your answer



Analysis:

Latency:

Clock period:

Number of muls:

Number of adds:

Number of regs:

Number of input ports:

Number of output ports:

This page is for scratch work for any question.

