1) Implement the equation \( X = \left( \left( A' + B' \right) \left( C' + D' + E' \right) + F' \right) G' \) using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS \( W/L = 2 \) and PMOS \( W/L = 6 \). Assuming \( L = 1 \) unit. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?

**Solution**

Rewriting the output expression in the form \( X = \left( \left( A + B \right) \left( C + D + E \right) + F \right) G = \left( \left( AB + CDE \right) \right) F \) allows us to build the pulldown network by inspection (parallel devices implement an OR, and series devices implement an AND). The pullup network is the dual of the pulldown network.

The plot shows sizes that meet the requirement - in the worst case, the output resistance of the circuit matches the output resistance of an inverter with NMOS \( W/L = 2 \) and PMOS \( W/L = 6 \).

The worst case pull-up resistance occurs whenever a single path exists from the output node to Vdd. Examples of vectors for the worst case are \( ABCDEFG = 1111100 \) and \( 0101110 \). The best case pull-up resistance occurs when \( ABCDEFG = 0000000 \).

The worst case pull-down resistance occurs whenever a single path exists from the output node to GND. Examples of vectors for the worst case are \( ABCDEFG = 0000001 \) and \( 0011110 \).

The best case pull-down resistance occurs when \( ABCDEFG = 1111111 \).
2) Either NAND gates or NOR gates can be used for implementing Boolean functions. Discuss which one of the two is more appropriate to be implemented in (i) complementary static CMOS logic, (ii) pseudo-NMOS logic. Explain in a few sentences.

Solution

The figures above show the complementary static CMOS implementation and pseudo-NMOS implementation of NAND and NOR gates. Let’s first consider the complementary static CMOS implementation. For the NAND gates, the PMOS transistors are in parallel whereas, for the NOR gate they are in series. The PMOS transistors in series would need twice the width of the transistors in parallel to have the same current drive. We also know that the mobility of PMOS transistors is 2 to 3 times lower than that of NMOS transistors. Hence the size of the NAND is smaller than the size of NOR if both are implemented in complementary static CMOS logic.

For the pseudo NMOS implementation, the PMOS transistors in both NAND and NOR are equally sized (assumption). The NMOS transistors in the NAND gate are in series, which imposes that NAND is physically bigger than NOR gate if they are sized for the same performance.
3) Consider the circuit in Figure P3. Assuming short channel transistors in 0.25 μm CMOS technology.

![Figure P3](image)

a) What is the output voltage if only one input is high? If all four inputs are high?

**Solution**

\[ I_D = k \cdot \frac{W}{L} \left( V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 - \lambda \cdot V_{DS}) \]

Consider a case when one input is high: \( A = V_{DD} \) and \( B = C = D = 0 \) V. Assume that \( V_{out} \) is small enough that \( V_{min} = V_{DSAT} \) for the PMOS device, and \( V_{min} = V_{DS} = V_{out} \) for the NMOS devices. Solve for \( V_{out} \) by setting the drain currents in the PMOS and NMOS equal to each other, \( |I_{DP}| = |I_{DN}| \), where the drain currents are functions of \( V_{out} \), \( V_{DD} \), and the device parameters.

\( V_{out} = 102 \text{ mV} \), and \( I_D = 35.7 \mu A \).

Now verify that the assumptions for \( V_{min} \) are correct. For the PMOS: \( V_{DS} = -2.34 \) V, \( V_{DSAT} = -1 \) V, \( V_{GT} = -2.1 \) V, therefore \( V_{min} = V_{DSAT} \). For the NMOS: \( V_{DS} = 102 \text{ mV}, V_{DSAT} = 630 \text{ mV}, V_{GT} = 2.07 \) V, therefore \( V_{min} = V_{DS} \).

Consider the case when all inputs are high: \( A = B = C = D = V_{DD} \). For these hand calculations, this is numerically equivalent to a circuit with a single NMOS device with \( W/L = 4 \times 1.5 \) and its gate tied to \( V_{DD} \). Now, the analysis used above for the case when one device is on can be reused, replacing \( W/L \) of the NMOS with \( 6 \), and using the same assumptions for \( V_{min}, V_{out} = 25 \text{ mV}, I_D = 35.9 \mu A \). The assumptions for \( V_{min} \) are correct.

b) What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

**Solution**

Notice in part a) that the drain current in the PMOS is 35.7 μA with one NMOS on and 35.9 μA with four NMOS devices on. The current in the PMOS can be approximated as 35.8 μA when any number of NMOS devices are on and 0 μA when all four are off. The probability that all four NMOS devices are off is \((1-\rho)^4\) where \( \rho \) is the probability an input is high. Therefore,
\[ P_{AVG} = P_{OFF} \cdot (1 - \rho)^4 + P_{ON} \cdot [1 - (1 - \rho)^4] \]

where \( P_{OFF} = 0 \) W, and \( P_{ON} = 89.5 \) μW. \( P_{AVG} = 83.9 \) μW when \( \rho = 0.5 \) and \( P_{AVG} = 30.7 \) μW when \( \rho = 0.5 \).

4) Consider a conventional 4-stage Domino logic circuit as shown in Figure P4 in which all precharge and evaluate devices are clocked using a common clock \( \phi \). For this entire problem, assume that the pulldown network is simply a single NMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all \( T/2 \). Assume that the transitions are ideal (zero rise/fall times).

**Figure P4**

a) Complete the timing diagram for signals \( Out1, Out2, Out3 \) and \( Out4 \), when the \( IN \) signal goes high before the rising edge of the clock \( \phi \) as given below. Assume that the clock period is 10 \( T \) time units.

**Solution**

The timing diagram is shown below.
b) Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock \( \phi \) is initially in the precharge state \((\phi=0\) with all nodes settled to the correct precharge states), and the block enters the evaluate period \((\phi=1)\). Is there a problem during the evaluate period, or is there a benefit to the overall performance? Explain.

**Solution**

There is no problem during the evaluate stage. The precharged nodes remain charged until a signal propagates through the logic, activating the pull-down network and discharging the node. In fact, this topology improves the circuit’s robustness in terms of charge sharing affecting the output for any generic pull-down network, and reduces the body effect in the pull-down network.

c) Assume that the clock \( \phi \) is initially in the evaluate state \((\phi=1)\), and the block enters the precharge state \((\phi = 0)\). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

**Solution**

There is a problem during the precharge stage. If all precharged nodes are discharged during the evaluate stage, when the precharge FETs simultaneously turn on, the pull-down networks will initially remain on, creating a short circuit. This continues in each gate until the previous gate charges, disabling its pull-down network.

5) Consider the circuit of Figure P5 fabricated in 0.25\(\mu\)m CMOS. Let \( C_X = 50 \) fF, \( M_r \) has \( W/L = 0.375/0.375 \), \( M_n \) has \( W/L_{eff} = 0.375/0.25 \). Assume the output inverter doesn’t switch until its input equals \( V_{DD}/2 \). Use the 0.25\(\mu\)m CMOS model in textbook for calculations.

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a) How long will it take \( M_n \) to pull down node \( x \) from 2.5 V to 1.25 V if \( I_n \) is at 0 V and \( B \) is at 2.5V?
Solution

To determine the time required for these transitions, we will find the average currents in the FETs $M_i$ and $M_n$. The equivalent resistance method will not suffice since it does not account for both devices being on.

For $M_i$, $I_{vdd=2.5} = 0$ since $V_{ds} = 0$. For the other case, the PMOS device is velocity saturated, so:

$$I_{vdd=1.25} = (-30)(1)(-2.1+0.5)(1+0.1*1.25) = -54 \mu A.$$  The average current in the PMOS is $-27 \mu A$.

$M_n$ is in the velocity saturation region for both endpoints of the transition. The two currents are therefore:

$$I_{vdd=2.5} = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 219 \mu A.$$  

$$I_{vdd=1.25} = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 205 \mu A.$$  

And the average current in the NMOS is $212 \mu A$.

The total current DISCHARGING the capacitor is $211 \mu A - 27 \mu A = 185 \mu A$.

The time for the transition is then

$$t = \frac{C \cdot \Delta V}{I_{avg}} = \frac{50 \mu F \cdot 1.25V}{185 \mu A} = 338 ps .$$

b) How long will it take $M_n$ to pull up node $x$ from 0V to 1.25V if $V_{in}$ is 2.5V and $V_B$ is 2.5V?

Solution

For the LH transition, the PMOS “keeper” is off. The NMOS $M_n$ is the only FET that is on for this transition. We present both methods for finding the pull-up time.

Equivalent Resistance: We need to perform a different sweep for this measurement than the regular $I_{dss} vs V_{ds}$ sweep. In this case, $V_{ds}$ is changing because the source node of the FET is rising. Since the source voltage is changing, $V_{gs}$ also is reducing as node $x$ rises. This effectively “turns down” the current the NMOS can sustain. Performing the appropriate sweep and measuring $R_{eq}$ gives $R_{eq} = (11.3k \Omega + 34.7k \Omega) / 2 = 23k \Omega$. Thus, $t = \frac{0.69 \cdot C \cdot R_{eq}}{0.69 \cdot 50 \mu F \cdot 23k \Omega} = 794 ps$.

Average Current: When $x = 0$, the pass transistor has a $V_{gs} = 2.5$ and a $V_{ds} = 2.5$, so it is velocity saturated.

$$I_{x=0} = (115)(1.5)(0.63)(2.07-0.63/2)(1+0.06*2.5) = 219 \mu A.$$  

When $x = 1.25$, the pass transistor has $V_{ds} = 1.25$ and $V_{gs} = 1.25$. It is still velocity saturated, but notice that $V_{gs}$ has decreased. Thus,

$$I_{x=1.25} = (115)(1.5)(0.63)(1.25-0.43-0.63/2)(1+0.06*1.25) = 59 \mu A.$$  

The average current is then $I_{avg} = 139 \mu A$.

$$t = \frac{C \cdot \Delta V}{I_{avg}} = \frac{50 \mu F \cdot 1.25V}{139 \mu A} = 450 ps .$$
c) What is the minimum value of $V_B$ necessary to pull down $V_X$ to 1.25V when $V_{In} = 0V$?

**Solution**

In order for $M_n$ to pull node $x$ low, the current in $M_r$ must equal or exceed the current that charges up the capacitor at every point in the transition. The maximum current in $M_r$ occurs when $x = 1.25V$, and it is (from part a) $I_{Mr} = 54uA$. We can write a current equation for $M_n$ at this point in the transition and solve for $V_B$:

Note that $M_n$ is velocity saturated at this point: $54 = (115)(1.5)(0.63)(V_B-0.43-0.63/2)(1+0.06*1.25)$.

Solving gives $V_B = 1.207V$.

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6) Figure P6 shows a two-input multiplexer. For this problem, assume independent, identically-distributed uniform white noise inputs at A, S, and B.

![Figure P6](image)

a) Find the exact signal ($P_1$) and transition ($P_{0 \rightarrow 1}$) formulas for nodes $X$, $Y$, and $Z$ for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic np-CMOS implementation. Assume only one transition during a clock cycle.
For Z,

\[\begin{array}{ccccc|c}
A & S & B & S' & Z \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 1 & 1 \\
0 & 1 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 & 0 \\
1 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 1 & 1 \\
1 & 1 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 & 1 \\
\end{array}\]

If we represent the truth table of the schematic we will see that \( P_1 = 0.5 \). Then
\[ P_{0 \rightarrow 1} = P_0 P_1 = 0.25 \times 0.5 = 0.25. \]

If it’s a dynamic np-CMOS implementation:

For X, \( P_1 = 0.75 \). In order to obtain the transition probability, an n-tree dynamic gate will be assumed. In this case: \( P_{0 \rightarrow 1} = P_0 = 0.25 \)

The analysis for Y is equal to the analysis for X.

For Z, using the truth table of the schematic we obtain, again, \( P_1 = 0.5 \). For the transition probability, it will be assumed that a np-CMOS structure is used. Then, Z is the output of a p-tree dynamic gate. Then: \( P_{0 \rightarrow 1} = P_1 = 0.5 \).

(Reference for the above is on page 289 in 2nd edition textbook)

b) Compute the switching power consumed by the multiplexer in Figure P6. Assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where \( C = 0.3 \) pF. Assume that \( V_{DD} = 2.5 \) V and independent, identically-distributed uniform white noise inputs, with events occurring at a frequency of 100 MHz. Perform this calculation on (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation.

On a static, fully complementary CMOS implementation

**Solution**

Switching power is:
\[ P_{SW} = \alpha \cdot f \cdot C \cdot V_{DD}^2 = (\alpha_{X0 \rightarrow 1} + \alpha_{Y0 \rightarrow 1} + \alpha_{Z0 \rightarrow 1}) \cdot f \cdot C \cdot V_{DD}^2 \]

We calculated in part(a) the probabilities of a \( 0 \rightarrow 1 \) transition for each node:
P_{0 \rightarrow 1} for X and Y is 0.1875 and for Z is 0.25.

Thus, P_{SW} = (2*0.1875+0.25)*100MHz*0.3pF*2.5^2 = 117.2uW.

On a dynamic CMOS implementation

We calculated the probabilities in part (a):

For X and Y is 0.25 and for Z is 0.5.
Thus, P_{SW} = (2*0.25+0.5)*100MHz*0.3pF*2.5^2 = 187.5uW.

c) Is the switching power P_{SW} of the dynamic implementation in part (b) reflecting the total power consumed? Explain, in a few sentences.

In part (b), the clock power is assumed = 0. Indeed, the clock power of dynamic logic can be significant. For a fair comparison, the clock power due to the circuit load must be taken into considerations. In modern IC, the clock power of dynamic logic is taking up more than 30% of the total chip power consumption.